Feasibility Study for Supercapacitor-Based Spacecraft Power System and its Development

Masatoshi Uno

DOCTOR of PHILOSOPHY

Department of Space and Astronautical Science
School of Physical Science
The Graduate University for Advanced Studies

March, 2012

Synopsis

Traditional spacecraft power systems are essentially based on secondary batteries, which are usually operated under tightly controlled conditions in order to meet spacecraft life requirements. However, conventional secondary battery technologies are facing many daunting obstacles to achieve longer life performance and improved operability. Supercapacitors (SCs) are emerging energy storage devices that offer a number of advantages over secondary batteries, which are attractive to meet increasing demand for spacecraft energy storage sources.

The objectives of this work are the feasibility study for SC-based spacecraft power systems and development thereof. Major hurdles for SCs to be an alternative to secondary batteries in spacecrafts are posed in Chapter 1, and are addressed in the following chapters. In Chapters 2–4, SC technologies are compared with conventional lithium-ion batteries (LIBs), and the feasibility of SCs being an alternative energy storage source in spacecraft power systems is studied. In Chapters 5–8, power system components for SC-based power systems are developed considering innate SC characteristics.

In Chapter 2, the scientific background of SCs and LIBs is covered to highlight characteristics, advantages, and drawbacks of SCs. Spacecraft power system architectures for SCs are also considered taking SC characteristics into account.

Chapter 3 includes cycle life evaluations as well as establishment of accelerated ageing testing and cycle life prediction model for SCs. Charge–discharge cycle tests emulating low-Earth orbit spacecraft profiles are performed at various conditions, and the feasibility of ageing acceleration is discussed based on the experimental life performance. Cycle life prediction model incorporating ageing acceleration factor is also established.

In Chapter 4, the system mass comparison is made between LIB- and SC-based spacecraft power systems, which consist of an energy storage source, photovoltaic (PV) arrays, and power conditioning system. The gap between LIBs and SCs in terms of specific energy can be bridged to great extent by using SCs with deep depth of discharge. In addition, the mass of PV arrays in the SC-based system can be saved by introducing a constant-power charging scheme.

In Chapter 5, novel cell voltage equalizers are proposed considering SC characteristics and general requirements in space. Equalization performances for series-connected SCs are experimentally demonstrated, and comparisons with conventional equalizers are made in terms of circuit complexity and design flexibility.

Chapter 6 proposes novel single-switch equalization chargers, which can simplify the power system configuration as a whole by integrating a charge regulator and equalizers into one unit, and demonstrates their charge performance for series-connected SCs.

In Chapter 7, novel unregulated interface converters, which are bidirectional dc-dc converters without voltage regulation, are proposed to achieve high-efficiency power conversions over wide voltage range. The proposed converters employ novel concepts, and exhibit unique characteristics.

Finally, in Chapter 8, an experimental SC-based power system is considered for a 28-V sun-regulated bus architecture with 50 W load power requirement, and is designed using the power system components proposed in Chapters 6 and 7. The system experimental test is performed to verify the operation of the SC-based power system.

Acknowledgement

My heartfelt appreciation goes to Prof. Koji Tanaka, who has been extremely helpful not only in providing worthwhile technical comments but also offering advices on authoring and styling technique. I am also indebt to Prof. Kazuyuki Hirose whose comments and suggestions made enormous contribution to my work. Finally, I would like to thank Japan Aerospace Exploration Agency (JAXA) for a grant that made it possible to complete this study.

Abstract

The aims of this work are to study the feasibility of supercapacitor (SC) technologies to be alternatives to secondary batteries in spacecraft power systems, and to develop power system components for SC-based power systems.

Mass saving, life extension, and improvement in operational flexibility are a primary research and development challenge in spacecraft power systems, where secondary battery technologies have been used as energy storage sources. In order to meet long mission life requirements of spacecrafts, secondary batteries need to be operated under precisely controlled conditions, implying that secondary battery technologies are facing obstacles to achieve longer life performance and improved operability. SC technologies offer longer life performance over wide temperature range which is attractive for spacecraft power systems. However, in order for SC technologies to be used as alternatives to secondary batteries, research efforts on system and component level are needed to address and overcome major hurdles, which originate from innate SC characteristics, including: (1) need of accelerated ageing testing method and cycle life prediction model, (2) mass increase due to low specific energy of SCs, thus needing a consideration for mass reduction at a power system level, (3) voltage imbalance among series-connected SCs, and (4) large voltage variation during cycling. Among a variety of SC technologies, electric double-layer capacitors (EDLCs) and lithium-ion capacitors (LICs), which are different types of SCs, were used to establish evaluation methods for feasibility study and to develop power system components universally applicable to other SC technologies.

Since cycle life performance of SCs is inherently longer than that of conventional secondary batteries, an ageing acceleration and/or cycle life prediction model are necessary to design and evaluate spacecraft power systems properly. Although many research efforts have been done for life evaluations and ageing accelerations for SCs in terrestrial use, similar studies emulating conditions in spacecrafts are necessary because operational conditions, such as cycle profiles and current rates, are totally different. Cycle life testing emulating typical low-Earth orbit profiles was performed at various conditions to study the feasibility of accelerated ageing testing. Resultant ageing trends could be extrapolated linearly with the square root of the number of cycles as the x-axis. Degradations were mainly influenced by temperature, and were governed by the Arrhenius model, which determines a temperature dependence of chemical reaction rates. Ageing acceleration factors were obtained from activation energies determined by the Arrhenius equation. A cycle life prediction model was established combining the linear extrapolation and acceleration factor. The experimental and predicted aging trends were in good agreement, verifying that achievable cycle life at a given temperature is predictable with the established model.

In order for SCs to be of benefit to a spacecraft as a whole, an SC-based power system must outperform in terms of system mass and/or operational life. Comparative analyses on power system mass were made for lithium-ion battery (LIB)-based and SC-based systems consisting of

photovoltaic (PV) arrays and power conditioning system components. The gap between LIBs and SCs in terms of specific energy can be bridged to great extent by operating SCs with deep depth of discharge. In addition, the mass of the PV arrays in the SC-based system can be saved by introducing a constant-power charging scheme for SCs. The comparative analysis results implied that the LIC-based power system has a potential to be an alternative energy storage source for long life requirement, for which LIBs must be operated with very shallow DoD to mitigate degradations.

Various equalization techniques for LIBs have been proposed and developed for not only terrestrial but also space applications, but further improvement is desired for SCs in space. Novel cell voltage equalizers and equalization chargers, which can simplify the power system configuration as a whole by integrating a charge regulator and equalizers into one unit, were proposed taking into account SC characteristics and general requirements in spacecrafts, such as reliability, design flexibility, and poor variety of rad-hard circuit components. Since the proposed equalizers and equalization chargers can operate with a single switch, the circuit complexity can be dramatically reduced compared with conventional ones, thus contributing to meet the requirements. Their individual equalizers' performances were experimentally demonstrated using series-connected EDLCs.

Since voltage variations of SCs during charge–discharge cyclings are wider than those of secondary batteries, power conversion electronics with a wide operational voltage range are required for SCs to be used as alternatives to batteries. Traditional dc-dc power converters using magnetic components tend to be massive and inefficient for extended operational voltage range. Novel magnetic-less unregulated interface converters (UICs), which can achieve high-efficiency power conversions over wide voltage range, were also proposed for SCs. With the proposed UICs, bus voltage variations can be maintained within a desired voltage range, whereas an SC voltage varies significantly. EDLCs were experimentally cycled with the proposed UICs for the demonstrations.

Finally, an experimental 28-V SC-based power system with 50 W load power requirement was considered for a 60-V EDLC. The experimental SC-based power system was designed based on the sun-regulated bus architecture using the proposed equalization charger and the UIC, and the system operation was experimentally verified emulating sunlight-eclipse cycles.

Table of Contents

Chapter 1
Introductions

Mass reduction, life extension, and improvement in operational flexibility for energy storage sources are primary challenges in spacecraft power systems. Alkaline batteries, such as Ni-Cd, Ni-MH, and Ni-H_2 batteries, had been used as spacecraft energy storage sources until the emergence of lithium-ion battery (LIB) technologies. LIBs, which offer the highest specific energy among commercial secondary battery technologies, have replaced alkaline batteries as energy storage sources, and have been the mainstream not only in consumer electronics but also in spacecraft power systems since the mid 2000's. Extensive studies for LIBs have been underway to achieve even higher specific energy and longer life performance. However, since life performance of secondary batteries including LIBs is strongly dependent on operating conditions, batteries in spacecrafts are usually operated under tightly controlled conditions in order to meet life requirements. Depth of discharge, charge voltage level, and operation temperature are strictly controlled to maximize operational life of batteries by mitigating electrochemical and mechanical degradations. In other words, secondary battery technologies are facing many daunting obstacles to achieve longer life performance with improved operability at comparable mass.

Supercapacitors (SCs), also designated as electrochemical capacitor or ultracapacitor, are emerging energy storage devices that offer several major advantages over the conventional secondary battery technologies in terms of life performance, power capability, temperature tolerance, and abuse tolerance. SCs have been attracting considerable attentions and been used mainly for high-power applications where SCs are used as high-power energy buffers, such as vehicular applications, regenerative systems in industries, and uninterruptible power supplies [1]–[6]. A number of research efforts have also been made for spacecraft hybrid power systems, in which SCs behave as a high-power auxiliary power source to complement secondary batteries and to meet high-power requirement for short duration [7]–[10].

Although conventional applications and research of SCs have been mainly limited to such high-power applications, the advantages offered by SCs, especially the long service life over wide temperature range, are also attractive for spacecraft energy storage sources to meet the increasing requirements. However, major hurdles originating from innate characteristics of SCs, which are listed below, must be addressed and overcome for SCs to be used as alternatives to secondary batteries in spacecraft power systems.

1) Establishment of accelerated ageing testing and cycle life prediction model
2) Possible mass increase due to low specific energies of SCs, thus needing a consideration for mass reduction at a power system level
3) Cell voltage imbalance originating from nonuniform individual cell properties of series-connected cells

4) Large voltage variations during cycling

Since cycle life performance of SCs is inherently long, an accelerated ageing testing method and/or a cycle life prediction model need to be established based on experimental life evaluation in order for SC-based power system to be designed properly. Low specific energy of SCs is the most daunting obstacle to employ SCs in spacecraft power systems where light energy storage sources are strongly desired. Hence, in addition to the efforts to increase their specific energy which are underway in terrestrial research sectors, the possibility of mass reduction at a power system level should be discussed to improve the likelihood of SC technologies being considered. The issue about the cell voltage imbalance has also been addressed for LIBs, and various kinds of cell voltage equalization techniques have been proposed and developed to mitigate or even eliminate such cell voltage imbalance. However, cell voltage equalizers with improved performance are still desired, and need to be designed considering not only SC characteristics but also general requirements in space. The large voltage variations of SCs during cycling poses a burden on conventional switching power converter designs in extending operational voltage range without diminishing power conversion efficiencies. Novel concepts for power conversion electronics may be beneficial to SC technologies to be adopted in spacecraft power systems.

The objectives of the works undertaken in this dissertation are the feasibility study for SC-based spacecraft power systems and development thereof. A variety of SC technologies have been developed or still under research and development [11]. In this study, two representative commercially available SC technologies, electric double-layer capacitors (EDLCs) and lithium-ion capacitors (LICs), which are different types of currently commercially available SCs, are used in order to establish universal evaluation methods for feasibility study and to develop spacecraft power system component universally applicable to future SC technologies.

Following chapters address and discuss the aforementioned major obstacles. Chapter 2 outlines fundamentals of LIBs, EDLCs, and LICs, as well as spacecraft power system architectures. Chapter 3 evaluates the cycle life performance of EDLCs and LICs, and discusses and establishes the feasibility of ageing acceleration and cycle life prediction model, respectively. In Chapter 4, the masses of LIB- and LIC-based power systems for a low-Earth-orbit spacecraft are compared based on mathematical analyses. Chapter 5 reviews conventional cell voltage equalizers, and proposes novel cell voltage equalizers considered suitable for SCs in space. Novel equalization chargers, which combine a charge regulator with cell voltage equalizers into one unit to simplify the power system configurations as a whole, are proposed in Chapter 6. Chapter 7 proposes unregulated interface converters (UICs) to achieve high-efficiency power conversions over wide voltage range. In Chapter 8, an experimental SC-based system is build based on system considerations, and a system level experimental demonstration test is performed for a sun-regulated 28-V power system with 50 W load power requirement using series-connected EDLCs.

References

[1] P. J. Grbović, P. Delarue, P. L. Moigne, and P. Bartholomeus, "Modeling and control of the ultracapacitor-based regenerative controlled electric drives," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 8, Aug. 2011, pp. 3471–6484.

[2] U. K. Madawala, D. J. Thrimawithana, and N. Kularatna, "An ICPT-supercapacitor hybrid system for surge-free power transfer," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, Dec. 2007, pp. 3287–3297.

[3] P. Thounthong, S. Rael, and B. Davat, "Control strategy of fuel cell and supercapacitors association for a distributed generation system," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, Dec. 2007, pp. 3225–3233.

[4] C. Abbey and G. Joos, "Supercapacitor energy storage for wind energy applications," *IEEE Trans. Ind. Appl.*, Vol. 43, No. 3, May/Jun. 2007, pp. 769–776.

[5] J. Jia, G. Wang, Y. T. Cham, Y. Wang, and M. Han, "Electrical characteristic study of a hybrid PEMFC and ultracapacitor system," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 6, Jun. 2010, pp. 1945–1953.

[6] W. Li, G. Joós, and J. Bélanger, "Real-time simulation of a wind turbine generator coupled with a battery supercapacitor energy storage system," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 4, Apr. 2010, pp. 1137–1145.

[7] T. Shimizu and C. Underwood, "Power subsystem design for micro-satellites using super-capacitor energy storage," 7*th Int. Energy Conversion Engineering Conf.* (*IECEC*), 2009, AIAA 2009-4500.

[8] M. J. Marcel, J. Baker, and K. Williams, "Design of an energy management system for a near space vehicle," 5*th Int. Energy Conversion Engineering Conf.* (*IECEC*), 2007, AIAA 2007-4800.

[9] M. J. Marcel and J. Baker, "Integration of ultra-capacitor into the energy management system of a near space vehicle," 5*th Int. Energy Conversion Engineering Conf.* (*IECEC*), 2007, AIAA 2007-4707.

[10] A. R. Aslan, A. Sofyali, E. Umit, C. Tola, I. Oz, and S. Gulgonul, "TURKSAT-3USAT: a 3U communication CubeSat with passive magnetic stabilization," *Recent Advances in Space Technologies (RAST)*, pp. 783–788, 2011.

[11] M. Jayalakshmi and B. Balasubramanian, "Simple capacitors to supercapacitors -an overview," *Int. J. Electrochem. Sci.*, Vol. 3, pp. 1196–1217, 2008.

Chapter 2
Lithium-Ion Battery and Supercapacitors

2.1 Introduction

Both lithium-ion batteries (LIBs) and supercapacitors (SCs) are energy storage devices. However, since their energy storage mechanisms as well as features are totally different, they have been used in different applications. This chapter outlines energy storage mechanisms and characteristics of LIBs and SCs, and compares their features, drawbacks, and characteristics. Possible spacecraft power system architectures for LIBs and SCs are also discussed taking their charge–discharge characteristics into account.

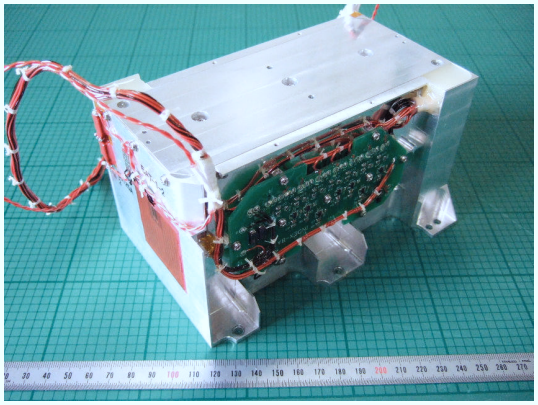
2.2 Lithium-Ion Battery

LIBs are the most common energy storage source not only in consumer portable electronics but also in recent spacecrafts. Lithium alloys, such as $LiCoO_2$, $LiNiO_2$, $LiMn_2O_4$, etc., are used as an active material for the positive electrode, while graphite carbon, in which lithium ions can intercalate, is used for the negative electrode. LIBs achieve the highest specific energy among commercial secondary batteries, with no memory effect and slow self-discharge rate when not in use. Vigorous research and development has been underway to achieve increased specific energy and extended life performance.

The energy storage mechanism of LIBs is based on electrochemical reactions. During charging, lithium ions carry the current from the positive to negative electrode through the organic electrolyte and separator, and vise versa during discharging. The cell reactions involve side reactions including degradation reactions, and the rates of electrochemical and mechanical degradations are strongly dependent on operating conditions, such as temperature, depth of discharge (DoD), and charge voltage. To extend service life by mitigating such degradations, LIBs need to be operated at reduced temperature with shallow DoD. Degradation mechanisms of LIBs can be characterized as two major factors; mechanical stress due to cycling and calendar degradations that take place even under floating or rest conditions. A cycle life prediction model considering these two factors separately has been established to predict cycle life under complicated cycling patterns [1].

The most prominent feature of LIBs is the highest specific energy among commercially available secondary batteries. Space qualified LIB cells achieve about 150 Wh/kg [1], which is about 2.5 times higher than that of traditional alkaline batteries. However, LIBs must be operated with great care to ensure years of safe operation without rapidly aging performance. Overcharging and/or operation above specified temperature range may lead to not only gas evolution due to electrolyte decomposition but also thermal instability of active materials. The decreased thermal instability of LIBs may cause accelerate irreversible deterioration and, in the worst case, an explosion or a fire. At the elevated temperature or in a fire, LIB cells become

(a)



(b)

Fig. 2.2.1. Photograph of (a) commercial off-the-shelf lithium-ion pouch cell and (b) pouch cell battery used for a small scientific satellite "REIMEI".

thermally unstable and release O_2 from active materials ($LiCoO_2$, $LiNiO_2$, or $LiMn_2O_4$), resulting in thermal runaway. Hence, not only operation voltage range but also temperature must be strictly controlled to ensure safety operation.

A number of LIBs for space applications have already been developed [1], tested [2]–[4], and implemented [5]. Commercial off-the-shelf lithium-ion pouch cells have also been used. For example, a small scientific satellite "REIMEI" employed $Li_xMn_2O_4$-based commercial off-the-shelf lithium-ion pouch cells, shown in Fig. 2.2.1(a) [6]. The pouch cells were potted with epoxy-based resin in a hard aluminum case, as shown in Fig. 2.2.1(b), in order to protect the pouch cell batteries from vacuum in space. The pouch cell battery equipped with REIMEI has been operated approximately 30000 cycles on orbit as of this writing, demonstrating that on-orbit battery's cycle life performance was not affected by the conditions in space. The potting technique used for REIMEI's pouch cell battery may also be used for SCs because most commercial SCs employ such pouch casing rather than robust metallic containers in order to increase their specific energies.

2.3 Supercapacitors

SCs, also known as electrochemical capacitors or ultracapacitors, are energy storage devices with relatively high specific capacitance, energy, and energy density, which are typically hundreds of times greater than those of conventional electrolytic capacitors. A variety of SC technologies have been developed or still under research and development. Types of SCs are classified by the energy storage mechanism [7]. The most prevalent and traditional SC technologies are electric double-layer capacitors (EDLCs) that store energies in double-layer capacitance formed on both positive and negative electrode. Hybrid capacitors, which are emerging SC technologies, utilize different energy storage mechanisms of double-layer capacitance and electrochemical reaction for respective electrode. Lithium-ion capacitors (LICs) is the most popular hybrid capacitors, and commercialization has been launched by several manufactures. Redox capacitors, also called as pseudo-capacitors, combine simultaneously two kinds of energy storage mechanism, i.e. non-faradic and faradic processes, to even enhance the

value of specific capacitance.

This dissertation deals with EDLCs and LICs as representative SC technologies. However, life testing and prediction model, system mass calculation model, power system components including equalizers, equalization chargers, and UICs, each of which is discussed and developed in the following chapters, can be used for other types of SC technologies.

2.3.1 Electric Double-Layer Capacitor

Generally, a double-layer is formed at the interface between conductive electrode and electrolyte in an electrochemical cell, and provides the effective separation of charge. EDLCs utilize huge double-layer capacitance for energy storage mechanism. Fig. 2.2.1 shows a schematic structure of an EDLC. Since the effective capacitance is proportional to an area of electrodes, activated carbon, which has a high specific area, is typically used for EDLCs. Since both the positive and negative electrodes are the activated carbon, they are also called "symmetric electrochemical capacitors". During charging, positively- and negatively-charged ions adsorb on the negative and positive electrode, respectively, and a terminal voltage increases as the adsorption process progresses. During discharging, on the other hand, the adsorbed ions migrate to the electrolyte, and its terminal voltage decreases. Thus, the charging and discharging processes of EDLCs are essentially adsorption and disorption, and do not involve electrochemical reactions.

The lack of electrochemical reactions provides several major advantages over secondary batteries, such as high power capability, superior cycle life performance, wide operating temperature range, high charge–discharge efficiency, etc. [8],[9]. EDLCs have been used and evaluated for industrial and vehicular applications [10]–[14]. However, since energies are stored only at the surface of electrodes, specific energies of EDLCs are rather lower than those of LIBs, in which electrochemical reactions take place in bulk electrodes. The low specific energy of EDLCs, typically less than 10 Wh/kg for cell, limits their applications to auxiliary energy

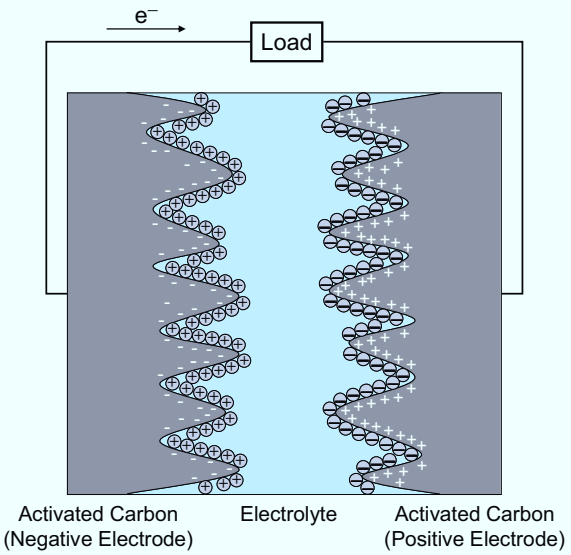


Fig.2.3.1. Image of positive and negative electrode structures of electric double-layer capacitor.

storage sources where EDLCs are used as high-power energy buffers to complement main energy sources such as secondary batteries, fuel cells, and renewable energy systems using photovoltaic (PV) cells and/or wind turbines when there is an instantaneous demand for relatively large power.

Cycle life testing for high-power applications such as industrial and vehicular applications has been performed [10]–[14], and the feasibility of ageing acceleration for EDLCs under floating conditions has also been investigated [15],[16]. However, no study has performed cycle life testing for low-power applications such as energy storage in spacecrafts. Cycle life performance and the feasibility of accelerated ageing tests for EDLCs in spacecrafts will be discussed and investigated in Chapter 3.

2.3.2 Lithium-Ion Capacitor

A LIC is an emerging hybrid capacitor that combines the features of LIBs and EDLCs [17]–[19]. Fig. 2.3.2 shows a schematic structure of a LIC. The positive electrode is identical to that of the EDLCs; the positive electrode is the activated carbon at which a double-layer is developed. On the other hand, negative electrode is a carbon material that is pre-doped with lithium ions, and works like a lithium-ion intercalation electrode used for LIBs. As a result, the capacity of the negative electrode is rather higher than that of the positive electrode, because energies can be stored in the bulk material of the negative electrode. The increased negative electrode capacity also increases the total capacity as a whole cell.

The major advantages of LICs are very similar to those of EDLCs, but a specific energy of LICs, typically less than <30 Wh/kg for cell, is much larger than that of EDLCs. Hence, LICs achieve greater performance than EDLCs without diminishing the advantages of conventional EDLCs [17]–[19]. LICs are known to be much safer than LIBs. Positive active materials of LIBs, which are lithium-oxide alloys, contain an element of oxygen, and the oxygen is released from the positive active material at an elevated temperature causing thermal runaway, which poses serious safety concerns. LICs, on the other hand, do not contain oxygen, and therefore, the thermal runaway mechanism is not likely.

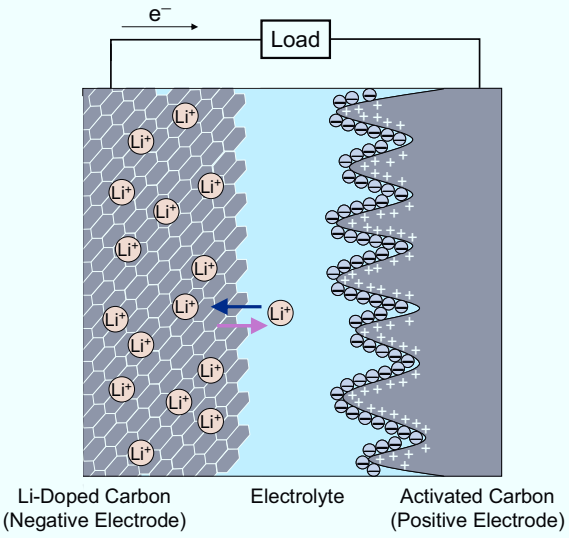


Fig.2.3.2. Image of positive and negative electrode structures of lithium-ion capacitor.

Since the LICs are relatively new in the market, no academic paper has reported life performance and the feasibility of ageing acceleration for LICs as of this writing. These issues will also be discussed in Chapter 3.

2.4 Comparison between Lithium-Ion Battery and Supercapacitors

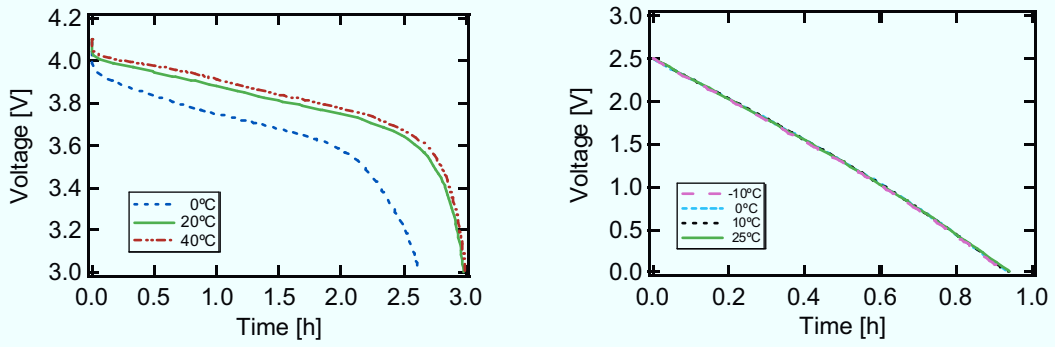
2.4.1 Specific Energy and Cycle Life

LIBs offer the highest specific energy (about 150 Wh/kg for space-qualified cell) among commercial secondary batteries [1]. However, since cycle life performance of LIBs is strongly dependent on depth of discharge (DoD), they are usually cycled with shallow DoD in order to meet cycle life requirements. For example, in low-Earth orbit (LEO) spacecraft applications where more than 30000 charge–discharge cycle life in orbit is required, LIBs are operated with a DoD shallower than 40% to meet the cycle life requirement [3]–[5]. In contrast, for geosynchronous-Earth orbit (GEO) spacecrafts, LIBs are cycled with deep DoD of <80%, because the required cycle number is much less. Thus, only 40% and 80% of the LIBs' specific energy is available during normal operations on LEO and GEO, respectively.

Specific energies of EDLCs and LICs are usually less than 10 Wh/kg and 30 Wh/kg, respectively, and are rather lower than that of LIBs. Their low specific energy has limited their applications to auxiliary energy storage sources. However, they can be potential energy storage sources in spacecraft power systems once their long cycle life at wide temperature range is factored in. If they could operate with deep DoD for desired life spans, the gap between LIBs and SCs in terms of specific energy would be bridged to great extent. Cycle life testing emulating LEO cycling conditions for EDLCs and LICs are performed, and a cycle life prediction model for SCs is established in Chapter 3. Detailed discussion on mass comparison will be made in Chapter 4 by introducing a concept of net specific energy, which is defined as a product of specific energy and DoD.

2.4.2 Operation Temperature

Operation temperature is one of the key factors that govern service life of energy storage cells. It is commonly accepted that calendar degradations of LIBs double for every 10°C increase, and hence, operation temperatures should be low enough to mitigate the temperature-dependent calendar degradations. However, electrical characteristics of LIBs are



(a) (b)

Fig. 2.4.1. Temperature dependence of electrical characteristics of (a) LIB and (b) EDLC cells.

strongly dependent on temperature, as shown in Fig. 2.4.1(a); the deteriorated performance at low temperature is marked. LIBs in spacecraft power systems are commonly operated between 0–10°C (usually specified as 5°C ± 5°C) in order to fulfill the life requirement of 30000 cycles without diminishing electrical characteristics. The temperature range of LIBs is very narrow compared with other components in spacecrafts. This narrow temperature range requires elaborate thermal design and controlling, negatively influencing the thermal system design and operation.

Although calendar degradations of SCs are also dependent on operation temperature, electrical characteristics of SCs are less dependent on operation temperature than those of LICs. Fig. 2.4.1(b) shows the temperature dependence of electrical characteristics of an EDLC cell. In addition, since the life performance of SCs are inherently longer than those of LIBs, the operation temperature range for SCs can be extended compared with those for LIBs. Extended temperature ranges would be beneficial to thermal system design and operation; not only the design flexibility for thermal system is improved but also a required power for heating is likely to be saved. Operation temperatures for SCs to fulfill certain cycle life requirements are estimated based on cycle life testing and life prediction model in Chapter 3.

2.4.3 Voltage Variation During Cycling

Generally, voltages of energy storage devices vary, and a voltage variation range is an important factor to be took into consideration to design not only power conversion electronics, such as bus voltage regulator, charge regulator, and discharge regulator, but also power system architectures. Fig. 2.4.2 compares the discharge curves of LIB, EDLC, and LIC cells at 25°C, and the voltage variation ranges of these cells are usually 3.0–4.2 V, 0–2.5 V, and 2.2–3.8 V, respectively. The discharge curve of the LIB is flat and its voltage variation range is relatively narrow, whereas those of EDLCs and LICs vary significantly. This implies that the conventional LIBs in spacecraft power systems can not be simply replaced with SCs, and power conversion electronics are indispensable to compensate the large voltage variations. For SCs to be used as alternative energy storage sources to LIBs, the voltage range of conventional power conversion electronics must be extended. However, extending the operational voltage range usually poses to some negative problems including increased size and mass of circuit components, reduced

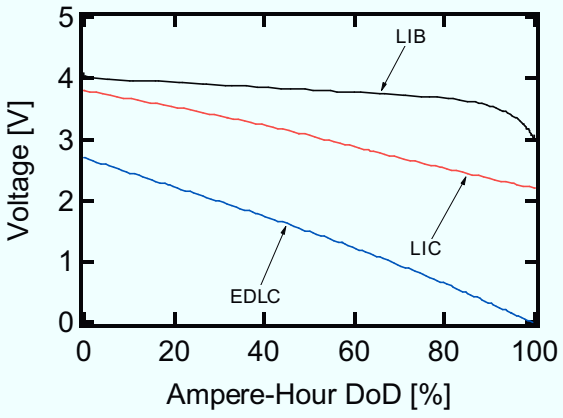


Fig. 2.4.2. Typical discharge curves of LIB, EDLC, and LIC cells.

power conversion efficiency, additional customization, etc. Another approach is an introduction of an unregulated interface converter (UIC) that is a kind of high-efficiency intermediate converter, with which the conventional power conversion electronics can be used without any customizations. In Chapter 7, two types of UICs are proposed for SC-based power systems.

2.5 Power System Architecture for Lithium-Ion Battery and Supercapacitors

2.5.1 Power System Architecture

Since voltage variation ranges of LIBs and SCs are totally different, as shown in Fig. 2.4.2, a power system architecture should be chosen considering the voltage variations so that power system requirements, such as power conversion efficiencies and bus voltage variation ranges, can be properly met with the least compromise. The power system architecture for LIBs and SCs is configured in one of the following systems.

2.5.1.1 Fully Regulated Bus System

A bus voltage in a fully regulated bus is controlled for entire period, and bus voltage variations are typically regulated within several percents. Fig. 2.5.1(a) shows the typical fully regulated bus using a LIB as its energy storage source. During sunlight, in which the PV arrays provide energies to the load and LIB, the bus voltage is regulated by the bus voltage regulator, while the LIB is charged by the charge regulator. In eclipse, the LIB discharges via the discharge regulator, and the power is supplied to the load at a regulated voltage. The fully regulated bus architecture generally finds applications where load power requirements are larger than 3 kW, typically in GEO spacecrafts. Since the bus voltage is regulated to be almost constant, an operational voltage range of dc-dc converters equipped with onboard instruments can be designed relatively narrow, and power distribution harness mass can be reduced compared with other architectures where bus voltages vary. In addition, the fully regulated bus offers great flexibility in battery design and cell selection, because battery voltage as well as the number of series connection can be any values within the charge and discharge regulators' duty cycle limit. Although the power conversion loss in the discharge regulator may be considered as a disadvantage of the fully regulated bus architecture, high-efficiency discharge regulators, which achieve power conversion efficiencies higher than 95%, have been developed [20]–[22],

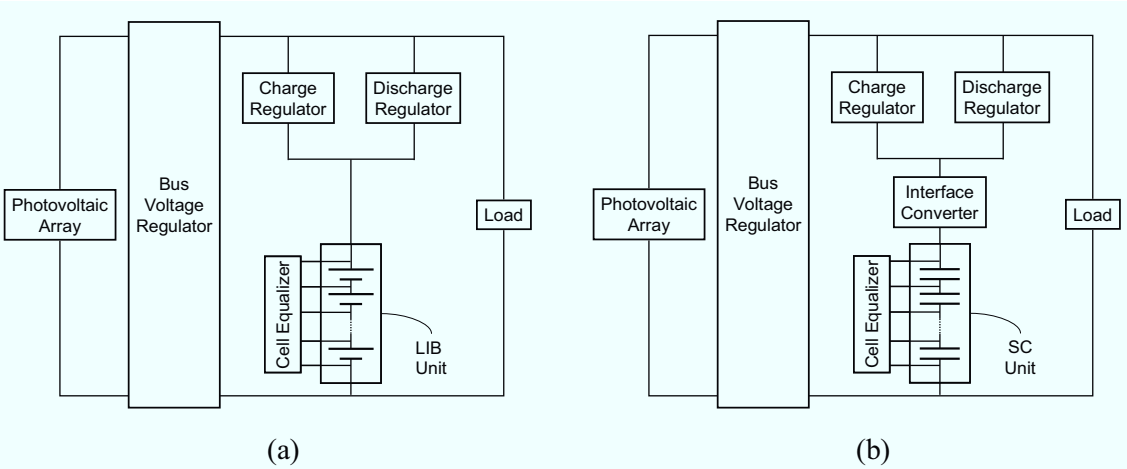


Fig. 2.5.1. Fully regulated bus architectures for (a) LIB-based and (b) SC-based systems.

competing with the discharge diode in sun-regulated bus architectures in terms of power conversion loss. However, the need of the discharge regulator adds cost and reduces the system reliability.

In the fully regulated bus architecture, the SC can be simply replaced with the LIB as long as the voltage variation range of the SC is acceptable to the charge and discharge regulators. If not acceptable, charge and discharge regulators with extended operation voltage range or a UIC are required. Fig. 2.5.1(b) illustrates the SC-based fully regulated bus architecture using a UIC. The charge regulator controls both a charge current and charge voltage for the SC which is placed beyond the UIC. Because of the existence of the UIC in between, charging performance of the charge regulator in terms of stability and accuracy may be negatively affected. In addition, total power conversion efficiencies for both charging and discharging are lower than those in Fig. 2.5.1(a) because of double power conversions in the charge and discharge regulators and the UIC.

2.5.1.2 Sun-Regulated Bus System

In a sun-regulated bus architecture using a LIB, shown in Fig. 2.5.2(a), the bus voltage is regulated by the bus voltage regulator during sunlight, and is unregulated during eclipse because of the LIB directly connected to the bus via the discharge diode. The advantage of this architecture over the fully regulated bus is the lack of the discharge regulator, reducing cost as well as the system complexity. The sun-regulated bus architectures usually find applications having the load power demand less than a few kilowatts, typically in LEO spacecrafts. However, since the LIB is directly connected to the bus without a discharge regulator in between, the bus voltage during eclipse varies as the LIB discharges. A typical variation range of a 28-V bus, for example, is 22–35 V, which is determined by the number of series connection of cells and cell voltage variation range, and therefore, dc-dc converters equipped with onboard instruments must be designed operational in that range.

Since voltages of SCs vary significantly, as shown in Fig. 2.4.2, the LIB can not be simply replaced with an SC without additional power conversion electronics. For SCs to be used in a sun-regulated bus architecture, the SC must supply the power to the load within a desired voltage range, which is typically 22–35 V for a 28-V bus system. Possible sun-regulated bus architectures for SCs are shown in Figs. 2.5.2(b) and (c). In the system illustrated in Fig. 2.5.2(b), the combination of the SC and a UIC is replaced with the LIB in Fig. 2.5.2(a). In other words, the SC with the UIC behaves as if an alternative LIB. Although a power conversion efficiency of the UIC can be very high as demonstrated in Chapter 7, a total power conversion efficiency for charging is expected to be lower than that in the conventional single power conversion system shown in Fig. 2.5.2(a) because of an efficiency penalty due to the double power conversion in the charger regulator and the UIC. Another possible architecture, shown in Fig. 2.5.2(c), has the UIC instead of the discharge diode. In this system, the UIC operates during eclipse (discharging period) only, and the charge power for the SC passes through the charge regulator only, reducing the number of the power conversion stage for charging compared with the system shown in Fig. 2.5.2(b). This system is very similar to the fully regulated bus architecture shown in Fig. 2.5.1(a), but the bus voltage during eclipse is unregulated. In addition to the improved power conversion efficiency for charging, the discharge diode can be

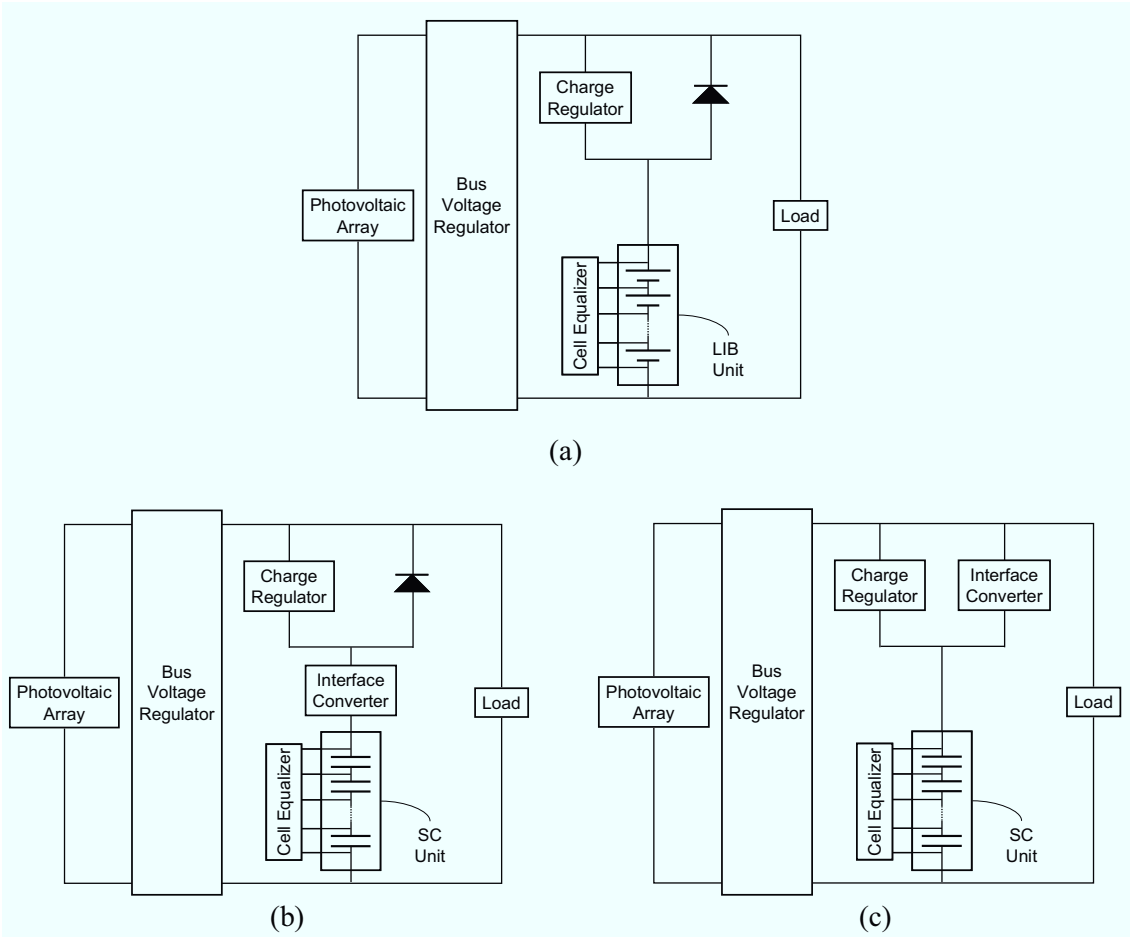


Fig. 2.5.2. Sun-regulated bus architectures for (a) LIB-based system and SC-based systems using unregulated interface converter (b) with discharge diode and (c) without discharge diode.

eliminated, and hence, this system is considered advantageous over the system in Fig. 2.5.2(b). From the viewpoint of charge performance of the charge regulator, the system in Fig. 2.5.2(c) is also better because of the UIC is not connected between the charge regulator and the SC. However, the charge regulator in Fig. 2.5.2(c) needs to be designed capable of the large voltage variation of the SCs, whereas conventional charge regulator without any retrofit can be used in Fig. 2.5.2(b).

2.5.1.3 Unregulated Bus System

The simplest power system architecture for a LIB is an unregulated bus system, shown in Fig. 2.5.3(a), which has neither charge regulator nor discharge regulator. Since the LIB is directly tied to the bus without any series component in between, the bus voltage is always unregulated and as same as the LIB's voltage. A charge current and charge voltage for the LIB are controlled by the bus voltage regulator, and hence, the bus voltage regulator in this system acts as a charge regulator. Although the simplest architecture, the charge control function needs to be incorporated into the bus voltage regulator. The unregulated bus architecture has the similar advantages and disadvantages of the sun-regulated bus architecture, discussed in the previous section. However, the bus voltage regulator in the unregulated bus system requires the largest

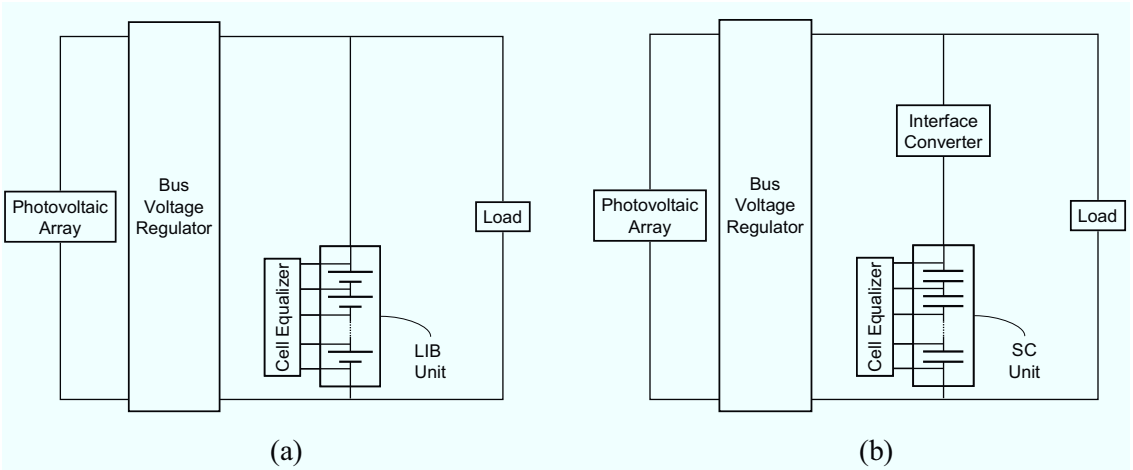


Fig. 2.5.3. Unregulated bus architectures for (a) LIB-based and (b) SC-based systems.

operational voltage range among the power system architectures discussed in this section. The input and output of the bus voltage regulator in the unregulated bus system are connected to the PV array and the LIB, respectively, whose voltages vary depending on conditions. Hence, the bus voltage regulator must be designed considering the severest condition in terms of duty cycle and voltage stress, which is likely to occur at the beginning of sunlight when the PV array's voltage and the LIB's voltage are the highest and lowest, respectively.

For SCs to be used instead of the LIB, a UIC is required in the unregulated bus system, as illustrated in Fig. 2.5.3(b). One concern is that the charge performance of the bus voltage regulator, in terms of stability and accuracy, may be negatively affected by the existence of the UIC connected in between, as explained in the previous sections.

2.5.2 Energy Transfer from Photovoltaic Array to Bus

The above-explained bus architectures are further subdivided into two groups, depending on the type of the bus voltage regulator.

2.5.2.1 Direct Energy Transfer

In a direct energy transfer (DET) system, the PV array and the load are connected with no series components in between. Shunt dissipators are usually used for DET systems, and regulate or roughly control the bus voltage within a desired variation range. Generally, PV arrays are sized to be capable to meet the power requirement at the end of mission life, and a generated power of the PV arrays should be delivered to the bus with minimum power loss in order to size the PV arrays as small as possible. Since there is no series component between the PV array and the bus, all the generated PV power at the end of life can be delivered to the bus with no loss in the ideal case. However, the excess power of the PV arrays is dissipated in the form of heat in order to control the bus voltage, and hence, the thermal system of spacecrafts must be designed to provide adequate cooling.

A variety of shunt dissipators, including linear and PWM shunts, have been developed, used, demonstrated, and proposed to reduce the burden on the thermal system. Other efforts have been made to combine the charge regulator with the shunt dissipator in order to reduce the number of

power system components as well as the system complexity and cost [23],[24].

2.5.2.2 Series Switching Regulator

Series switching regulators (SSRs) are switching dc-dc converters that control the voltage conversion ratio between the PV arrays and the bus. Contrary to the DET systems, since only a required power is extracted from the PV arrays by the SSR, the heat dissipation can be significantly reduced compared with that in the DET systems. However, heat due to power conversion losses in the SSRs needs to be dissipated inside the spacecraft body, negatively influencing the thermal system. Besides, the PV arrays in SSR systems should be sized larger than those in the DET systems in order to compensate a power conversion loss in the SSRs. Another concern is bus voltage ripples induced by high-frequency switching operations of the SSRs.

The SSRs can operate as maximum power point tracker (MPPT), with which the PV arrays are always able to operate at the maximum power point. The MPPT finds a variety of applications having relatively short sunlight period or large variations in solar flux, array temperature, and sun angle in spacecrafts with no sun tracking gimbals. The SSRs also can be combined with the charge regulator in the unregulated systems, as already discussed in Section 2.5.1.3.

References

[1] H. Yoshida, N. Imamura, T. Inoue, K. Takeda, and H. Naito, “Verification of life estimation model for space lithium-ion cells,” *Electrochemistry*, Vol. 78, No. 5, pp. 482–488, 2010.

[2] X. Wang, Y. Sone, and S. Kuwajima, “Effect of operation conditions on simulated low-Earth orbit cycle-life testing of commercial lithium-ion polymer cells,” *J. Power Sources*, Vol. 142, No. 1–2, pp. 313–322, Mar. 2005.

[3] X. Wang, Y. Sone, H. Naito, C. Yamada, G. Segami, and K. Kibe, “Cycle-life testing of 100-Ah class lithium-ion battery in a simulated geosynchronous-Earth-orbit satellite operation,” *J. Power Sources*, Vol. 160, pp. 602–608, Sep. 2006.

[4] X. Wang, Y. Sone, H. Naito, C. Yamada, G. Segami, and K. Kibe, “Cycle-life testing of large-capacity lithium-ion cells in simulated satellite operation,” *J. Power Sources*, Vol. 161, pp. 594–600, Oct. 2006.

[5] B. V. Ratnakumar, M. C. Smart, C. K. Huang, D. Perrone, S. Surampudi, and S. G. Greenbaum, “Lithium-ion batteries for Mars exploration missions,” *Electrochemica Acta*, Vol. 45, pp. 1513–1517, Jan. 2000.

[6] M. Uno, K. Ogawa, Y. Takeda, Y. Sone, K. Tanaka, M. Mita, and H. Saito, “Development and on-orbit operation of lithium-ion pouch battery for small scientific satellite "REIMEI",” *J. Power Sources*, Vol. 196, No. 20, pp. 8755–8763, Oct. 2011.

[7] M. Jayalakshmi and B. Balasubramanian, “Simple capacitors to supercapacitors -an overview,” *Int. J. Electrochem. Sci.*, Vol. 3, pp. 1196–1217, 2008.

[8] Bohlen, J. Kowal, and D. U. Sauer, “Ageing behavior of electrochemical double layer capacitors part II. Lifetime simulated model for dynamic applications,” *J. Power Sources*, Vol. 173, pp. 626–632, Nov. 2007.

[9] R. Lu, C. Zhu, L. Tian, and Q. Wang, "Modeling the dynamic behavior of supercapacitors using impedance spectroscopy," *IEEE Transaction on Industry Applications*, Vol. 38, No. 6, pp. 1622–1626, Dec. 2002.

[10] N. Rizoug, P. Bartholomeus, and P. L. Moigne, "Modeling and characterizing supercapacitors using an online method," *IEEE Transactions on Industrial. Electronics*, Vol. 57, No. 12, pp. 3980–3990, Feb. 2010.

[11] Hammar, P. Venet, R. Lallemand, G. Coquery, and G. Rojat, "Study of accelerated aging of supercapacitors for transport applications," *IEEE Transactions on Industrial Electronics*, Vol. 57, No. 12, 3972–3979, Apr. 2010.

[12] E. H. E. Brouji, O. Briat, J. M. Vinassa, N. Bertrand, and E. Woirgard, "Impact of calendar life and cycling ageing on supercapacitor performance," *IEEE Transactions on Vehicular Technology*, Vol. 58, No. 8, pp. 3917–3929, Jul. 2009.

[13] Briat, J. M. Vinassa, N. Bertrand, H. El Brouji, J. Y. Deletage, and E. Woirgard, "Contribution of calendar ageing modes in the performances degradation of supercapacitors during power cycling," *Microelectronics Reliability*, Vol. 50, No. 9–11, pp. 1796–1803, Sep./Nov. 2010.

[14] H. El Brouji, O. Briat, J. M. Vinassa, N. Bertrand, and E. Woirgard, "Comparison between changes of ultracapacitors model parameters during calendar life and power cycling ageing tests," *Microelectronics Reliability*, Vol. 48, No. 8–9, pp. 1473–1478, Aug./Sep. 2008.

[15] T. Umemura, Y. Mizutani, T. Okamoto, T. Taguchi, K. Nakajima, and K. Tanaka, "Life expectancy and degradation behavior of electric double layer capacitor Part I," in *Proc. the 7th Int. Conf. Properties and Appl. of Dielectric Materials*, Vol. 3, pp. 944–948, Jun. 2003.

[16] R. Kötz, P. W. Ruch, and D. Cericola, "Aging and failure mode of electrochemical double layer capacitors during accelerated constant load tests," *J. Power Sources*, Vol. 195, No. 3, pp. 923–928, Feb. 2010.

[17] S. M. Lambert, V. Pickert, J. Holden, X. He, and W. Li, "Comparison of supercapacitor and lithium-ion capacitor technologies for power electronics applications," in *Proc. Power and Electronics Machines and Drives*, pp. 19–21, 2010.

[18] N. Böckenfeld, R. S. Kühnel, S. Passerini, M. Winter, and A. Balducci, "Composite $LiFePO_4$/AC high rate performance electrodes for Li-ion capacitors," *J. Power Sources*, Vol. 196, pp. 4136–4142, Apr. 2011.

[19] H. Gualous, G. Alcicek, Y. Diab, A. Hammar, P. Venet, K. Admas, M. Akiyama, and C. Marumo, "Lithium ion capacitor characterization and modeling," *ESSCAP'2008*, 2008.

[20] E. Sanchis, E. Maset, A. Ferreres, J. B. Ejea, V. Esteve, J. Jordan, A. Garrigos, and J. M. Blanes, "High-Power Battery Discharge Regulator for Space Applications," *IEEE Transactions on Industry Applications*, Vol. 57, No. 12, pp. 3935–3943, Dec. 2010.

[21] E. Maset, J. B. Ejea, A. Ferreres, A. Ferreres, E. S. Kilders, J. Jordan and V. Esteve, "High-Efficiency Weinberg Converter for Battery Discharging in Aerospace Applications," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, pp. 1510–1516, Mar. 2006.

[22] L. Soubrier, P. Besdel, T. Daubresse, and E. Trehet, "High Performance BDR for the PCU of Alphabus," in *Proc. 8th European Space Power Conference*, Sep. 2008.

[23] A. Capel and P. Perol, “Comparative Performance Evaluation between the S4R and the S3R Regulated Bus Topologies,” in *Proc. IEEE 32nd Power Electronics Specialist Conference*, pp. 1963–1969, Jun. 2001.

[24] A. Garrigos, J. A. Carrasco, J. M. Blanes, and E. S. Kilders, “A New Sequential Switching Shunt Regulator ―Digital Shunt Regulator (S3R-DSR) for Solar Array Regulators,” in *Proc. IEEE International Symposium on Industry Electronics*, pp. 1064–1069, Jul. 2006.

Chapter 3
Cycle Life Evaluation for Supercapacitors

3.1 Introduction

Cycle life performance of EDLCs has been evaluated for industrial and vehicular applications [1]–[5], whereas no academic papers have reported life performance of LICs as of this writing. Ageing acceleration and cycle life prediction are of primary importance because testing for actual lifespan, which may be more than 10 years, is impractical in laboratories. The ageing of EDLCs can be accelerated by elevating the temperature on the basis of the Arrhenius model, which expresses chemical reaction rate as a function of temperature [6]–[8]. Conventional accelerated ageing tests are performed under float conditions with constant voltage and temperature [8]–[10]; therefore, the influence of charge–discharge cycling on the life performance is not considered. Previous research on high-power charge–discharge cycle life testing reported that ageing behavior during high-power cycling differs from that during float conditions [3]–[5]. In addition, because the charge–discharge current for such high-power cycling is very large, the temperatures of EDLCs tend to increase because of Joule heating in resistive components [11],[12]; this heat generation strongly influences cycle life performance [13]. Ageing during low-power cycling aiming for alternative battery applications, in which heat generation is negligibly low because of low charge–discharge current, is considered to be different from that during high-power cycling.

In this chapter, the feasibility of accelerated cycle life testing for SCs (i.e., EDLCs and LICs) is discussed, and a cycle life prediction model is established. In Section 3.3, cycle life performance of EDLCs and LICs at various temperatures and DoDs is evaluated. Section 3.4 discusses temperature dependence of degradations based on the resultant cycle life performance and Arrhenius equation. Activation energies and acceleration factor, which are the major parameters for the life prediction model, are mathematically determined. In Section 3.5, a cycle life prediction model considering temperature and number of cycles is established, and examples of cycle life prediction on the basis of the established model are also presented.

3.2 Experimental Conditions

3.2.1 Charging and Discharging Schemes During Cycling

Constant current–constant voltage (CC–CV) charging and constant current (CC) discharging are the most common schemes for LIB cycle life performance tests. For practical use, LIBs are charged by a charger that usually adopts the CC–CV charging scheme. Because this charging scheme is determined by chargers, EDLCs and LICs may also be charged in a similar manner even when LIBs are replaced with EDLCs or LICs.

On the other hand, a discharging scheme for EDLCs and LICs should differ from that for LIBs in cycle life testing. LIBs in practical use discharge to loads via dc–dc converters that

supply power to the loads at a regulated constant voltage, thus discharging LIBs at constant power (CP). In other words, the converter viewed from the LIBs acts as a CP load. A discharge curve of a LIB, shown in Fig. 2.4.2 in the previous chapter, is relatively flat at DoD smaller than approximately 80%, and therefore, LIBs discharge at almost CC even for the CP loads in practical usage although their currents slightly vary. Thus, cycle life testing using a CC discharging scheme is reasonable for LIBs although actual cycling profiles are anticipated to be more complicated than those in laboratories. On the other hand, voltages of EDLCs and LICs vary significantly with change of DoD as compared with that of LIBs. Thus, the discharge current of SCs for the CP loads increases with a decrease in their voltage. This inherent trait makes the CP discharging scheme preferable for cycle life testing.

3.2.2 Depth of Discharge

It is well known that LIBs deteriorate significantly with deeper DoD [14],[15]. Therefore, DoD is one of the most important parameters for cycle life testing of LIBs. DoD is usually defined as the ratio of the discharged capacity to the rated capacity, and LIBs are cycled using CC discharging, with which the discharged capacity is invariably constant in every charge–discharge cycle. On the other hand, the discharged capacity for cycling using CP discharging varies with voltage decline due to ageing, whereas the discharged energy is invariably constant in every charge–discharge cycle. In this study, energy DoD, which is the ratio of the discharged energy to the rated energy, was defined for standardization throughout the cycle life testing using the CP discharging scheme. Ampere-hour DoD, D_{Ah}, and energy DoD, D_E, are given by

$$D_{Ah} = \frac{V_{cha} - V_{EoD}}{V_R - V_{cut-off}}, \tag{3.1}$$

$$D_E = \frac{V_{cha}^{\ 2} - V_{EoD}^{\ 2}}{V_R^{\ 2} - V_{cut-off}^{\ 2}}, \tag{3.2}$$

respectively, where V_R, V_{cha}, $V_{cut\text{-}off}$, and V_{EoD} are the rated charge voltage (or maximum charge voltage), charge voltage, cut-off voltage, and end of discharge voltage, respectively. The relationship between D_{Ah} and D_E for SCs is obtained from (3.1) and (3.2) as

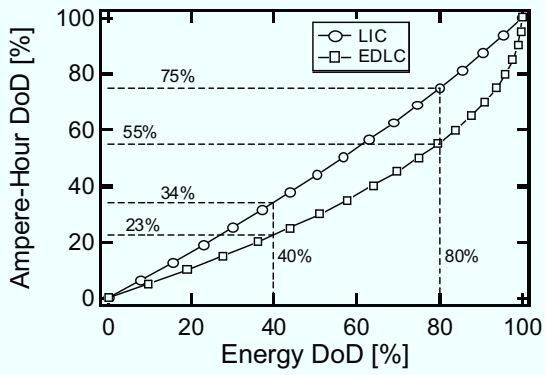


Fig. 3.2.1. Relationship between ampere-hour DoD and energy DoD.

Table 3.1. Charge-discharge cycling conditions for SCs.

Cell	DoD (D_E)	Charge Voltage (V_{cha})		Temperature
		EDLC	LIC	
1	80%	2.5 V	3.8 V	40°C
2	40%	2.3 V	3.6V	
3				
4	80%	2.5 V	3.8 V	0°C
5	40%	2.3 V	3.6V	
6				
7	80%	2.5 V	3.8 V	30°C (EDLC) 25° C (LIC)
8	40%	2.3 V	3.6V	
9				
10	CV	2.5 V (for 500 F cells only)	n/a	40°C
11			n/a	0°C
12			n/a	30°C

$$D_E = \frac{V_{cha}^{\ 2} - \left\{V_{cha} - D_{Ah}\left(V_R - V_{cut-off}\right)\right\}^2}{V_R^{\ 2} - V_{cut-off}^{\ 2}}. \tag{3.3}$$

The relationship between D_{Ah} and D_E for an EDLC ($V_R = V_{cha} = 2.5$ V, $V_{cut\text{-}off} = 0$ V) and LIC ($V_R = V_{cha} = 3.8$ V, $V_{cut\text{-}off} = 2.2$ V) are shown in Fig. 3.2.1.

3.2.3 Charge-Discharge Cycling Conditions

EDLCs (1500 F or 500 F, V_R = 2.5 V) and LICs (2000 F-class, V_R = 3.8 V), whose photographs are shown in Fig. 3.2.2, were used for the cycle life testing. Nine cells, Cells 1–9, were cycled at various conditions, and three cells of 500-F-EDLC were tested at floating conditions, as shown in Tables 3.1 where there are 2 levels of DoD (D_E), 2 levels of charge voltage (V_{cha}), and 3 levels of temperature in order to systematically investigate cycle life performance. For comparison, lithium-ion pouch cells with capacity of 3.0 Ah were also cycled with D_{Ah} = 20% or 40% at 25°C.

As explained in the previous section, DoD is one of the most important parameters for cycle life testing. In order to investigate DoD dependence on SC degradation, the SCs were cycled with two D_E levels. A deep DoD level of D_E = 80%, which allows 20% degradation at the end of

(a) (b)

Fig. 3.2.2. Photograph of (a) 1500-F and 500-F-EDLCs, and (b) 2000-F-class LIC.

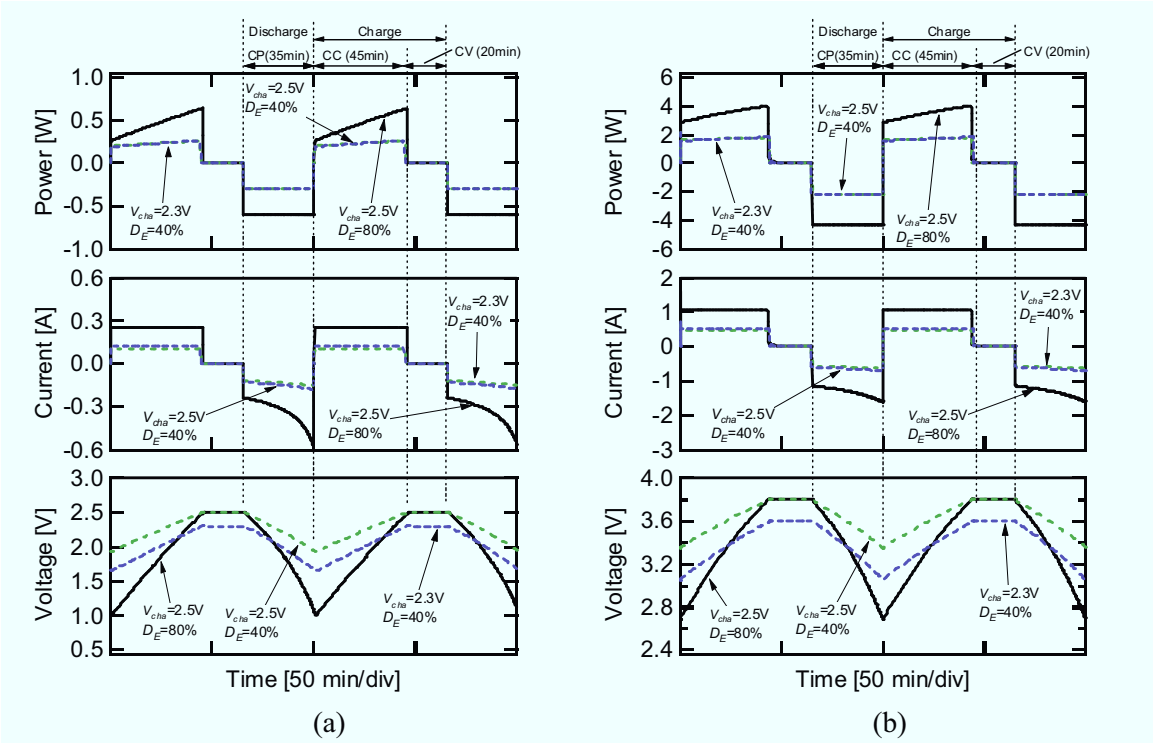


Fig. 3.2.3. Typical cycling profiles for (a) 1500-F-EDLCs and (b) LICs.

life, was a baseline condition. On the other hand, a shallow DoD of D_E = 40% was for comparison.

Degradations of SCs under floating conditions are accelerated with an increase in charge voltage, and 100 mV increase reportedly corresponds to 10°C increase [7],[10],[16],[17]. However, an influence of charge voltage during cycling on degradations of SC for alternative battery applications has not been reported. To investigate an impact of charge voltage during cycling on degradations, cells were tested at 2 charge voltage levels.

A typical operation temperature range for low-Earth-orbit spacecraft is specified to be −5°C–30°C [18], but temperatures rarely fall below 0°C in practical use. The cells were tested at 0°C and 30°C, which are in the typical operation temperature range, as well as at 40°C, at which ageing is expected to be accelerated compared with the typical temperature range.

A single charge–discharge cycle consisted of 65 min charging and 35 min discharging, emulating typical charge–discharge cycling for low-Earth-orbit spacecraft [19],[20]. Cells were charged with the CC–CV charging scheme and discharged with CP discharging. The values of charge current during the CC charging period were determined so that the CC and CV charging periods were 45 and 20 min, respectively, at the beginning of cycle life testing. The current for CC charging, I_{CC}, is determined as

$$I_{CC} = \frac{C\left(V_{cha} - V_{EoD}\right)}{T_{CC}}, \tag{3.4}$$

where C is the capacitance and T_{CC} is the CC charging period in second. The power for discharging, P_{dis}, is given by

$$P_{dis} = \frac{\frac{1}{2} C V_R^{\,2} D_E}{T_{dis}}, \tag{3.5}$$

where T_{dis} is discharging period in second. Fig. 3.2.3(a) and (b) shows typical profiles of voltage, current, and power during charge–discharge cycling for 1500-F-EDLCs and LICs, respectively.

The capacitance retentions were periodically measured at 25°C. The capacitance measurement was performed with the CC–CV charging scheme at 1.0 C rate for 5 h, followed by CC discharging at 1.0 C rate. The capacitance retention ratio is the ratio of the measured capacitance at each cycle to the initial capacitance.

3.3 Experimental Cycle Life Performance

Figs. 3.3.1(a)–(c) show the typical discharge curve trend of a lithium-ion cell, 1500-F-EDLC, and LIC during capacitance measurement. The discharging time of the lithium-ion cell consistently decreased because of degradation, and the voltage decline at the beginning of discharging became significant with the number of cycles, indicating a significant increase in cell impedance. In contrast to the lithium-ion cell shown in Fig. 3.3.1(a), the discharge curves of the EDLC and LIC, shown in Figs. 3.3.1(b) and (c), respectively, did not change significantly with the number of cycles, indicating that the degradations due to cycling were rather smaller

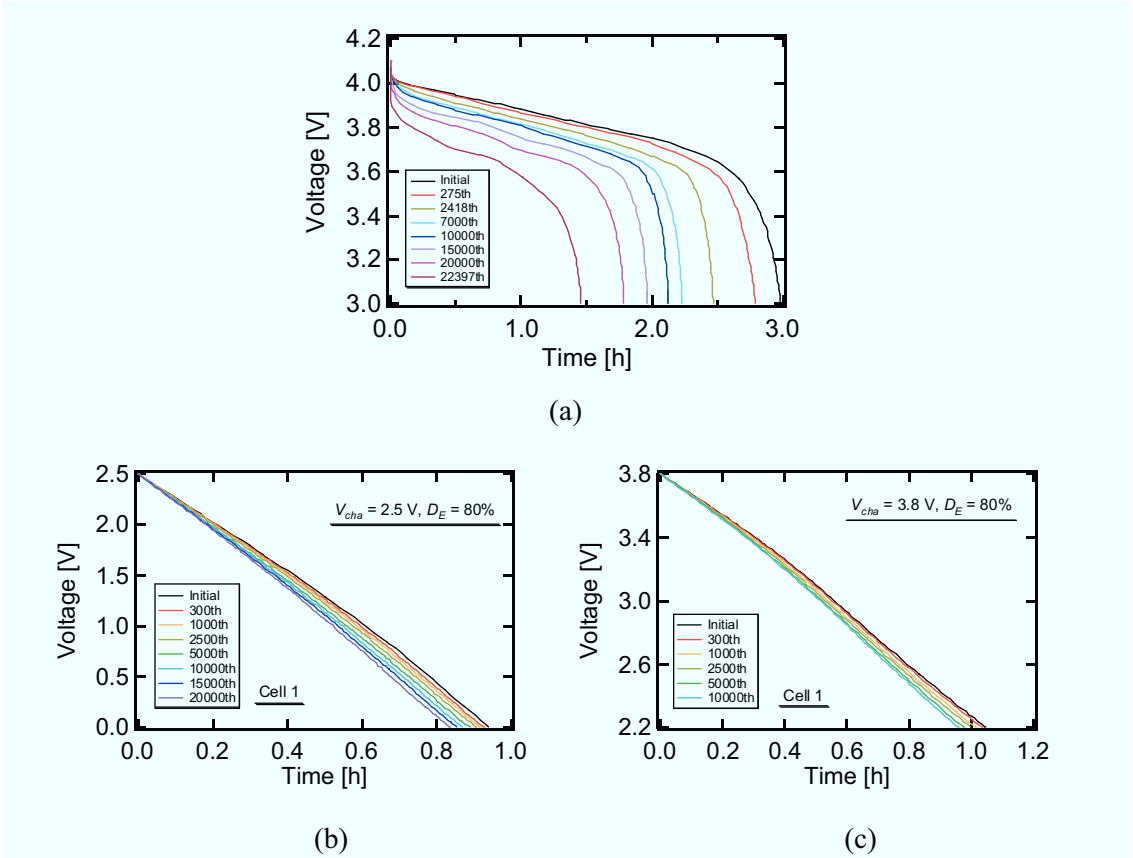
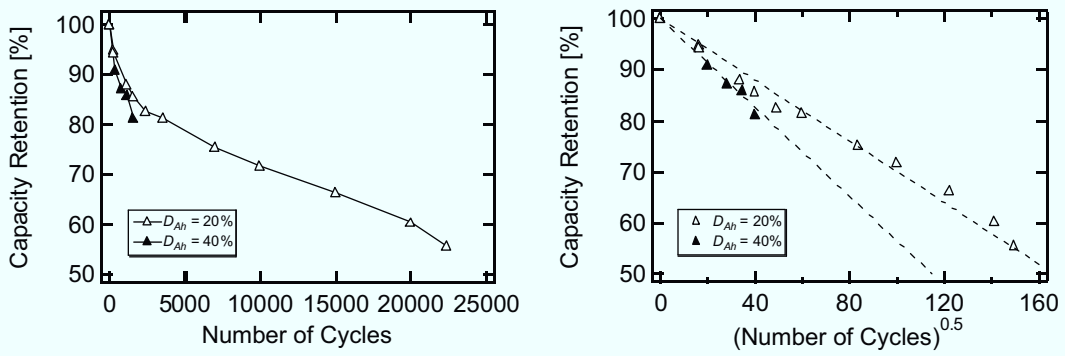


Fig. 3.3.1. Typical discharge curve trend of (a) lithium-ion cell, (b) EDLC, and (c) LIC during capacitance/capacity measurement.

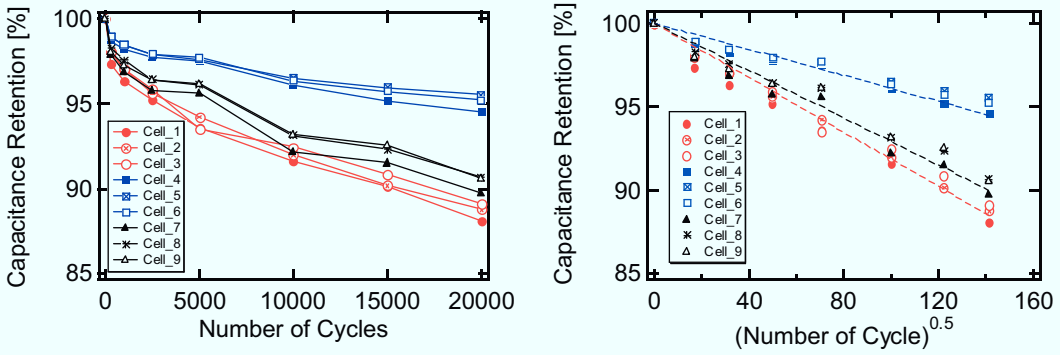


(a) (b)

Fig. 3.3.2. Capacitance retention trends of lithium-ion cells as a function of (a) number of cycles and (b) square root of number of cycles.

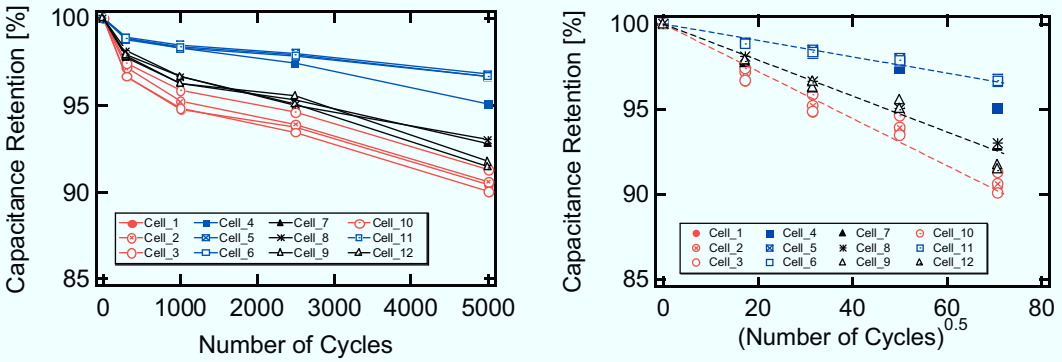
than that of the lithium-ion cell.

Capacitance/capacity retention trends of lithium-ion cells, 1500-F- and 500-F-EDLCs, and LICs as a function of number of cycles are shown in Figs. 3.3.2(a)–3.3.5(a), respectively. The lithium-ion cell at the deep DoD condition (i.e., D_{Ah} = 40%) exhibited greater degradation than that at the shallow DoD (D_{Ah} = 20%), as similar trends have been reported in the literature [21]–[23]. The capacity retention of the cell at D_{Ah} = 20% decreased to approximately 80% at 5000th cycle. On the other hand, all the capacitance retentions of EDLCs and LICs were higher than 90% at the 5000th cycle or approximately 0.95 years, demonstrating superior cycle life performances. The degradations of EDLCs and LICs cycled with the higher charge voltage level (V_{cha} = 2.5 V and 3.8 V for EDLCs and LICs, respectively) and D_E = 80% (Cells 1, 4, and 7) were slightly severer than the others. However, the resultant retention trends were almost independent on cycle conditions although the capacitance fade during float conditions is reportedly accelerated with an increase in charge voltage (V_{cha}) [7],[10],[16],[17]. On the other hand, temperature dependence of the capacitance retention trends was explicit; higher temperatures resulted in significant capacitance fade. This temperature-dependent trend occurs because electrolyte and impurity decomposition rates accelerate at higher temperatures [8],[9],



(a) (b)

Fig. 3.3.3. Capacitance retention trends of 1500-F-EDLCs as a function of (a) number of cycles and (b) square root of number of cycles.



(a) (b)

Fig. 3.3.4. Capacitance retention trends of 500-F-EDLCs as a function of (a) number of cycles and (b) square root of number of cycles.

and the decomposition product, which might reduce accessibility of porous electrodes, consequently reduces effective capacitance [3],[5]. The measured temperatures of EDLCs and LICs during cycle life testing were the same as the ambient temperatures, indicating that temperature increase due to Joule heating in internal resistance was small enough.

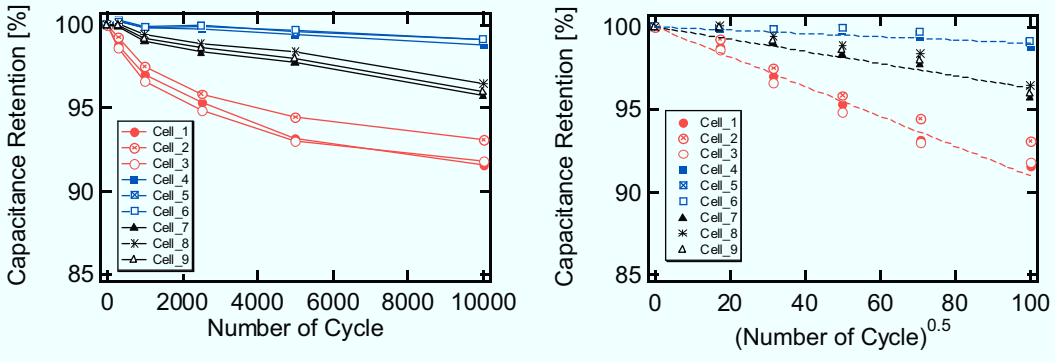
Figs. 3.3.2(b)–3.3.5(b) redraw the capacitance retention trends of lithium-ion cells, EDLCs, and LICs as a function of the square root of the number of cycles. It is empirically accepted that the retention trends of LIBs can be linearly extrapolated using the square root of the number of cycles or testing time as the x-axis [19],[24],[25]. In such a manner, the retention trends can be extrapolated linearly by using

$$C_T = 100 - d_T\sqrt{N}\,, \tag{3.6}$$

where C_T and d_T are the capacitance retention and degradation rate constant at temperature T, respectively, and N is the number of cycles. The degradation ratio at N cycle and temperature T, D_T, is given by

$$D_T = d_T\sqrt{N}\,. \tag{3.7}$$

Experimental retentions and extrapolation curves agreed well for all temperature conditions,



(a) (b)

Fig. 3.3.5. Capacitance retention trends of LICs as a function of (a) number of cycles and (b) square root of number of cycles.

indicating that the extrapolation using (3.6) can be used to predict cycle life performance of EDLCs and LICs at a given temperature for alternative battery applications.

3.4 Temperature Dependence of Capacitance Retention

3.4.1 Arrhenius Equation and Activation Energy

In accelerated stress tests for electrolytic capacitors and semiconductor devices, an Arrhenius model is generally used to express temperature dependency of life. The calendar degradation rates of the secondary batteries under the float conditions can also be expressed by the Arrhenius equation [24], in which the rate of a chemical reaction, K, is given by

$$K = A\,exp\left(\frac{-E_a}{RT}\right), \tag{3.8}$$

where A, E_a, R, and T are the constant, activation energy, gas constant, and temperature in Kelvin, respectively. The Arrhenius equation suggests that higher temperatures result in more rapid chemical reactions. Because the degradations of EDLCs and LICs are considered to be due to chemical reactions [9], the degradation ratio, D_T, which is proportional to the degradation reaction rate, is given by

$$D_T = bK\,, \tag{3.9}$$

where b is the constant. From (3.8) and (3.9),

$$D_T = A_D\,exp\left(\frac{-E_a}{RT}\right), \tag{3.10}$$

where

$$A_D = bA\,. \tag{3.11}$$

Equation (3.10) can be rewritten as

$$ln\,D_T = \frac{-E_a}{1000R}\frac{1000}{T} + ln\,A_D\,, \tag{3.12}$$

or

$$log\,D_T = \frac{1}{2.303}\frac{-E_a}{1000R}\frac{1000}{T} + log\,A_D\,. \tag{3.13}$$

These equations verify that the relationship between logarithmic D_T and inverse of T is indicated by a linear line having a slope of $-E_a$ as long as the degradation mechanism in a particular temperature range is homogeneous and governed by the Arrhenius model.

3.4.2 Acceleration Factor

The acceleration factor for every 10°C increase, α, is defined as

$$\alpha = \sqrt[\left(\frac{T-T_{ref}}{10}\right)]{\frac{D_T}{D_{Tref}}}\,, \tag{3.14}$$

where D_{Tref} is the degradation ratio at the reference temperature, T_{ref}. From (3.10) and (3.14), α can be rewritten as

$$\alpha = \left(\frac{T-T_{ref}}{10}\right)\sqrt{exp\left\{\frac{E_a}{R}\left(\frac{1}{T_{ref}}-\frac{1}{T}\right)\right\}}. \qquad (3.15)$$

3.4.2 Determination of Activation Energy and Acceleration Factor

Fig. 3.4.1 shows representative resultant Arrhenius plot trends of 1500-F- and 500-F-EDLCs and LICs. The results showed good linearity for both EDLCs and LICs in all conditions, implying that the degradation rate was dominated by the ambient temperature during LEO-emulated cyclings in which the cell temperatures were almost equal to the ambient temperatures because of negligible heat generated during cycling. Because the degradation trends are well expressed by the Arrhenius equation, degradations can be accelerated by elevating the temperatures. The slopes in the Arrhenius plots shown in Fig. 3.4.1 did not change significantly with the number of cycles. This indicates that each degradation mechanism of EDLCs and LICs in the experimental temperature range (0–40°C) was homogeneous throughout the entire testing period.

As expressed by (3.12) or (3.13), the slope in Arrhenius plot is equal to $-E_a$; E_a of degradation at each cycling condition was determined from the Arrhenius plots. Fig. 3.4.2 shows the trends of E_a for degradation. The determined E_a of 1500-F- and 500-F-EDLCs and

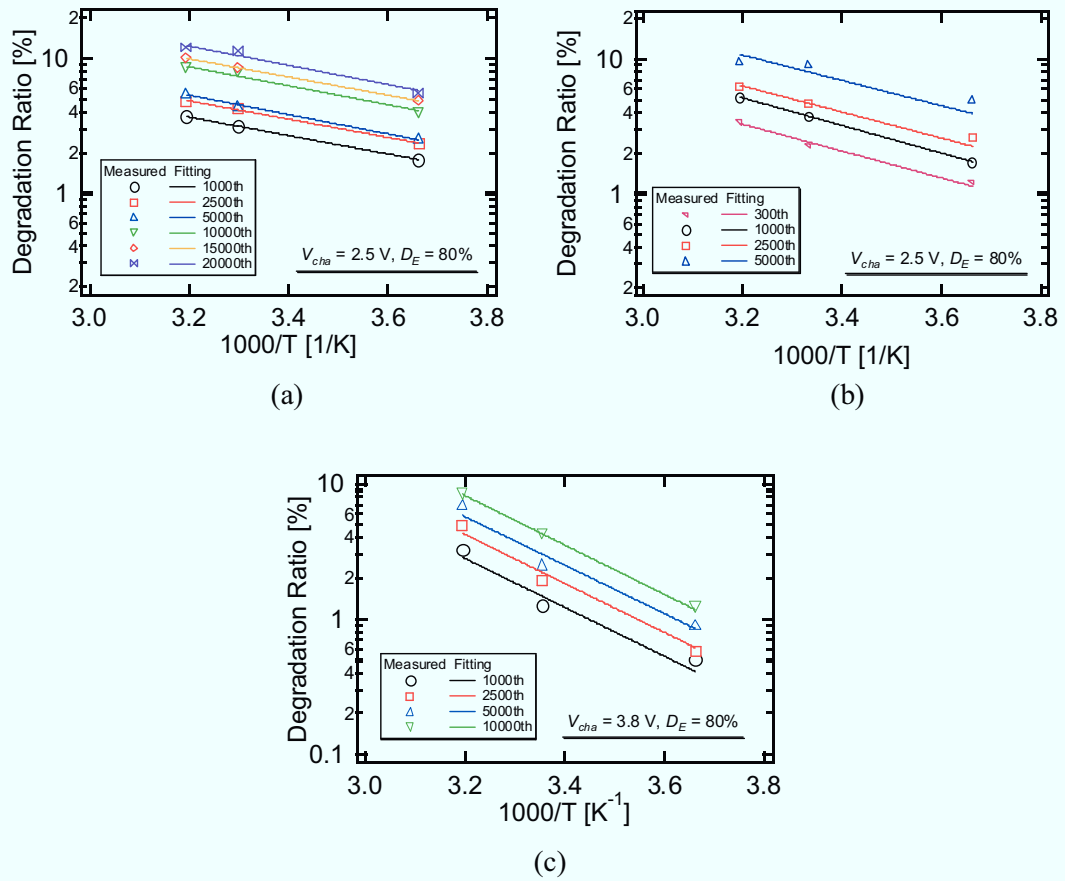


Fig. 3.4.1. Arrhenius plot trends of (a) 1500-F- and (b) 500-F-EDLCs cycled at V_{cha} = 2.5 V D_E = 80%, and LICs cycle at V_{cha} = 3.8 V D_E = 80%.

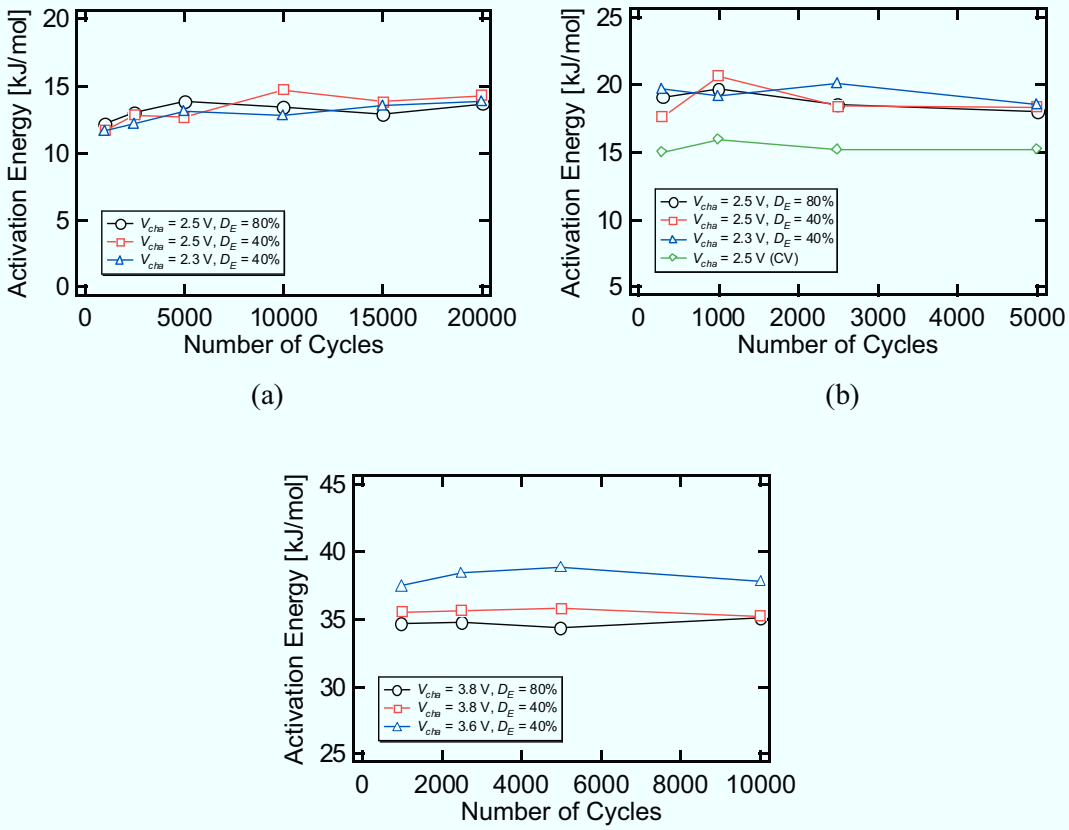
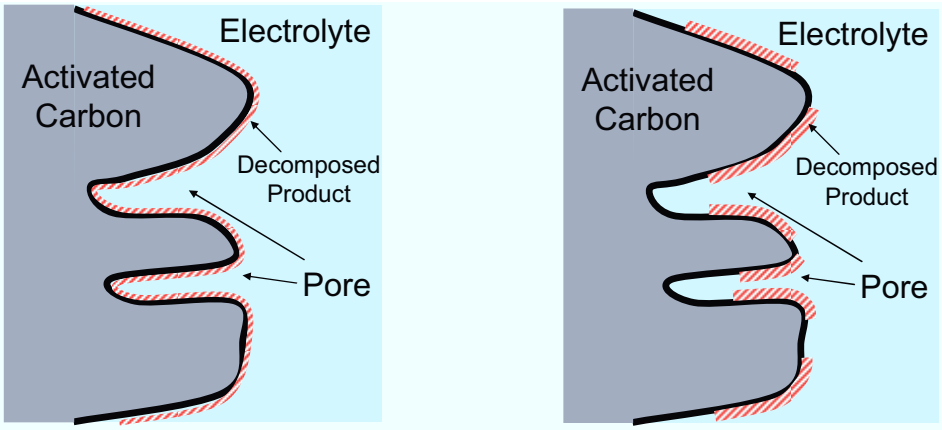


Fig. 3.4.2. Trends of activation energies of (a) 1500-F- and (b) 500-F-EDLCs, and (c) LICs during cycling.

LICs were approximately 11−15, 15−20, and 35−39 kJ/mol, respectively, almost independent on cycling conditions, and almost constant throughout the entire cycle testing.

The E_a of the cycled 500-F-EDLCs was approximately 17–20 kJ/mol, while that under floating conditions was 15 kJ/mol, as shown in Fig. 3.4.2(b). The difference in E_a implies that the temperature dependence of capacitance degradation was different between cycling and floating conditions. This tendency is considered consistent with the previous studies reporting that degradation mechanisms and behaviors under cycling and floating conditions are different [3]–[5]. The reported degradation mechanism is as follow; the electrolyte and impurity are decomposed, and the decomposition product, which might reduce accessibility of porous activated carbon electrodes, consequently reduces effective capacitance. Figs. 3.4.3(a) and (b) show images of deposition of decomposed products on activated carbon electrode during floating and cycling conditions, respectively. In floating conditions, the decomposition products is expected to deposit onto the electrode uniformly because of lack of ion movement, whereas preferential deposition near the entrance of pores is likely during cycling because of ion movement [3]–[5]. Although the difference in the determined activation energies implies the different degradation mechanisms, electrochemical investigations, which are out of scope of this study, is necessary to quantitatively correlate degradation mechanisms with activation energies.

Since EDLCs have symmetrical electrode structure using activated carbon electrode for both



(a) (b)

Fig. 3.4.3. Deposition of decomposed products on activated carbon electrode during (a) floating conditions and (b) cycling.

the anode and cathode, as mentioned in Section 2.3.1, the same degradation mechanism would take place on both the anode and cathode. On the other hand, the electrode structure of LICs are asymmetrical using activated carbon electrode and Li-doped carbon electrode for its cathode and anode, respectively, as explained in Section 2.3.2, the above-mentioned degradation takes place only on the cathode, and a degradation similar to that of LIBs is expected to occur on the anode electrode. The different degradations on the anode and cathode in the LICs are considered to be a cause of the higher activation energy of the LICs. However, further detailed investigation using electrochemical approach is necessary to elucidate the degradation mechanism and the higher activation energy of the LICs.

Acceleration factor α = 2, which generally indicates that life is halved for every 10°C increase, is commonly accepted for not only electrolytic capacitors and LIBs but also EDLCs in some cases [7],[16],[17]. Kötz et al. performed accelerated ageing tests for SCs under floating condition, and an acceleration factor of 2 for 10°C increase was experimentally obtained in a temperature range of 35°C–85°C [10]. Furthermore, previous studies for LIBs reported that E_a of the degradation rate of LIBs is approximately 43–48 kJ/mol [24], and α for LIBs is determined to be 1.7–2.1 on the basis of (3.15) in the temperature range of 0°C–40°C, implying that α = 2 is reasonable for LIBs. However, because the determined E_a for EDLCs and LICs under cycling in our study were rather lower than that for LIBs, α = 2 becomes impractical for EDLCs and LICs under cycling. From the determined E_a and (3.15), α for 1500-F- and 500-F-EDLCs and LICs under cycling in the temperature range 0–40°C was determined to be approximately 1.2, 1.3, and 1.64, respectively, suggesting that the degradations of 1500-F- and 500-F- EDLCs and LICs proceed 1.2, 1.3, and 1.64 times faster for every 10°C increase.

3.5 Cycle Life Prediction for SCs Based on Cycle Life Prediction Model

In this section, the cycle life prediction model combining the extrapolation and the acceleration factor determined from the Arrhenius equation discussed in Sections 3.4.1 and 3.4.2, respectively, is established. The relationship among cycle life, temperature, and capacitance retention at the end of life is discussed on the basis of the established cycle life

prediction model. Finally, examples of cycle life prediction to meet certain capacitance retention targets are shown.

3.5.1 Cycle Life Prediction Model

Because the capacitance retention trends as a function of the square root of the number of cycles could be extrapolated linearly and temperature dependence of the degradation was expressed using the acceleration factor, cycle life performance at a certain temperature can be predicted by combining the extrapolation and the acceleration factor. Substituting (3.7) and (3.14) into (3.6) yields

$$C_T = 100 - d_{Tref}\alpha^{\left(\frac{T-Tref}{10}\right)}\sqrt{N}\,. \tag{3.16}$$

This equation suggests that C_T at given N can be predicted by determining α and d_{Tref}.

A cycle life, N_{EoL}, is given by rewriting (3.16) as

$$N_{EoL} = \left\{\frac{100 - C_{EoL}}{d_{Tref}\alpha^{\left(\frac{T-Tref}{10}\right)}}\right\}^2, \tag{3.17}$$

where C_{EoL} is the capacitance retention at the end of life.

3.5.2 Cycle Life Prediction

Umemura et al. reported that the degradation behavior of EDLCs under floating conditions in the range of 40ºC–60ºC is governed by Arrhenius model [8]. Kötz et al. reported the same acceleration factor (a factor of 2 in their case) could be applied to SCs under floating conditions in the temperature range of 30ºC–85ºC [10]. Both studies imply that the activation energy in each test temperature range was homogeneous because activation energies can be obtained from either the Arrhenius equation or acceleration factor as discussed in Sections 3.4.1 and 3.4.2. Although the life testing in our study was performed under cycling conditions in the temperature range of 0°C–40°C, the temperature range for life predictions were extended to 0°C–60°C by assuming that the activation energy of the not only EDLCs but also LICs degradations in the experimental life performance tests would be homogeneous at least up to 60°C. Based on the assumption, cycle life predictions were performed in the temperature range of 0°C–60°C using (3.16) or (3.17) with the experimentally obtained activation energy E_a = 13, 18.5, and 35 kJ/mol, which yields an acceleration factor α = 1.2, 1.3, and 1.64 according to (3.15). Table 3.2 shows the parameters used for the cycle life prediction. d_{Tref} was determined

Table 3.2. Parameters used for cycle life prediction for SCs.

	1500-F-EDLC	500-F-EDLC	LIC
E_a	13 kJ/mol	18.5 kJ/mol	35 kJ/mol
R		8.314	
α	1.2	1.3	1.64
T_{ref}		40°C	
d_{Tref}	0.08	0.14	0.09
C_{EoL}		80%	

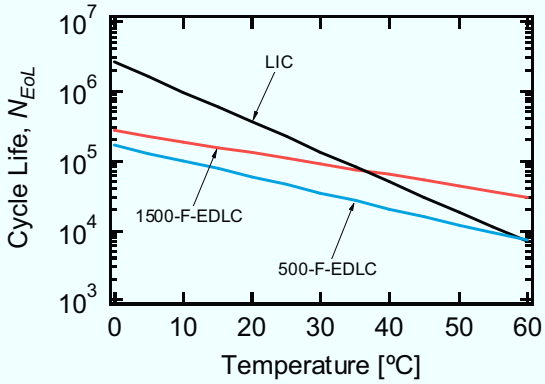


Fig. 3.5.1. Predicted cycle lives of EDLCs and LIC as a function of temperature.

from the capacitance retention at 40°C (Fig. 3.3.3–3.3.5).

On the basis of (3.17), Fig. 3.5.1 compares predicted cycle lives, N_{EoL}, of EDLCs and LICs, by assuming that the end of life is defined as the time at which the capacitance retention ratio decreases to 80% (i.e., C_{EoL} = 80%). The predicted cycle life of the 1500-F-EDLC was longer than that of the 500-F-EDLC at all temperatures, implying that their cell designs are different influencing cycle life performance. At temperatures higher than 37°C, the 1500-F-EDLC would operate longer than the LIC, whereas vice versa in the lower temperature region. The greater temperature dependence of the LIC's cycle life is due to the larger value of E_a than that of EDLCs.

Cycle life at a certain temperature can be predicted from the relationship shown in Fig. 3.5.1. However, the maximum allowable temperature required to achieve a certain cycle life may be more important in some applications because a higher allowable temperature simplifies system thermal design and management. For example, if 1500-F-EDLCs demand N_{EoL} of 30000 cycles, operating temperatures should be designed to be less than approximately 60°C. On the other hand, the temperature of the LIC would need to be controlled lower than approximately 45°C.

Cycle life of SCs was predicted on the basis of (3.16). Figs. 3.5.2(a) and (b) show examples of cycle life predictions for EDLCs and LICs, respectively. The experimental retention trends of Cells 1, 4, and 7, shown in Fig. 3.3.3–3.3.5, were also plotted as references. The experimental and predicted retention trends agreed well at all temperatures, thus proving that the cycle life prediction model expressed by (3.16) is appropriate for alternative battery applications. In addition, Fig. 3.5.2 also depicts the predicted capacitance retention trends that can achieve cycle life requirement at the highest possible ambient temperature. The results suggested that if a 1500-F- and 500-F-EDLCs are desired to fulfill cycle life requirements of 30000 and 60000 cycles or approximately 5.7 and 11.4 years at C_{EoL} = 80%, the temperature of the EDLCs must be designed to be less than 61°C and 42°C for 1500-F-cell, and 33°C and 20°C for 500-F-cell, respectively, to mitigate the temperature-dependent degradation. On the other hand, the temperature of a LIC needs to be controlled less than 45°C and 37°C, respectively, to meet the same cycle lire requirement.

The cycle life predictions were made based on the assumption that degradation mechanism would be homogeneous until the end of life. If unforeseen degradation mechanism (sudden

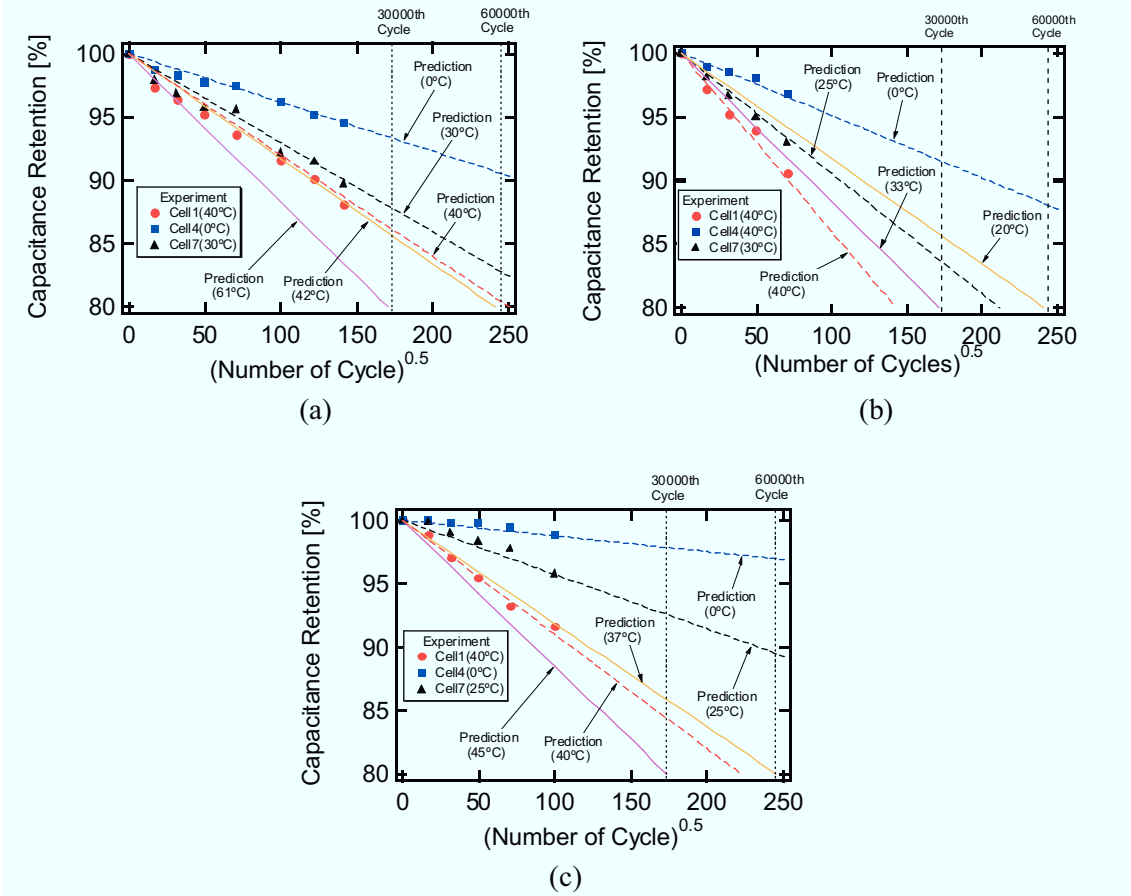


Fig. 3.5.2. Examples of cycle life prediction for (a) 1500-F- and (b) 500-F-EDLCs, and (b) LICs.

death in the worst case) were to occur ahead, the life prediction would be no longer feasible unless a new acceleration factor expressing the unforeseen degradation is properly adopted. As long as there is any possibility of unforeseen degradation mechanisms ahead, the cycle life testing should be continued until the SCs reach their end of life.

3.6 Conclusions

This chapter discussed accelerated cycle life testing and the cycle life prediction model for EDLCs and LICs aiming for alternative battery applications.

EDLCs and LICs were cycled at various DoDs, temperatures, and charge voltage conditions. The resultant capacitance retention trends were depicted linearly with the square root of the number of cycles as the x-axis, indicating that the retention trends can be linearly extrapolated. Capacitance retentions were mainly influenced by temperature, implying that degradations can be accelerated by elevating the temperature.

Activation energies of the degradation ratios of cycled EDLCs and LICs were determined by the Arrhenius equation. The determined activation energies that were almost constant for the entire testing period were determined to be 11–15, 15–20, and 35–39 kJ/mol for 1500-F- and 500-F-EDLCs and LICs, respectively. These activation energies correspond to the acceleration factors of approximately 1.2, 1.3, and 1.64 in the temperature range of 0–40°C, indicating that

degradation proceeded 1.2, 1.3, and 1.64 times faster for every 10°C increase.

The cycle life prediction model was established on the basis of combining the extrapolation and acceleration factor. The experimental and predicted capacitance retention trends agreed well at all temperature conditions, thus proving that the established cycle life prediction model is appropriate for EDLCs and LICs.

In this study, life prediction model for cycling was established. With an acceleration factor for floating conditions and transforming the number of cycles into testing time, the established life prediction model is considered to be adapted for floating life prediction model or even combined life prediction model. Establishment for floating and/or combined life prediction model as well as experimental verifications will be of future research interest.

3.7 References

[1] N. Rizoug, P. Bartholomeus, and P. Le Moigne, "Modeling and characterizing supercapacitors using an online method," *IEEE Transactions on Indudtrial Electronics*, Vol. 57, No. 12, pp. 3980–3990, Dec. 2010.

[2] A. Hammar, P. Venet, R. Lallemand, G. Coquery, and G. Rojat, "Study of accelerated aging of supercapacitors for transport applications," *IEEE Transactions on Industrial Electronics*, Vol. 57, No. 12, pp. 3972–3979, Dec. 2010.

[3] E. H. El Brouji, O. Briat, J. M. Vinassa, N. Bertrand, and E. Woirgard, "Impact of calendar life and cycling ageing on supercapacitor performance," *IEEE Transactions on Vehicular Technology*, Vol. 58, No. 8, pp. 3917–3929, Oct. 2009.

[4] O. Briat, J. M. Vinassa, N. Bertrand, H. El Brouji, J. Y. Deletage, and E. Woirgard, "Contribution of calendar ageing modes in the performances degradation of supercapacitors during power cycling," *Microelectronics Reliability*, Vol. 50, No. 9–11, pp. 1796–1803, Sep./Nov. 2010.

[5] H. El Brouji, O. Briat, J. M. Vinassa, N. Bertrand, and E. Woirgard, "Comparison between changes of ultracapacitors model parameters during calendar life and power cycling ageing tests," *Microelectronics Reliability*, Vol. 48, No. 8–9, pp. 1473–1478, Aug./Sep. 2008.

[6] H. Gualous, R. Gallay, G. Alcicek, B. Tala-Ighil, A. Oukaour, B. Boudart, and Ph. Makany, "Supercapacitor ageing at constant temperature and constant voltage and thermal shock," *Microelectronics Reliability*, Vol. 50, No. 9–11, Sep./Nov. 2010, pp. 1783–1788.

[7] R. Kötz, M. Hahn, and R. Gallay, "Temperature behavior and impedance fundamentals of supercapacitors," *J. Power Sources*, Vol. 154, No. 2, pp. 550–555, Mar. 2006.

[8] T. Umemura, Y. Mizutani, T. Okamoto, T. Taguchi, K. Nakajima, and K. Tanaka, "Life expectancy and degradation behavior of electric double layer capacitor Part I," in *Proc. the 7th Int. Conf. Properties and Applications of Dielectric Materials*, Vol. 3, pp. 944–948, Jun. 2003.

[9] P. Azais, L. Duclaux, P. Florian, D. Massiot, M. A. Lillo-Rodenas, A. Linares-Solano, J. P. Peres, C. Jehoulet, and F. Beguin, "Causes of supercapacitors ageing in organic electrolyte," *J. Power Sources*, Vol. 171, No. 2, pp. 1046–1053, Sep. 2007.

[10] R. Kötz, P. W. Ruch, and D. Cericola, "Aging and failure mode of electrochemical double layer capacitors during accelerated constant load tests," *J. Power Sources*, Vol. 195, No. 3, pp. 923–928, Feb. 2010.

[11] K. Paul, M. Christian, V. Pascal, C. Guy, R. Gerard, and Z. Younes, “Constant power cycling for accelerated ageing of supercapacitors,” in *Proc. European Conf. Power Electronics Applications*, pp. 1–10, Sep. 2009.
[12] J. Schiffer, D. Linzen, and D. U. Sauer, “Heat generation in double layer capacitors,” *J. Power Sources*, Vol. 160, No. 1, pp. 765–772, Sep. 2006.
[13] O. Bohlen, J. Kowal, and D. U. Sauer, “Ageing behavior of electrochemical double layer capacitors Part II. Lifetime simulation model for dynamic applications,” *J. Power Sources*, Vol. 173, No. 1, pp. 626–632, Nov. 2007.
[14] J. P. Fellner, G. J. Loeber, S. P. Vukson, and C. A. Riepenhoff, “Lithium-ion testing for spacecraft applications,” *J. Power Sources*, Vol. 119–121, pp. 911–913, Jun. 2003.
[15] X. Wang, Y. Sone, and S. Kuwajima, “Effect of operation conditions on simulated low-Earth orbit cycle-life testing of commercial lithium-ion polymer cells,” *J. Power Sources*, Vol. 142, No. 1–2, pp. 313–322, Mar. 2005.
[16] O. Bohlen, J. Kowal, and D. U. Sauer, “Ageing behaviour of electrochemical double layer capacitors Part I. Experimental study and ageing model,” *J. Power Sources*, Vol. 172, No. 1, pp. 468–475, Oct. 2007.
[17] P. Kurzwell and B. Frenzel, “Capacitance characterization methods and ageing behavior of supercapacitors,” in *Proc. the 15th Int. seminar on Double Layer Capacitors*, pp. 1–12, Dec. 2005.
[18] R. A. Marsh, S. Vukson, S. Surampudi, B. V. Ratnakumar, M. C. Smart, M. Manzo, and P. J. Dalton, “Li ion batteries for aerospace applications,” *J. Power Sources*, Vol. 97–98, pp. 25–27, Jul. 2001.
[19] S. Brown, K. Ogawa, Y. Kumeuchi, S. Enomoto, M. Uno, H. Saito, Y. Sone, D. Abraham, and G. Lindbergh, “Cycle life evaluation of 3 Ah $Li_xMn_2O_4$-based lithium-ion secondary cells for low-Earth-orbit satellites,” *J. Power Sources*, Vol. 185, No. 2, pp. 1444–1453, Dec. 2008.
[20] M. Uno, K. Ogawa, Y. Takeda, Y. Sone, K. Tanaka, M. Mita, and H. Saito, “Development and on-orbit operation of lithium-ion pouch battery for small scientific satellite "REIMEI",” *J. Power Sources*, Vol. 196, No. 20, pp. 8755–8763, Oct. 2011.
[21] L. H. Thaller, “Expected cycle life vs. depth of discharge relationships of behaved single cells and cell strings,” *J. Electrochemical Society*, Vol. 130, No. 5, pp.986–990, May 1983.
[22] M. S. Berberich and H. Willmes, “Concept for a 48 V DC power supply system with lithium ion batteries for telecom applications,” in *Proc. IEEE International Telecommunication Energy Conference*, pp. 31–36, 2007.
[23] J. P. Fellner, G. J. Loeber, S. P. Vukson, and C. A. Riepenhoff, “Lithium-ion testing for spacecraft applications,” *J. Power Sources*, Vol. 119-121, pp. 911–913, Jun. 2003.
[24] H. Yoshida, N. Imamura, T. Inoue, K. Takeda, and H. Naito, “Verification of life estimation model for space lithium-ion cells,” *Electrochemistry*, Vol. 78, No. 5, pp. 482–488, 2010.
[25] Y. Mita, S. Seki, N. Terada, N. Kihira, K. Takei, and H. Miyashiro, “Accelerated test methods for life estimation of high-power lithium-ion batteries,” *Electrochemistry*, Vol. 78, No. 5, pp. 382–386, 2010.

Chapter 4
Power System Mass Comparison

4.1 Introduction

Mass saving and life extension are the primary requirements for spacecraft power systems. Other miscellaneous requirements include wide temperature tolerance, abuse tolerance, safety, operational simplicity, etc. For the adaptation of a power system using an EDLC or LIC for its energy storage source to be of benefit to a spacecraft as a whole, one of the following criteria must be fulfilled; 1) the EDLC- or LIC-based power system must achieve a longer operation life than would have been achieved with a power system using a traditional secondary battery at the comparable mass, 2) the EDLC- or LIC-based system must achieve a lighter power system mass than would have been achieved with a power system using a traditional secondary battery at the comparable operation life. Since the specific energy of LICs is higher than that of conventional EDLCs, LICs are expected more promising in spacecraft power systems where mass saving is of primary importance.

This chapter compares the masses of power systems using LIBs and SCs as its energy storage source for LEO spacecraft applications. A constant power (CP) charging scheme that can reduce the size and mass of photovoltaic (PV) arrays in combination with SCs is proposed. The LIB- and LIC-based power systems, including PV arrays and power conditioning system, are compared at various DoD levels with respect to mass at a given LEO spacecraft condition.

4.2 Specific Energy Comparison

As aforementioned in Chapter 2, the specific energies of EDLCs and LICs are rather lower than those of secondary batteries. However, the specific energy gap between secondary batteries and SCs can be bridged to a great extent when we consider the net specific energy, which is defined as

$$Net\,Specific\,Energy = Specific\,Energy \times DoD\,. \tag{4.1}$$

Specific energies of space-qualified alkaline batteries, such as Ni–Cd, Ni–MH, and Ni–H_2 batteries, are 40–60 Wh/kg (cell), and that of space-qualified LIBs is less than 150 Wh/kg (cell) [1]–[3]. Generally, DoD for LEO spacecrafts is less than 40% to achieve > 30000 cycles [2]–[4]. Therefore, the net specific energies of these batteries are at least less than 40% of their specific energies, as shown in Table 1.

Specific energies of state-of-the-art EDLCs and LICs are <10 Wh/kg (cell) and <30 Wh/kg (cell), respectively. Because the cycle life performance of EDLCs and LICs is independent of DoD, as demonstrated in Chapter 3, they can be cycled at deep DoD for achieving high net specific energy. In Table 4.1, the net specific energies at 80% DoD that allow a maximum degradation of 20% are given as an example. The net specific energy of LIC can match that of

Table 4.1. Comparison between traditional secondary battery cells and capacitors.

	Secondary Battery		Capacitor	
	Alkaline Battery (Ni-Cd, Ni-MH, and Ni-H_2)	Lithium-Ion Battery (LIB)	Electric Double-Layer Capacitro (EDLC)	Lithium-Ion Capacitor (LIC)
Specific Energy	40–60 Wh/kg	150 Wh/kg	< 10 Wh/kg	< 30 Wh/kg
Depth of Discharge	< 40%	< 40%	< 80%	< 80%
Net Specific Energy	< 24 Wh/kg	< 60 Wh/kg	< 8 Wh/kg	< 24 Wh/kg

alkaline batteries, although it is still rather lower than that of LIB. The net specific energies of SCs can even increase with deeper DoD, although allowable degradation as well as achievable cycle life are reduced (e.g., 90% DoD allows 10% degradation).

Although the gap between LIBs and SCs is bridged to a great extent, it still seems unlikely that SCs are considered to be an alternative energy storage source to LIBs for spacecraft applications with the traditional cycle life requirement of 30000 cycles. However, for even longer cycle life requirements, DoDs for LIBs must be even shallower to mitigate DoD-dependent degradations, further reducing the net specific energy of LIBs. This implies that EDLCs and LICs for longer cycle life requirements would compete with LIBs in terms of net specific energy. In addition, the size and mass of PV arrays can be reduced when EDLCs and LICs are used, contributing mass saving at power system level, as explained later. Thus, EDLCs and LICs are expected to be a potential alternative energy storage source for longer cycle life applications.

4.3 Size and Mass Reduction of Photovoltaic Arrays

4.3.1 Charge Characteristics of LIB and SC

A constant current–constant voltage (CC–CV) charging scheme is usually used so that LIBs can be charged to a high state-of-charge (SoC) level. With the CC–CV charging scheme, the charge power of LIBs peaks at the end of the CC charging period or at the beginning of the CV

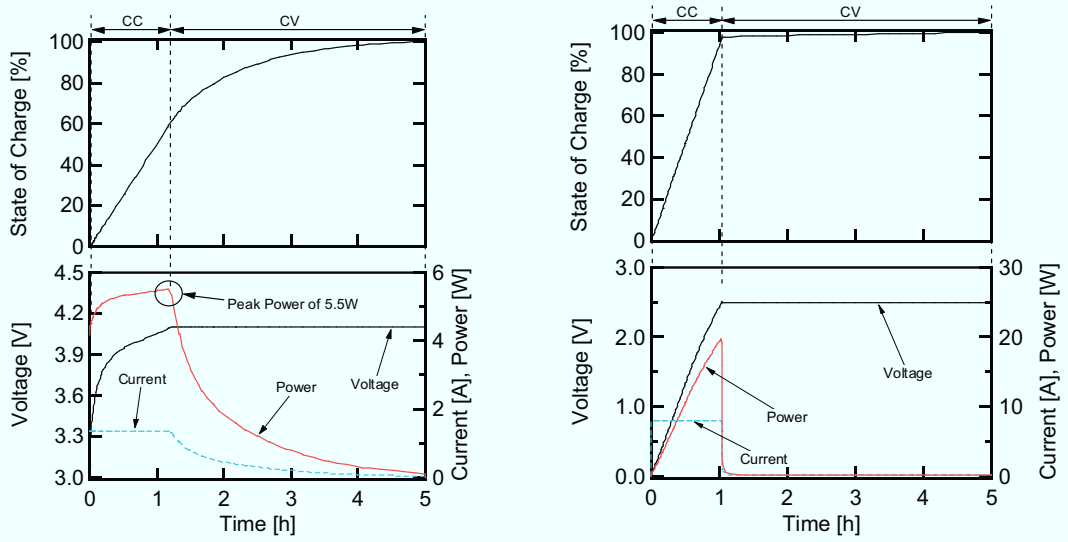


Fig. 4.3.1. Typical charge profiles of (a) a 10-Wh LIB cell and (b) a 10-Wh EDLC cell charged with a constant current–constant voltage (CC–CV) charging scheme.

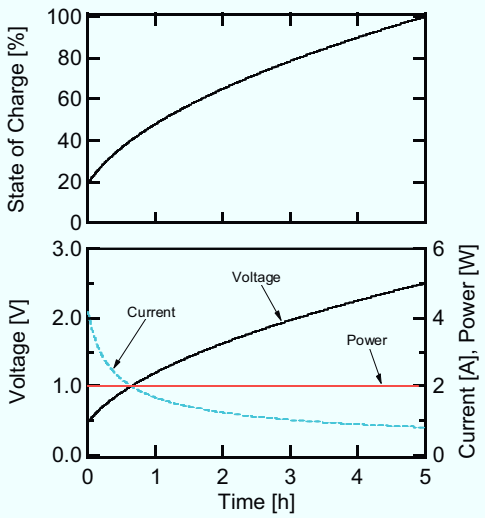


Fig. 4.3.2. Notional charge profiles of an EDLC cell charged with a constant-power (CP) charging scheme.

charging period, as shown in Fig. 4.3.1(a), which illustrates the typical charge profiles of a 10-Wh LIB cell. Without CV charging, the SoC of LIBs reaches only less than 60–80% depending on the battery design, state of health, temperature, and charge rate. To charge LIBs to a high SoC level, the CV charging period is necessary.

On the other hand, to reach a high SoC level, SCs do not necessarily need to be charged with CV charging, as shown in Fig. 4.3.1(b), which illustrates the typical charge characteristics of a 10-Wh EDLC cell charged with the CC–CV charging scheme. EDLCs can be almost fully charged (97% or even higher) with CC charging only. By eliminating the CV charging period and introducing a constant-power (CP) charging scheme, the required power to charge EDLCs can be leveled and the peak power for charging can be reduced, as depicted in Fig. 4.3.2. This charging scheme (CP charging without CV charging) may be used for LIBs, although achievable SoC is reduced by approximately 20–40% as mentioned above. This SoC reduction may be acceptable at the beginning of life, at which there is a margin for capacity retention. At the end of life, on the other hand, a serious shortage of available capacity is very likely. For example, with approximately 50% capacity retention at the end of life (shown in Fig. 3.3.2), the 40% reduction in SoC due to the lack of CV charging results in only 10% available capacity, with which spacecrafts are no longer powered for entire period of eclipse.

The charge characteristic of EDLCs was discussed in this section. Since LICs exhibit similar charge characteristics, the peak power reduction by introducing the CP charging scheme is also feasible for LICs.

4.3.2 Cycle Profiles of LIB- and SC-Based Power Systems

Fig. 4.3.3 shows typical profiles of a LIB and PV power during LEO-emulated cycling. A load power profile, which is assumed constant for the sake of simplicity, is also depicted. As mentioned in the previous section, the LIB needs CV charging to reach a high SoC level; otherwise, it results in a lower SoC. The charge power for the LIB becomes the highest at the

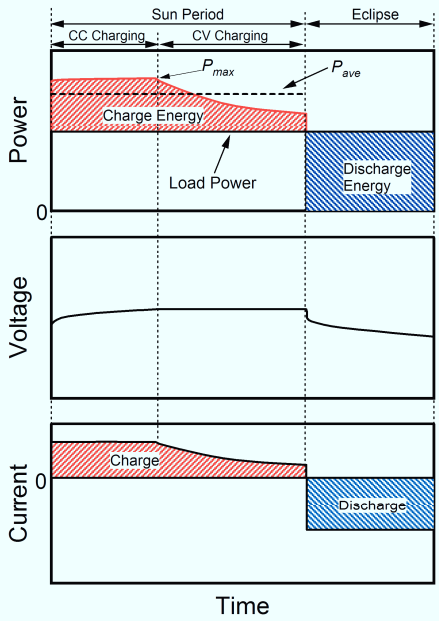


Fig. 4.3.3. Typical profiles of a LIB and PV power during LEO-emulated charge-discharge cycling.

end of the CC charging period (or at the beginning of the CV charging period) at which both the voltage and charge current are the highest, as seen in Fig. 4.3.3. The power demand for PV arrays is the sum of the load power and charge power for the LIB. Assuming that the load power is constant, PV arrays are required to supply the maximum power, P_{max}, at the end of the CC charging period, as shown in Fig. 4.3.3. The average power demand during the sun period is denoted by P_{ave}. The power demand decreases as the charge current for the LIB tapers, and thus, the arrays' power varies significantly during the sun period [5]. Therefore, PV arrays are not fully utilized because of the large variation in the LIB charge power. It is reported that only 73% of available solar array energy is used at a certain condition [6]. The surplus power of PV arrays in a direct energy transfer (DET) system is dissipated by shunt dissipators. The larger the surplus power of PV arrays, the larger the size of shunt dissipators. In a power system using series regulators, on the other hand, the surplus power is not extracted, even though it leads to a temperature increase of PV arrays.

As for SCs, CV charging is not necessary for SCs to be charged to a high SoC level as discussed in the previous section. Instead of the CC charging scheme, a CP charging scheme can be used. Fig. 4.3.4 shows the notional profiles of an SC using a CP charging scheme and PV power during a LEO-emulated charge-discharge cycling. By properly designing the charge power during CP charging so that the voltage reaches the rated charge voltage at the end of the sun period, the power demand for PV arrays can be leveled and P_{max} can be curtailed to P_{ave}, as shown in the top panel of Fig. 4.3.4. Because the value of P_{max} is roughly proportional to the size and mass of PV arrays, the power demand leveling using SCs can reduce the size and mass of PV arrays. Fig. 4.3.4 depicts the ideal case where the load power is constant and there is no surplus power. In practice, however, the load power fluctuates and there must be a surplus

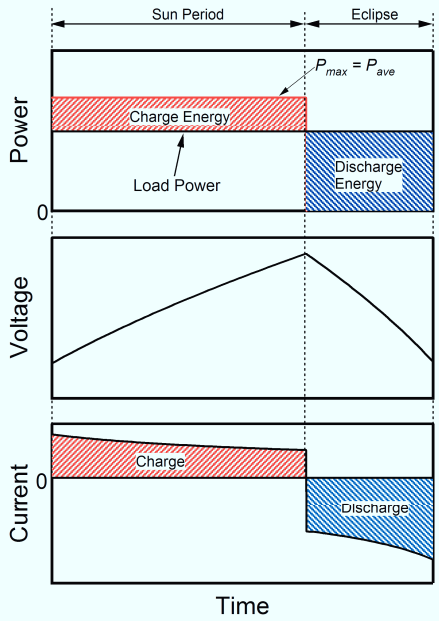


Fig. 4.3.4. Notional profiles of a LIC using CP charging scheme and PV power during LEO-emulated charge-discharge cycling.

power that needs to be dissipated by the shunt dissipator if the power system is a DET type. Although the shunt dissipator is still needed, the size of the dissipator can be reduced because of the reduced surplus power.

The reduced size of PV arrays offers some miscellaneous benefits at the spacecraft level [7]. LEO spacecrafts require a reboost of their altitude in orbit, because the atmospheric drag constantly decreases their altitude. PV arrays with reduced size can decrease the atmospheric drag, providing less opportunities of reboosting and decreased mass of the chemical propellant. Furthermore, because the torque compensation hardware, such as wheels and magnetic torquers, must be sized for the drag and the moment of inertia of the spacecraft, smaller PV arrays can reduce the size and burden of the attitude control system.

4.4 Mass Comparison between LIB- and LIC-Based Power Systems

In the following sections in this chapter, only LICs, which are the most feasible capacitors for spacecraft applications, are considered and then compared with LIBs. The masses of the LIB-based and LIC-based power systems, including PV arrays, are compared in this section. The comparative analysis is made on the basis of the DET system shown in Fig. 4.4.1. Masses of the energy storage source (i.e., LIB and LIC), PV arrays, and power conditioning system (PCS) including discharge regulator, charge regulator, and shunt dissipator, are considered for the comparison.

4.4.1 LIB-Based Power System

A single charge-discharge cycle consists of the sun and eclipse periods with a length of T_{sun} and $T_{eclipse}$, respectively. The energy storage source supplies the power to the load via the discharge regulator during the eclipse period. The discharged energy during the eclipse period,

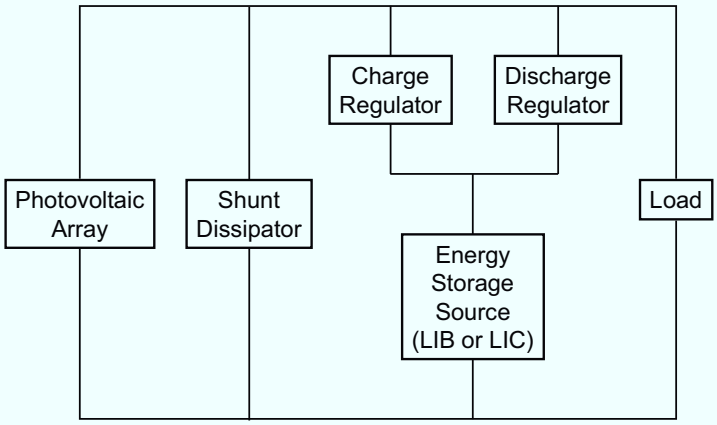


Fig. 4.4.1. DET electrical power system.

E_{dis}, is expressed as

$$E_{dis} = \frac{P_{load} T_{eclipse}}{\eta_{dis}}, \tag{4.2}$$

where P_{load} is the load power, and η_{dis} is the efficiency of the discharge regulator.

A battery contains cells and mechanical structural supports that present approximately 20% increase in mass over that of the cells [8]. By defining A as the ratio of the mechanical structural supports to the mass of the cells, the mass of the LIB, M_{LIB}, can be determined as

$$M_{LIB} = \frac{E_{dis}(1+A)}{D_{Ah} S_{LIB\_cell}}. \tag{4.3}$$

where S_{LIB_cell} is the specific energy of the LIB cell, and D_{Ah} is the ampere-hour DoD, which was defined in Chapter 3.2.2.

The capacity of the LIB, C_{LIB}, can be determined as

$$C_{LIB} = \frac{E_{dis}}{D_{Ah} V_{ave}}, \tag{4.4}$$

where V_{ave} is the average voltage during discharging.

The charge current for the LIB, I_{cha}, is

$$I_{cha} = C_{LIB} R_{cha}. \tag{4.5}$$

where R_{cha} is the charge rate, also well known as C-rate. We defined the charge/discharge ratio, $R_{C/D}$, as

$$R_{C/D} = \frac{R_{cha} T_{sun}}{D_{Ah}}. \tag{4.6}$$

For LEO spacecrafts, an $R_{C/D}$ equal to 1.25 is used in the literature [2], [9].

The charge power from PV arrays is supplied via a charge regulator with an efficiency η_{cha}. As mentioned in Section 4.3.1, the LIB requires the maximum charge power at the end of CC

charging or at the beginning of CV charging, at which the voltage of the LIB is as high as V_{cha}. Therefore, the power demand for PV arrays from the LIB, P_{cha_LIB}, is represented as

$$P_{cha\_LIB} = \frac{I_{cha} V_{cha}}{\eta_{cha}} . \tag{4.7}$$

The mass of PV arrays in the LIB-based system, M_{PV_LIB}, with the specific power of ρ_{PV}, is determined as

$$M_{PV\_LIB} = \frac{P_{load} + P_{cha\_LIB}}{\rho_{PV}} . \tag{4.8}$$

Assuming that the shunt dissipator is designed capable of the sum of P_{load} and P_{cha_LIB}, the mass of the PCS in the LIB-based system, M_{PCS_LIB}, is given by

$$M_{PCS\_LIB} = P_{cha\_LIB} m_{cha} + P_{load} m_{dis} + \left(P_{cha\_LIB} + P_{load}\right) m_{Shunt} , \tag{4.9}$$

where m_{cha}, m_{dis}, and m_{Shunt} are the mass/watt coefficient of the charge regulator, discharge regulator, and shunt dissipator, respectively [10].

From (4.3), (4.8), and (4.9), the mass of the LIB-based system, M_{LIB_System}, is given by

$$M_{LIB\_System} = M_{LIB} + M_{PV\_LIB} + M_{PCS\_LIB} . \tag{4.10}$$

4.4.2 LIC-Based Power System

The mass of the LIC, M_{LIC}, is represented as

$$M_{LIC} = \frac{E_{dis}\left(1 + A\right)}{D_E S_{LIC\_cell}} . \tag{4.11}$$

where S_{LIC_cell} is the specific energy of the LIC cell, and D_E is the energy DoD defined in Chapter 3.2.2.

As discussed in Section 4.3.1, the LIC can be charged with the CP charging scheme so that the LIC is fully charged at the end of the sun period. The power demand for PV arrays from the LIC using the CP charging scheme, P_{cha_LIC}, is expressed as

$$P_{cha\_LIC} = \frac{E_{dis}}{\eta_{cha} T_{sun}} . \tag{4.12}$$

The mass of PV arrays in the LIC-based system, M_{PV_LIC} and M_{PCS_LIC}, respectively, are

$$M_{PV\_LIC} = \frac{P_{load} + P_{cha\_LIC}}{\rho_{PV}} , \tag{4.13}$$

$$M_{PCS\_LIC} = P_{cha\_LIC} m_{cha} + P_{load} m_{dis} + \left(P_{cha\_LIC} + P_{load}\right) m_{Shunt} . \tag{4.14}$$

From (4.11), (4.13), and (4.14), the mass of the LIC-based system, M_{LIC_System}, is determined as

$$M_{LIC\_System} = M_{LIC} + M_{PV\_LIC} + M_{PCS\_LIC} . \tag{4.15}$$

Table 4.2. Parameters used for the mass comparison between LIB-based and LIC-based electrical power systems.

Parameter	Symbol	Value
Load Power	P_{load}	1000 W
Sun Period	T_{sun}	1 h
Eclipse Period	$T_{eclipse}$	0.5 h
C/D Ratio (for LIB only)	$R_{C/D}$	1.25
Charge Voltage (LIB only)	V_{cha}	28.7 V
Average Discharge Voltage (LIB only)	V_{ave}	25.9 V
Ratio of Mechanical Strucrural Supports	A	20%
Specific Power of PV Array	ρ_{PV}	60 W/kg
Efficiency of Discharge Regulator	η_{dis}	90%
Efficiency of Charge Regulator	η_{cha}	90%
Mass/Watt Coefficient of Discharge Regulator	m_{dis}	7 kg/kW
Mass/Watt Coefficient of Charge Regulator	m_{cha}	7 kg/kW
Mass/Watt Coefficient of Shunt Dissipator	m_{Shunt}	2 kg/kW

4.4.3 Mass Comparison between LIB- and LIC-Based Power Systems

The mass of the LIB- and LIC-based systems for P_{load} of 1000 W were compared on the basis of the parameters shown in Table 4.2. The specific energies of rigid honeycomb-based PV arrays are usually 50–70 W/kg [11]–[13]. Assuming that multi-junction solar cells are used for PV arrays, ρ_{PV} has a typical value of 60 W/kg. The values of m_{CR}, m_{DR}, and m_{Shunt} were determined based on [10]. Because the discharge curve of LIBs is flat as shown in Fig. 2.4.1, D_{Ah} of the LIB was assumed to be equal to D_E for the sake of simplicity. The mass of the LIB- and LIC-based power systems with nominal specific energies of S_{LIB_cell} = 150 Wh/kg and S_{LIC_cell} = 30 Wh/kg as well as those with ± 20% variations (i.e., S_{LIB_cell} = 120 and 180 Wh/kg, and S_{LIC_cell} = 24 and 36 Wh/kg) as a function of energy DoD (D_E) are depicted in Fig. 4.4.2.

The mass of the LIB-based system at the deep DoD region of about 40% was less than 63 kg. This could not be achieved by the LIC-based system. From the system mass viewpoint, the LIC cannot be an alternative energy storage source to the LIB for relatively deep DoD applications unless the outstanding cycle life performance of the LIC is took into consideration. On the other hand, the LIB-based system in the shallow DoD region, in which the cycle life performance is

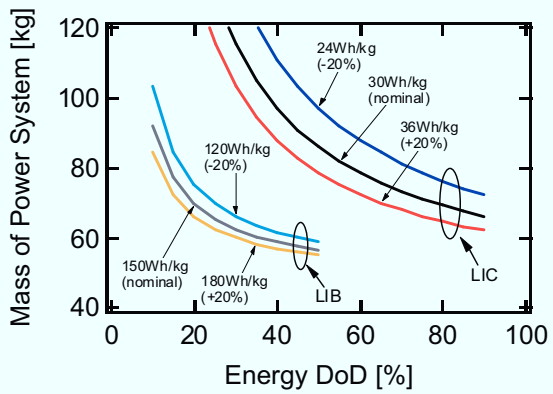


Fig. 4.4.2. Mass of LIB- and LIC-based electrical power systems as a function of energy DoD.

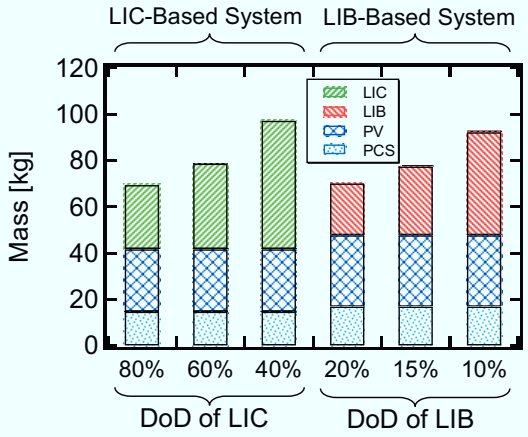
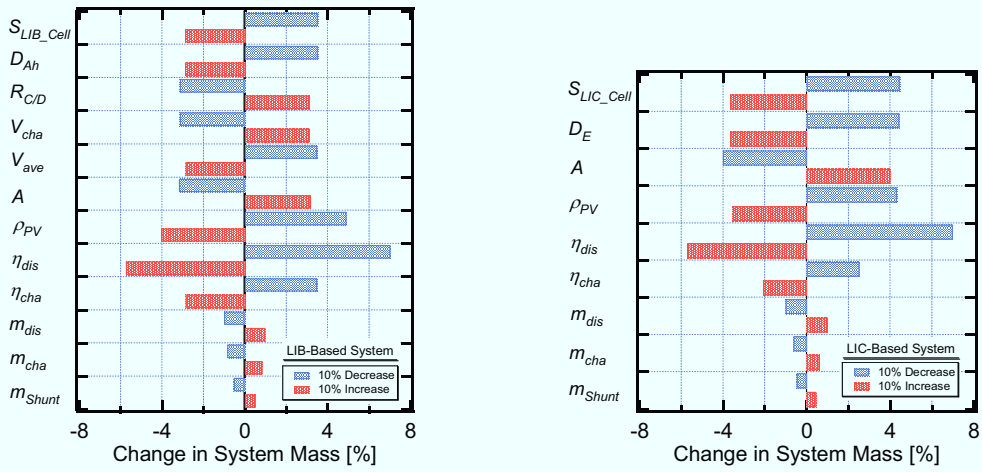


Fig. 4.4.3. Mass breakdown of the LIB- and LIC-based system with S_{LIB_Cell} = 150 Wh/kg and S_{LIC_cell} = 30 Wh/kg, respectively.

extended and longer service life is achievable, was comparable with the LIC-based system with S_{LIC_cell} larger than 30 Wh/kg in the deep DoD region.

Fig. 4.4.3 shows the mass breakdowns of LIB- and LIC-based systems with baseline specific energies of S_{LIB_cell} = 150 Wh/kg and S_{LIC_cell} = 30 Wh/kg, respectively. The mass of PV arrays was independent of DoD for both systems and was determined to be 30.9 and 27.0 kg for LIB- and LIC-based systems, respectively, and approximately 13% of PV arrays mass was saved in the LIC-based system compared with the LIB-based system. The mass of the PCS in the LIC-based system was smaller than that in the LIB-based system; M_{PCS_LIB} and M_{PCS_LIC} were determined to be 17.0 and 14.5 kg, respectively. Since the charge power for the LIC (P_{cha_LIC}) can be smaller than that for the LIB (P_{cha_LIC}) as discussed in Section 4.3.1, the PCS mass in the LIC-based system was saved compared with that in the LIB-based system, as can be understood from (4.9) and (4.14).

The longer the cycle life required, the shallower the DoD of LIBs needs to be. When the cycle life longer than the conventional cycle life requirement of more than 30000 cycles is required, DoD may have to be even shallower than 20%. DoDs for both systems in Fig. 4.4.3 are considered suitable for achieving a longer cycle life requirement. At 20% DoD for the LIB-based system, for example, the system mass was approximately 69.8 kg and this was comparable with the LIC-based system at 80% DoD (69.3 kg). Similarly, the LIB-based system at DoD lower than 15% was comparable with the LIC-based system at 60% DoD. Thus, the LIC is considered to be an alternative to the LIB that is operated with shallow DoD for achieving long cycle life, even from the system mass viewpoint, although the energy demand in contingency operations should be considered for the LIC at deep DoD. If the system masses of LIB- and LIC-based systems are comparable, the LIC-based system is considered advantageous from the viewpoint of operation temperature. For example, LIBs are usually operated between 0–10°C in order to mitigate temperature-dependent calendar degradations at reasonable electrical characteristics (see Fig. 2.4.1(a)) to fulfill the typical life requirement in spacecrafts. Meanwhile, the estimated operation temperature for LICs to fulfill the cycle life requirement of 30000 and 60000 cycles are <45°C and <37°C, respectively, as shown in Fig. 3.5.2(c) in the



(a) (b)

Fig. 4.4.4. Tornado diagrams considering ±10% changes in each parameter for (a) the LIB-based system with S_{LIB_Cell} = 150 Wh/kg and D_{Ah} = 20%, and (b) the LIC-based system with S_{LIC_Cell} = 30 Wh/kg and D_E = 80%.

previous chapter. With the extended operation temperature range, the thermal system of spacecrafts can be designed more flexibly. Once the other miscellaneous benefits, such as mass reductions of the shunt dissipator, chemical propellant, and attitude control system (as mentioned in Section 4.3.2), are factored in, the likelihood of the LIC to be an alternative energy storage source can be further improved.

Considering that a number of design parameters were included in the mass comparisons made in Figs. 4.4.2 and 4.4.3, the sensitivity analyses were performed in order to investigate the percentage impact of each design parameters on the power systems mass. The LIB-based system with S_{LIB_Cell} = 150 Wh/kg and D_{Ah} = 20%, and the LIC-based system with S_{LIC_Cell} = 30 Wh/kg and D_E = 80% were analyzed considering ±10% changes in each design parameter value specified in Table 4.2. The results of the sensitivity analysis are shown in Fig. 4.4.4, in which the percentage impact on the system mass are illustrated in the form of a tornado diagram. For example, if the value of S_{LIB_Cell} increased (decreased) by 10%, the mass of the LIB-based system would decrease (increase) by approximately 2.9% (3.5%). The LIB- and LIC-based systems showed similar tendency; the efficiency of the discharge regulator, η_{dis}, exhibited the largest impact, while the mass/watt coefficients for the PSC, m_{Shunt}, m_{dis}, and m_{cha}, showed the minimal influences.

Except for η_{dis}, ρ_{PV} exhibited the largest impact on the system mass in the LIB-based system, and the influences of the LIB-related parameters (i.e., S_{LIB_Cell}, D_{Ah}, $R_{C/D}$, V_{cha}, V_{ave}, and A) were in the same level and were smaller than that of ρ_{PV}. The impacts of ρ_{PV} and η_{cha} in the LIB-based system were greater than those in the LIC-based system. Since the charge power as well as the power demand for the PV arrays in the LIB-based system using the CC–CV charging scheme tend to be larger than those in the LIC-based system employing the CP charging scheme as discussed in Section 4.3.1, the impact of charging-related parameters (i.e., ρ_{PV} and η_{cha}) in the LIB-based system was greater. On the other hand, in the LIC-based system, the influences of

the parameters related to the LIC, such as S_{LIC_Cell}, D_E, and A, were larger than those in the LIB-based system, while the impact of ρ_{PV} in the LIC-based systems was smaller than that in the LIB-based system. This is because the mass ratio of the energy storage source in the LIC-based system was larger than that in the LIB-based system as shown in Fig. 4.4.3. Thus, the results of the sensitivity analysis suggest that in order to reduce the system mass, different approaches would be effective for different systems; except for η_{dis}, the improvement on ρ_{PV} would be most effective in the LIB-based system, while not only the improvement on ρ_{PV} but also that on LIC-related parameters, such as S_{LIC_Cell}, D_E, and A, would be equally important in the LIC-based system.

4.5 Conclusions

The masses of power systems using LIBs and SCs as its energy storage source for LEO spacecraft applications were compared in this chapter. A CP charging scheme that can reduce the size and mass of PV arrays in the SC-based power system was proposed. LIBs usually need not only CC charging but also CV charging to be charged to a high SoC level, while SCs can reach a high SoC without CV charging. Using CP charging instead of CC charging, the power demand for PV arrays from SCs can be leveled to be constant, resulting in a reduction of the size and mass of PV arrays.

The mass comparison between the LIB- and LIC-based power systems was made on the basis of the DET system. In the case that the LIB-based system is operated at a relatively shallow DoD (shallower than 20%) to achieve long cycle life, the LIC-based system with deep DoD (60–80%) can be comparable. The analysis indicated that the LIC can be an alternative energy storage source that achieves longer operation life at extended operation temperature range than would have been achieved with LIBs at comparable power system mass. Other miscellaneous benefits, such as mass reductions of the shunt dissipator, chemical propellant, and attitude control system, improve the likelihood of LICs being considered to be a spacecraft energy storage source.

References

[1] H. Yoshida, N. Imamura, T. Inoue, K. Takeda, and H. Naito, “Verification of life estimation model for space lithium-ion cells,” *Electrochemistry*, Vol. 78, No. 5, pp. 482–488, 2010.

[2] X. Wang, Y. Sone, H. Naito, C. Yamada, G. Segami, and K. Kibe, “Cycle-life testing of 100-Ah class lithium-ion battery in a simulated geosynchronous-Earth-orbit satellite operation,” *J. Power Sources*, Vol. 160, pp. 602–608, Sep. 2006.

[3] X. Wang, Y. Sone, H. Naito, C. Yamada, G. Segami, and K. Kibe, “Cycle-life testing of large-capacity lithium-ion cells in simulated satellite operation,” *J. Power Sources*, Vol. 161, pp. 594–600, Oct. 2006.

[4] B. V. Ratnakumar, M. C. Smart, C. K. Huang, D. Perrone, S. Surampudi, and S. G. Greenbaum, “Lithium-ion batteries for Mars exploration missions,” *Electrochemica Acta*, Vol. 45, pp. 1513–1517, Jan. 2000.

[5] Z. Jiang, S. Liu, and R. A. Dougal, “Design and testing of spacecraft power systems using VTB,” *IEEE Trans. Aerosp. Electron. Syst.*, Vol. 39, No. 3, pp. 976–989, Oct. 2003.

[6] M. A. Hoberecht and R. D. Green, “Use of excess solar array power by regenerative fuel cell energy storage systems in low Earth orbit,” in *Proc. Energy Conversion Engineering Conference*, pp. 224–227, 1997.
[7] M. R. Patel, *Spacecraft Power Systems*. London: CRC Press, 2005, chapter 7.3.2.
[8] S. C. Roberts and G. S. Aglietti, “Structural performance of a multifunctional spacecraft structure based on plastic lithium-ion batteries,” *Acta Astronautica*, Vol. 67, pp. 424–439, Sep. 2010.
[9] J. P. Fellner, G. J. Loeber, S. P. Vukson, and C. A. Riepenhoff, “Lithium-ion testing for spacecraft applications,” *J. Power Sources*, Vol. 119-121, pp. 911–913, Jun. 2003.
[10] A. Capel and P. Perol, “Comparative performance evaluation between the S4R and the S3R regulated bus topologies,” in *Proc. IEEE Power Electronics Specialist Conference*, pp. 1963–1969, 2001.
[11] K. Shimazaki, Y. Kobayashi, M. Takahashi, M. Imaizumi, T. Takamoto, T. Ito, and Y. Nozaki, “Development status of ultra-lightweight solar panel using space solar sheet,” in *Proc. IEEE Photovoltaic Specialist. Conference*, pp. 2457–2461, 2009.
[12] J. Merrill, P. E. Hausgen, D. C. Senft, and H. H. Yoo, “Current status of photovoltaic development at AFRL,” in *Proc. IEEE Aerospace Conference*, pp. 1–5, 2005.
[13] J. Gibb and S. Billets, “A case study: Integrating triple-junction solar cells into flat-folding flexible solar array panels,” in *Proc. IEEE Photovoltaic Specialist. Conference*, pp. 731–735, 2010.

Chapter 5
Cell Voltage Equalizer

5.1 Introduction

Since the cell voltage of LIBs and SCs is inherently low, individual cells need to be connected in series to meet the voltage demands of certain loads. However, series-connected energy storage cells suffer from a cell voltage imbalance that may lead to premature ageing and a decrease in the available energies of the cells. Cell voltage imbalance inevitably occurs because of differing individual cell properties such as capacitance, internal impedance, and self-discharge rate. In addition to such nonuniform electrical properties, the temperature gradient in a module/battery that accelerates the nonuniform self-discharging of cells can also result in cell voltage imbalance.

Although the average voltage of series-connected cells is lower than or equal to the upper voltage limit, a voltage imbalance may result in the overcharging of some cells. Similarly, some cells may be over-discharged though the average voltage is higher than or equal to the lower voltage limit. Because overcharging and over-discharging the cells cause irreversible deteriorations, each individual cell voltage should be maintained within a specified safety voltage range. However, as long as the cells are charged (discharged) in series, the charging (discharging) process should be limited by the cell with the highest (lowest) voltage so that no cell is overcharged (over-discharged). With such limitations, the cells cannot be fully charged (discharged), and hence, series-connected cells exhibit poor energy utilization. Therefore, cell voltage imbalances should be minimized in order to prolong the life of the cells and maximize their available energies.

Firstly, general requirement for cell voltage equalizers for SCs in spacecraft applications is discussed. Secondly, conventional cell voltage equalizers, which have been used for LIBs and SCs, are reviewed in order to describe general drawbacks underlying in conventional equalizers. Thirdly, high-frequency charge-discharge cycling induced by cell voltage equalizers, which may cause premature deterioration of energy storage cells, is addressed. The influence of high-frequency cycling on life performance of lithium-ion cells are experimentally investigated, and proper switching frequency region for cell voltage equalizers is determined. Lastly, three novel equalizers are proposed in Sections 5.5, 5.6, and 5.7.

5.2 General Requirement for Cell Voltage Equalizer for Supercapacitors in Spacecraft

High-reliability is a primary requirement for electronics in spacecrafts. Since SCs are inherently long-life energy storage cells, the reliability of peripheral electronics including cell voltage equalizers would be considered more important than ever. Reducing component count is one of the most effective approach to improve the reliability. In cell voltage equalizers, the number of switches is considered to be a good index for representing a circuit's complexity

because each switch requires a driver IC and ancillary components, such as resistors, capacitors, diodes, and opto-couplers. Therefore, the reduction in the number of switch is the key to improve the equalizers' reliability.

In order to utilize stored energies of SCs as efficiently as possible, energy efficiency of equalizers should be high. Equalizers are categorized into two groups: dissipative and nondissipative equalizers. The latter ones are preferable from the viewpoint of efficiency, as discussed in the following sections.

Since SCs are expected to be used in long life applications, cell voltage equalizers for SCs should be designed considering that components used in equalizers gradually deteriorate, especially at harsh conditions in space, and parameter changes due to ageing are very likely. Parameter matching among components is strict requirement for some types of equalizers, and parameter mismatching results in insufficient equalization performance or even voltage imbalance caused by equalizers in the worst case. Hence, equalizers that do not require strict parameter matching are considered suitable for SCs in long life applications.

Another concern is poor variety of radiation-hardened (rad-hard) electrical components, especially ICs. Most nondissipative equalization techniques require feedback control, and control ICs. On the other hand, feedback control circuits in spacecrafts often designed using discrete components because of poor variety of rad-hard ICs. This not only complicate design and development procedures but also increase the component count, resulting in reduced reliability. Hence, equalizers operable without feedback control is desirable.

5.3 Review of Conventional Cell Voltage Equalizer

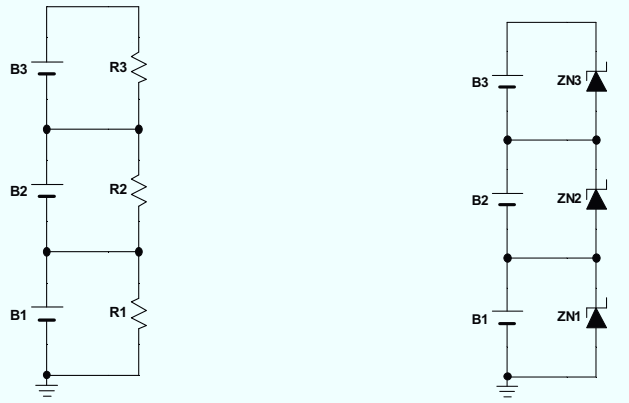
5.3.1 Dissipative Equalizer

The most common and traditional approach involves the use of dissipative equalizers, which do not require high-frequency switching operations. With dissipative equalizers, the voltage of series-connected cells can be equalized by removing stored energy or by shunting current from the cells with higher voltage. During the equalization process, the excess energy or current is dissipated in the form of heat, negatively influencing the thermal system of spacecrafts. Dissipative equalizers find advantages over nondissipative equalizers in terms of circuit simplicity and cost. The dissipative equalizers can be categorized into two groups: passive and active equalizers.

5.3.1.1 Passive Dissipative Equalizer

Fig. 5.3.1(a) shows the simplest solution, in which a passive resistor is connected to each cell resulting in a higher effective self-discharge rate. Cell voltage imbalance gradually decreases because of different effective self-discharge rate depending on cell voltage levels and resistance values. Although simple, relentless power loss in resistors reduces the energy efficiency of battery/module, depending on the effective self-discharge rate, and hence, this equalizer is rarely used in practical use.

Another concept of passive dissipative equalizer is to use Zener diodes, as shown in Fig. 5.3.1.(b). Cell voltages exceeding a Zener voltage level are cramped by Zener diodes operating as bypass circuits. The power loss in Zener diodes during rest period is negligibly low depending on leakage current of Zener diodes. However, Zener diodes must be chosen to be



(a) (b)

Fig. 5.3.1. Dissipative equalizers using (a) resistors and (b) Zener diodes.

capable of the largest possible charge current because the charge current flows to the Zener diode when the cell voltage reaches the Zener voltage level. In addition, a great temperature dependency of Zener voltage, which may not be acceptable in most applications, should be took into consideration.

5.3.1.2 Active Dissipative Equalizer (Shunting Equalizer)

Although dissipative equalization technologies seem less effective compared with nondissipative equalizers which are introduced in Section 5.3.2, the shunting equalizers are widely used in various applications, and a number of battery management ICs that include shunting equalizers are available because of their simplicity, modularity (or extendibility), and cost effectiveness.

Fig. 5.3.2 shows a schematic drawing of shunting equalizers connected to a two-series cell. Cell voltages are monitored and compared with a preset voltage level (shunt voltage level). When the cell voltage reaches or exceeds the shunt voltage level, the charge current is shunted through a transistor to reduce the net charge current. The product of cell voltage and shunt

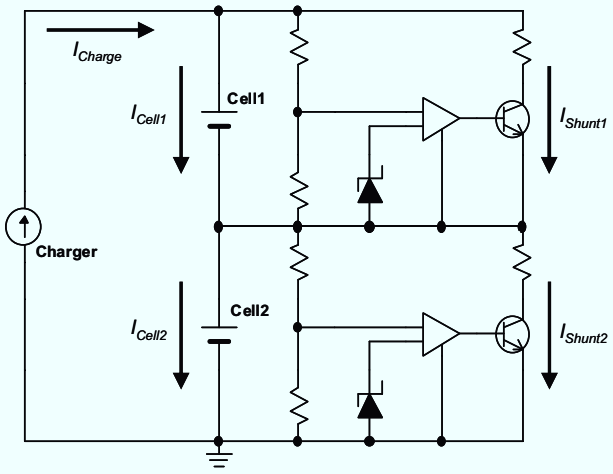


Fig. 5.3.2. Schematic drawing of shunting equalizer.

current, I_{Shunt}, is the power dissipation in the equalizer. Therefore, I_{Shunt} has a practical limitation from the viewpoints of efficiency and heat generation. Large I_{Shunt} makes thermal design and management difficult. To keep the power dissipation and heat generation at practical levels, shunting equalizers are generally designed capable of shunting only a part of the charge current, I_{Charge}. I_{Charge} is the sum of the net charge current, I_{Cell}, and the shunt current, I_{Shunt}, as expressed by

$$I_{Charge} = I_{Cell} + I_{Shunt} . \tag{5.1}$$

In most cases, when I_{Shunt} is set to be smaller than I_{Charge}, I_{Cell} continues to flow even after the cell voltage reaches the shunt voltage level. This leads to cell voltage overshoot above the shunt voltage level and the equalizer keeps drawing I_{Shunt} until the cell voltage falls below the shunt voltage level.

Fig. 5.3.3 shows an example charging profiles of an EDLC module consisting of two cells in series. EDLCs with capacitance of 100 F were charged with CC-CV charging scheme of 70 mA and 3.9 V (1.95 V/cell), and the shunt voltage level and shunt current were set to be 2.0 V and 30 mA, respectively. The cell voltages rose linearly during CC (Period A). When the voltage of Cell 2 reached the shunt voltage of 2.0 V (Period B), the equalizer for Cell 2 began shunting 30 mA of the 70 mA charge current. There was an inflection point observed in the module voltage at that moment. During Period B, Cell 2 was still being charged with 40 mA, so its voltage continued to increase, but its slope was gentler than during Period A. The change in the voltage slope of Cell 2 gave inflection points not only for Cell 2 but also for the module voltage. Thus, Cell 2 was overcharged above the shunt voltage level. On the other hand, Cell 1 was charged with 70 mA during both Period A and Period B.

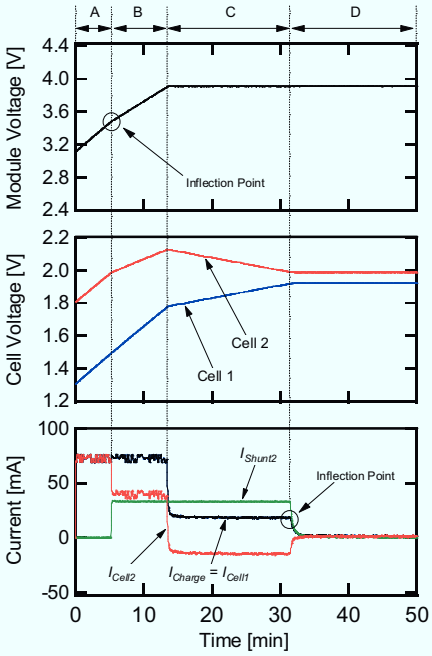


Fig. 5.3.3. Experimental charging profiles of two series EDLCs using shunting equalizers with a 30 mA shunt current.

The module voltage reached 3.9 V (1.95 V/cell), and the charger shifted from the CC to CV mode, during which the charge current was tapered (Period C). At that moment, the voltage of Cell 1 was less than 2.0 V, whereas Cell 2 was still overcharged, and thus, the equalizer continued shunting. I_{Shunt2} of 30 mA was still flowing, while the charger tapered I_{Charge}. According to (5.1), the currents of Cells 1 and 2 during Period C are

$$\begin{cases} I_{Charge} = I_{Cell1} & (Cell1) \\ I_{Charge} = I_{Cell2} + I_{Shunt2} & (Cell2) \end{cases}. \tag{5.2}$$

Therefore,

$$I_{Cell1} - I_{Cell2} = I_{Shunt2}. \tag{5.3}$$

Since the sum of the cell voltages was maintained at 3.9 V by the charger operating in CV mode, the voltage of Cell 1 increased while that of Cell 2 decreased. A decrease in the voltage of Cell 2 represents discharging, or a negative value of I_{Cell2}. In other words, Cell 2 started to discharge while the module itself was still being charged. In the case of EDLCs, I_{Cell1} and I_{Cell2} can be roughly determined by

$$I_{Cell} = C\frac{dV_{Cell}}{dt}, \tag{5.4}$$

where C is the capacitance and V_{Cell} is the cell voltage. The capacitances of Cells 1 and 2 were 100 F, and their voltage change should be equal because of the fixed voltage of 3.9 V applied by the charger. Therefore, from (5.3) and (5.4), I_{Cell1} and I_{Cell2} can be determined to be 15 and −15 mA, respectively.

When the voltage of Cell 2 reached a shunt voltage of 2.0 V, all currents began taper to 0 A

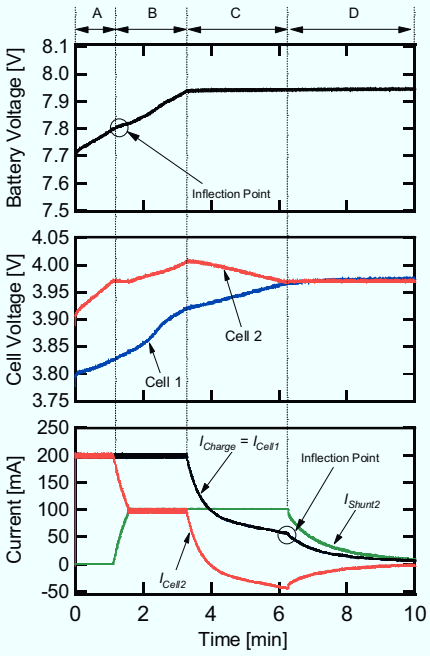


Fig. 5.3.4. Experimental charging profiles of two series LIB cells using shunting equalizers with a 100 mA shunt current.

during Period D. The equalizer no longer operated during this period, and therefore, I_{Shunt} should be zero. Equation (5.1) indicates that I_{Charge} equaled I_{Cell}, and was simply dominated by the charger. Tapering I_{Shunt2} provided an inflection point in I_{Charge}.

During Periods B and C, Cell 2 was temporarily overcharged above the shunt voltage level and the shunting equalizer operated. Note that the module voltage and charge current showed inflection points during the CC and CV periods, respectively. Technically, they occurred at the beginning and end of shunting. These inflection points originated from the overcharged cell. These results indicate that cell voltage imbalances might be detected by observing the module voltage and charge current profiles without measuring individual cell voltages.

Fig. 5.3.4 shows another example of charging profiles of LIB cells with capacity of 2.0 Ah that were charged with CC-CV charging scheme of 200 mA and 7.94 V (3.97 V/cell). Two cells were initially charged to 30% and 60% of SoC, and the shunt voltage level and shunt current were 3.975 V and 100 mA, respectively.

When Cell 2 reached the shunt voltage of 3.97 V, shunting of 100 mA of the 200 mA charge current began. During this shunting period, the voltage of Cell 2 continued increasing, because Cell 2 was charged substantially with 100 mA; thus, the voltage showed a gentler slope, while Cell 1 was still provided with 200 mA. The change in the voltage slope of Cell 2 provided inflection points not only for Cell 2 but also for the battery voltage.

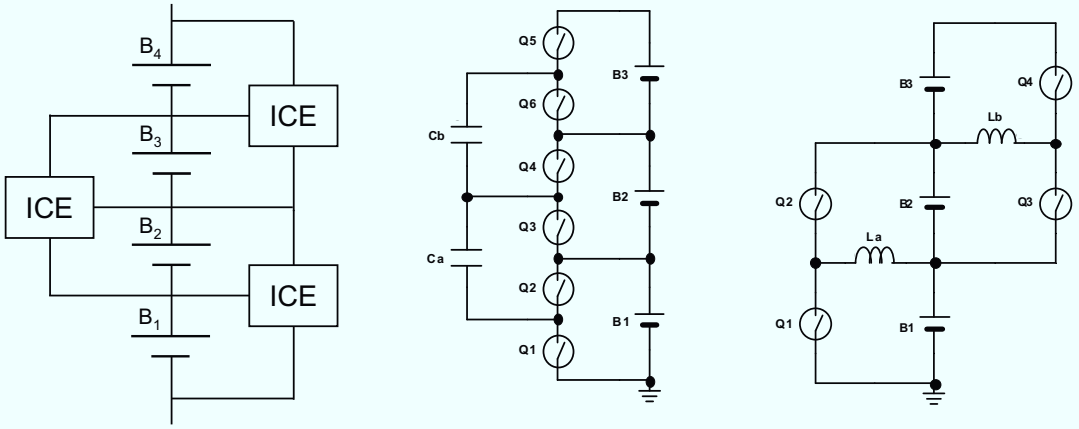
The charge current started tapering after the battery voltage reached 7.94 V. At that moment, the voltage of Cell 1 was less than 3.97 V. On the other hand, Cell 2 was overcharged that the shunt circuit should operate. The equalizer continued shunting 100 mA, while the charger continued tapering. After the charge current was tapered below the shunt current of 100 mA, the charge current of Cell 2 became negative, implying that Cell 2 started discharging substantially. Since the sum of the cell voltages was maintained at 7.94 V by the charger operating in CV mode, the voltage of Cell 1 increased while that of Cell 2 decreased. During this period, the charge current had to be tapered to a particular value determined by (5.3), so that the voltages of Cell 1 and 2 increased and decreased at the same rate. Cell 2 voltage decreased until it fell to a shunt voltage level of 3.975 V, and was followed by tapering to 0 A. An inflection point was observed in the charge current.

In the case of LIB cells, experimental profiles showed gentler curves than those of EDLCs because of their inherent nonlinear characteristics. Overall, interactive performance was analogous to that of the EDLCs, and the inflection points in the battery voltage and charge current were observed as well.

Most LIBs in spacecrafts use shunting equalizers. However, this equalizer needs as many switches, voltage sensors, and comparators proportional to the number of series connection of cells. In addition, this equalizer inevitably causes energy loss in the form of heat generation during equalization process, which may not only negatively influence the thermal system but also restrict operations due to the temperature rise. The operation flexibility is also poor because cells are equalized only during charging process, especially at fully charged states.

5.3.2 Nondissipative Equalizer

Nondissipative equalizers that transfer charges or energies of cells among cells are considered more suitable and promising than dissipative equalizers in terms of energy efficiency



(a) (b) (c)

Fig. 5.3.5. Schematic drawing of (a) individual cell equalizers, (b) switched capacitor-based equalizer, and (c) buck-boost converter-based equalizer.

and thermal management. In addition, nondissipative equalizers (including proposed equalizers) are usually operational during both charging and discharging, and hence, operation flexibility can be improved compared with dissipative equalizers. Numerous nondissipative equalization techniques have been proposed and demonstrated. Representative nondissipative equalizer topologies are presented in following sections.

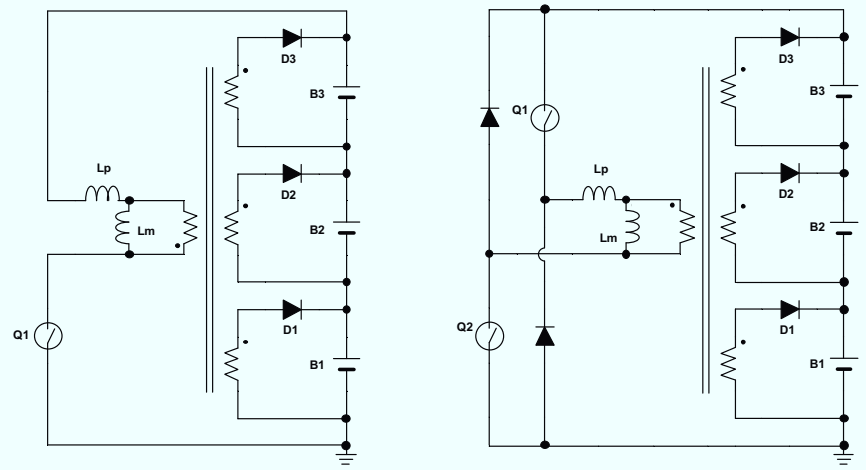
5.3.2.1 Individual Cell Equalizer

Fig. 5.3.5(a) depicts a schematic drawing of the individual cell equalizer (ICE). ICEs are typically based on individual dc–dc converters such as switched capacitor converters [1],[2] and buck-boost converters [3], as shown in Figs. 5.3.5(b) and (c), respectively. In these topologies, the charges or energies of the series-connected cells can be transferred between adjacent cells to eliminate cell voltage imbalance. The number of series connection of cells can be arbitrary extended by adding the number of ICEs.

Since these conventional topologies of ICEs are derived from multiple individual dc-dc converters, numerous switches, sensors, and switch drivers are required in proportion to the number of series-connected energy storage cells. Therefore, their circuit complexity and cost are prone to increase, and their reliability decreases as the number of series connection of cells increases. This is a serious concern not only in spacecraft applications but also vehicular applications where the reliability is of great importance.

5.3.2.2 Equalizer Using Multi-Winding Transformer

In cell voltage equalizers using a multi-winding transformer based on flyback converter and forward converter topologies, shown in Figs. 5.3.6(a) and (b), respectively, the energies of series-connected cells can be redistributed via a multi-winding transformer [4],[5] to the cell(s) having the lowest voltage. The number of switches required in the multi-winding transformer-based equalizers are significantly less than those required in ICE topologies. However, these topologies need a multi-winding transformer that must be customized



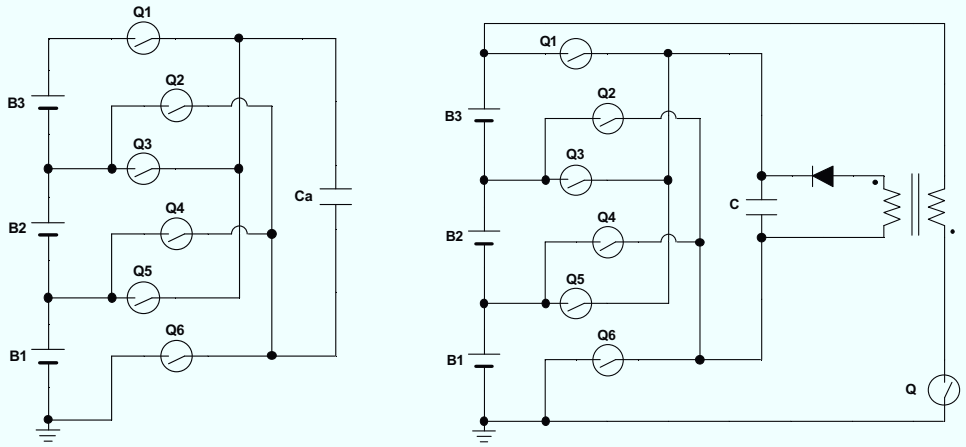
(a) (b)

Fig. 5.3.6. (a) Flyback converter- and (b) forward converter-based cell voltage equalizers using a multi-winding transformer.

depending on the number of series connections, and hence, the modularity is not good. In addition, since parameter mismatching among multiple secondary windings results in voltage imbalance that never be compensated by control, multi-winding transformers must be design and made with great care. Generally, the difficulty of parameter matching increases with the number of secondary windings. Therefore, their applications are usually limited to modules/batteries with small number of series connection.

5.3.2.3 Equalizer Using Single Converter with Selection Switches

Figs. 5.3.7(a) and (b) show equalizers using a single converter and selection switches based on flying capacitor converter and flyback converter, respectively. In these topologies, individual cell voltages are monitored, and the cell with the lowest voltages is determined using a



(a) (b)

Fig. 5.3.7. Equalizers using a single converter and selection switches based on (a) flying capacitor and (b) flyback converter.

microcontroller or DSP. In the flying capacitor-based equalizer, shown in Fig. 5.3.7(a), the energy of the cell with the highest voltage is delivered to the cell with the lowest voltage via the flying capacitor C_a by selecting proper switches. In the flyback converter-based equalizer, shown in Fig. 5.3.7(b), the energy of series-connected cells are redistributed to the cell with the lowest voltage via the flyback converter and selected switches.

These topologies can reduce the number of circuit components compared with ICE topologies, and do not need multi-winding transformer. However, the number of switches required is still large, and furthermore, microcontroller- or DSP-based management is mandatory because a target cell (i.e., a cell with the lowest voltage) must be determined for equalization to be implemented.

5.3.3 General Concerns and Drawbacks of Conventional Equalizers

Nondissipative equalizers, shown in Figs. 5.3.5, 5.3.6, and 5.3.7, operate at frequencies higher than several ten kilohertz and maintain cell voltage deviations below a desired level. However, because equalization processes of nondissipative topologies involve the exchange of charge or energy among energy storage cells, their charge-discharge profiles during equalization are much more complicated than conventional cycling profiles that are simply determined by loads. The cells are forced to be cycled within a conventional charge-discharge cycling period ranging from seconds to hours as well as at a high frequency that is equal to the operating frequency of the equalizers. In other words, the cells may be cycled at high frequency. Detailed concerns and discussion are made in the next section.

As mentioned in Chapter 2, the specific energy of SCs is lower than that of traditional secondary batteries, so an SC-based energy storage system may require a larger number of cells to be connected in series and/or parallel than LIB-based energy storage systems, although SCs have potentials to match or outperform the traditional batteries in terms of net specific energy for particular applications. In other words, the number of series connections of SCs is prone to be larger than that of LIBs. Hence, using multiple switches or transformer windings, which leads to increased cost and circuit complexity, is undesirable for an SC-based energy storage system. In addition, conventional topologies are undesirable from the viewpoint of reliability because of their complexity, since electrical circuits should be as simple as possible in order to mitigate risks of failure, especially for applications that require long-term use, i.e., SC-based energy storage systems.

5.4 High-Frequency Charge-Discharge Cycling Induced by Cell Equalizer

5.4.1 Cause of High-Frequency Charge-Discharge Cycling

Fig. 5.4.1 shows a schematic of a battery pack composed of n cells connected in series with cell voltage equalizers that have two switching states: (a) state A and (b) state B. The battery pack is connected to an external circuit (i.e., a charger or load) and the direction of $I_{Battery}$ designated in Fig. 5.4.1 gives the charging direction. Series-connected cells B_1, …, B_n are charged or discharged with current $I_{Battery}$, which is positive and negative for charging and discharging, respectively. The equalizers exchange charges or energies of B_1, …, B_n among themselves in the form of equalization currents $I_{eq1\text{-}A}$, …, $I_{eqn\text{-}A}$ and $I_{eq1\text{-}B}$, …, $I_{eqn\text{-}B}$ during states A and B, respectively. Therefore, currents $I_{B1\text{-}A}$, …, $I_{Bn\text{-}A}$ and $I_{B1\text{-}B}$, …, $I_{Bn\text{-}B}$, that flow through B_1,

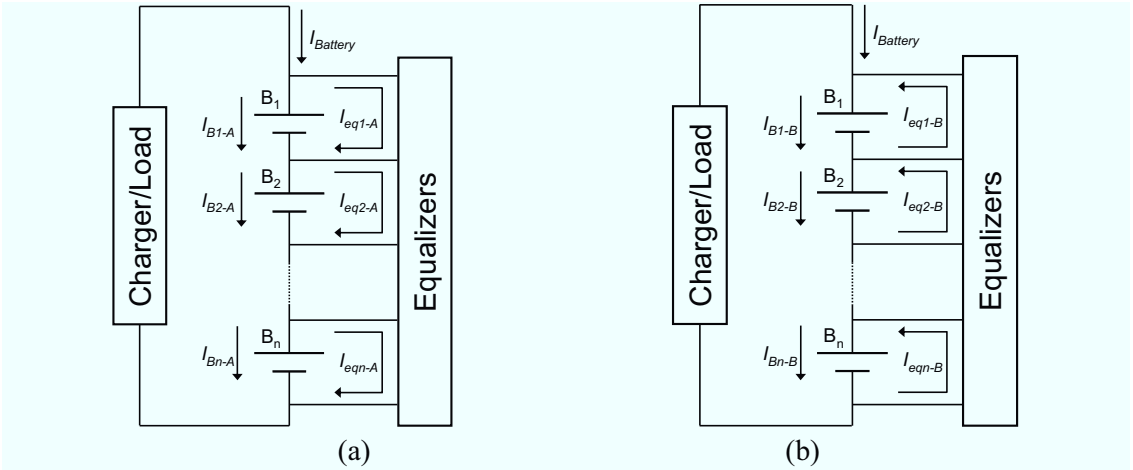


Fig. 5.4.1. Schematic drawing of a battery comprising *n* cells connected in series with cell equalizers in (a) state A and (b) state B.

…, B_n during states A and B are different from $I_{Battery}$. Currents $I_{eq1\text{-}A}$, …, $I_{eqn\text{-}A}$ and $I_{eq1\text{-}B}$, …, $I_{eqn\text{-}B}$, which depend on the voltage imbalance of B_1, …, B_n, can be positive or negative. States A and B alternate with each other at high frequency because of the switching operation of the equalizers. Currents $I_{Bn\text{-}A}$ and $I_{Bn\text{-}B}$ can be expressed as

$$I_{Bn-A} = I_{Battery} - I_{eqn-A}, \tag{5.5}$$

$$I_{Bn-B} = I_{Battery} + I_{eqn-B}. \tag{5.6}$$

As long as $I_{Bn\text{-}A}$ and $I_{Bn\text{-}B}$ are in the same direction, B_n is simply being charged or discharged. However, if the currents in states A and B are not in the same direction, charge-discharge cycling occurs while the battery pack itself is simply being charged or discharged. Because states A and B alternate at high frequency, usually around several ten kilohertz, cells can be pulsated, resulting in a high-frequency cycling.

An example of an experimental equalization process is shown to provide a qualitative understanding of how the high-frequency charge-discharge cycling occurs during the equalization process. Switched-capacitor-based equalizers are widely used for not only LIB cells but also SCs because of their circuit simplicity, modularity, and ease of control [1]–[2]. A switched capacitor equalizer was used as a representative of nondissipative cell voltage equalizers. Fig. 5.4.2 shows a battery pack consisting of three cells B_1–B_3 in series with switched capacitor equalizers, and an external circuit (i.e., a charger or load) is also connected to the battery pack. Fundamental operations without charge-discharge currents from/to the external circuit are demonstrated experimentally. Odd- and even-numbered switches are alternately turned-on and -off to transfer the charges of B_1–B_3 via energy-transfer capacitors C_a and C_b. As shown in Fig. 5.4.3(a), B_1 and B_2 are connected to C_a and C_b via odd-numbered switches in state A. In state B shown in Fig. 5.4.3(b), even-numbered switches are turned-on to connect B_2 and B_3 to C_a and C_b. Thus, B_1–B_3 in the battery pack can exchange their charges via capacitors C_a and C_b.

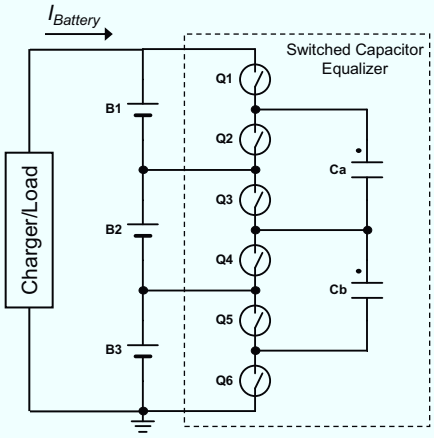


Fig. 5.4.2. Switched capacitor equalizer for a battery pack consisting of three cells connected in series.

LIB cells with a capacity of 2.0 Ah, which will also be used for life performance tests in Section 5.4.2.1, were used for the equalization experiment. B_1–B_3 with initial voltages of 4.2, 4.0, and 3.8 V, respectively, were equalized by 440 μF Al electrolytic capacitors of C_a and C_b at a switching frequency of 10 kHz. MOSFETs with 4 mΩ on-resistance were used for Q_1–Q_6. Odd- and even-numbered switches were alternately turned-on and -off with a fixed duty cycle of 45% and 5% dead time between each state to avoid any possibility of short-through current. There was neither charge nor discharge currents (i.e., $I_{Battery}$ = 0 in Fig. 5.4.1) from/to the external circuit.

Cell voltage profiles and current waveforms 2 h after the start of equalization are shown in Fig. 5.4.4. In the equalization process, the cell with the higher voltage acts as a source and the cell with the lower voltage acts as a load. In other words, B_1, the cell with the highest initial voltage, "gives" its charge to the other cells, while B_3, the cell with the lowest initial voltage, "receives" charges from the other cells. The current I_{B1} was negative (i.e., discharging) in state A and gave its charge to C_a. In state B, the charge given by B_1 in state A was transferred from C_a to B_2. Thus, B_2 showed a positive current (i.e., charging) and the integral of I_{B2} over the duration of state B corresponded to the charge delivered from C_a. During state A, on the other

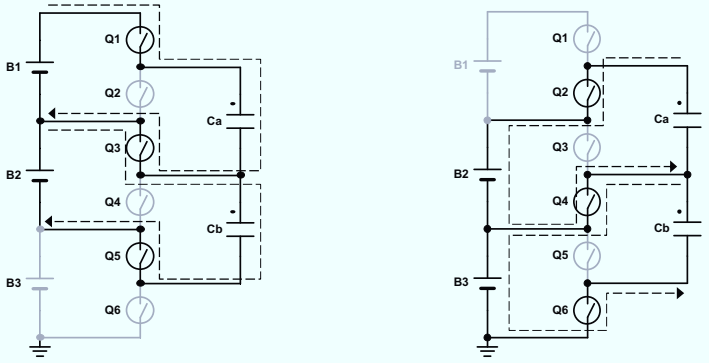
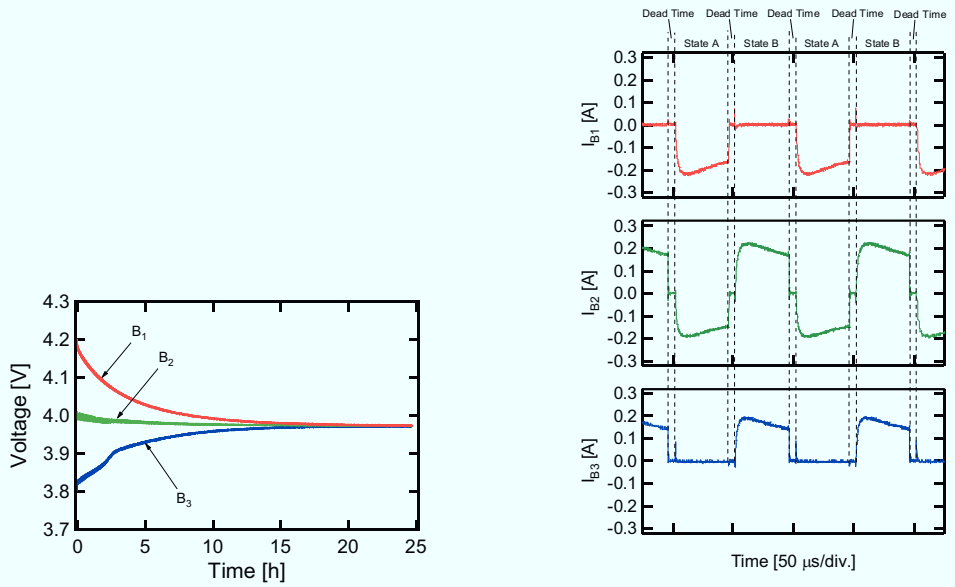


Fig. 5.4.3. Switching states of a switched capacitor equalizer, (a) state A and (b) state B.



(a) (b)

Fig. 5.4.4. Experimental equalization using switched capacitor equalizers. (a) equalization profiles and (b) current waveforms 2 h after the start of equalization.

hand, B_2 showed a negative current (i.e., discharging) because it gave its charge to C_b. B_3 during state B showed a positive current and it received the charge from C_b. These current waveforms demonstrated that B_2, which served as a path for charge traveling from B_1 to B_3, was cycled at a high frequency of 10 kHz, whereas B_1 and B_3 were discharged and charged only during state A and B, respectively. Ultimately, the cell voltages of B_1–B_3 converged to approximately 3.97 V.

In the equalization example shown in Fig. 5.4.4, no external circuit such as a charger or load was present, so that the battery pack itself was neither charged nor discharged, although the cells were charged and discharged each other throughout the equalization process. This example corresponded to $I_{Battery} = 0$ in (5.5) and (5.6), and only B_2 was cycled at high frequency. However, during the charging/discharging of the battery pack, the charging/discharging currents from/to the external circuit could be superimposed on the equalization current profiles that were shown in Fig. 5.4.4(b). According to (5.5) and (5.6), with a charger or load, not only B_2 but also B_1 (B_3) could be cycled at high frequency during the charging (discharging) of the battery pack. For example, if the battery pack had been charged at $0 \leq I_{Battery} \leq 0.2$ A, not only B_2 but also B_1 would have been cycled at high frequency. On the other hand, if the battery pack had been discharged at $-0.2 \leq I_{Battery} \leq 0$ A, B_2 and B_3 would have been cycled at high frequency.

The above experimental example indicated that the equalization process possibly induces high-frequency cycling. Because the frequencies of such cyclings are equal to the equalizer's operating frequency, which is usually around several ten kilohertz, a very large number of cycles with very shallow depth of discharge is induced. In general, cycling is one of the major causes of cell degradation, so these shallow high-frequency cyclings are considered to negatively impact the life performance of LIB cells and SCs.

5.4.2 High-Frequency Cycling Experiment

5.4.2.1 High-Frequency Cycling Conditions

To investigate the qualitative influence of high-frequency cycling on life performance of LIB cells, commercially available 2-Ah prismatic LIB cells (UF103450P, SANYO) were cycled at high frequency by bipolar power sources. The cells use lithium cobalt oxide ($LiCoO_2$) for the positive electrode (the most prevalent active material for the positive electrode of lithium-ion cells in consumer electronics application) and graphite for the negative electrode. The experimental setup and charge-discharge profiles are shown in Fig. 5.4.5. An equalization current rate of approximately C/100, which is considered sufficient to overcome the charging current during float charging, is used for lead-acid cells and is also considered to be appropriate for lithium-ion cells [2],[6]. In this study, to accelerate and clarify the dependence of cycle frequency on cell degradation, a charge-discharge current of 1.0 A (C/2 rate), which is large as the equalization current, was used. The charge-discharge current was determined by the voltage across a 1-Ω resistor. Life performance was evaluated for average cell voltages of 4.2 and 3.8 V, so that the output voltage of the bipolar power source was set to be a square waveform with a peak-to-peak voltage of 2.0 V, i.e., 5.2–3.2 V for 4.2 V cycling and 4.8–2.8 V for 3.8 V cycling.

In the frequency range from 1 Hz to 100 kHz, the cells were cycled for every decade at room temperature. The duty ratio of the charge and discharge periods was 50%. Because the output voltage of the bipolar power sources was fixed-square waveform of 5.2–3.2 or 4.8–2.8 V, the average of the sum of the cell voltage and the voltage across the 1-Ω resistor was 4.2 or 3.8 V. For long-term experiments on LIB cells, coulombic efficiency and self-discharge had been anticipated to cause cell voltage decline. To eliminate the influence of cell voltage decline due to these two factors on the life performance of the cells, the average cell voltages had to be held constant at 4.2 or 3.8 V during high-frequency cycling. Generally, LIB cells offer nearly 100% coulombic efficiency (99.8% for the cells used in this study), and hence, the charge and discharge currents were regarded as identical because the charge and discharge periods were essentially equal. Therefore, the average voltage across the 1-Ω resistor during cycling was almost zero, and the average cell voltage could be maintained at 4.2 or 3.8 V. Thus, cell voltage decline due to coulombic efficiency and self-discharge was prevented in this experiment.

Float charging tests were also performed to obtain calendar degradation trends as baseline data. To evaluate life performance, capacity measurements were periodically performed with a constant current–constant voltage (CC–CV) charging of 1880 mA, 4.2 V for 2.5 h and a CC discharging current of 376 mA. Two cells were assigned for each test condition, and the average values of the measured capacities were used for analyses and discussion.

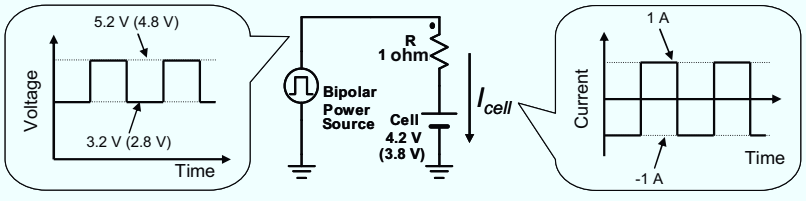


Fig. 5.4.5. Experimental setup and charge-discharge profiles for high-frequency cycling tests.

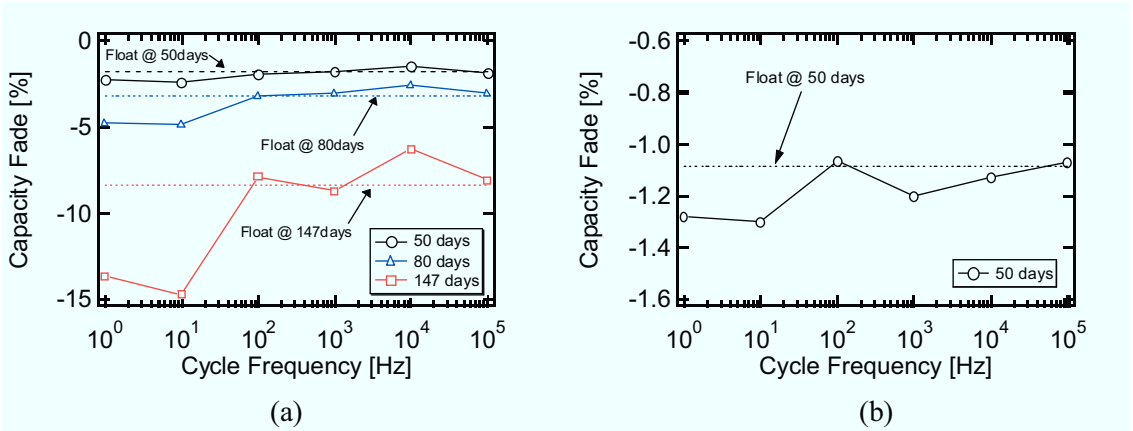


Fig. 5.4.6. Capacity fade versus cycle frequency for average voltages (a) 4.2 V and (b) 3.8 V.

5.4.2.2 Resultant Capacity Retention Trends

Figs. 5.4.6(a) and (b) show the capacity fade trend versus cycle frequency for average cell voltages of 4.2 and 3.8 V, respectively. Capacity fade ratios of the LIB cells under float charging conditions are indicated as dashed lines. Cells cycled at an average voltage of 4.2 V showed a greater capacity fade tendency than those cycled at 3.8 V because cell degradation is generally accelerated at higher voltages [7]. However, analogous degradation trends were observed for both average voltage conditions. The capacity fade ratios were significant at frequencies below 10 Hz. Cells cycled above 100 Hz, on the other hand, showed the almost identical degradation trends as those tested at the float charging conditions under which the capacity fade ratio reflected calendar degradations only. These trends indicated that the calendar degradations were dominant at high frequency ranges even though the cells were cycled. At low frequency ranges, on the other hand, cycling also played a major role in deteriorating the capacity retention.

In general, LIB cells have their own time constants, which are determined by the double-layer capacitance and charge-transfer resistance in both the anode and cathode. Because the cycle periods of high-frequency cycling are significantly shorter than those of conventional cycling, analyzing frequency-dependence of current response and distribution in the cells was inferred as a clue to reveal frequency-dependent degradation trends. In fact, previous studies on lead-acid batteries reported that high-frequency current components only charge and discharge double-layer capacitances and do not allow time for ionic diffusion to occur to a significant degree, whereas ionic diffusion is fully operative at low frequencies [8],[9].

The major role of equalizers is to equalize cell voltage to prolong the life of cells. Therefore, degradation due to the equalizers must be avoided. The results obtained here suggest that cell voltage equalizers should operate at particular frequencies at which equalizers do not negatively influence the life performance of cells. The experimental results shown above are expected to be valuable to electrical researchers and engineers for designing effective cell equalizers. To apply such information in circuit designs, further analysis was required to reveal the major factors that degraded the cells. To address this issue, Section 5.4.3 focuses on comparing experiment and simulation to determine the frequency-dependent internal factors that affected the life of cells, including the double-layer capacitance and charge-transfer resistance.

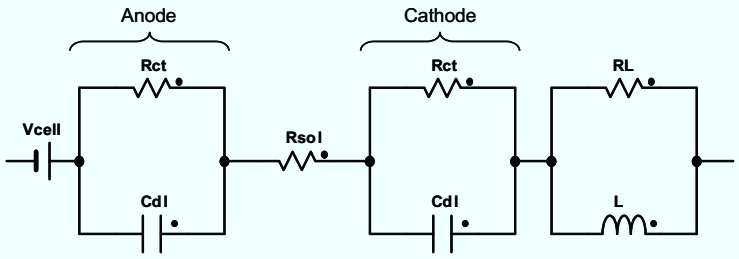


Fig. 5.4.7. Equivalent circuit of a lithium-ion cell for simulation analysis.

5.4.3 High-Frequency Cycling Simulation Analysis

5.4.3.1 Equivalent Circuit Modeling

The product of double-layer capacitance C_{dl} and charge-transfer resistance R_{ct} forms a time constant, and the current response and distribution of these components depend on frequency. The internal behavior of cells was evaluated by simulation analyses. To model a simulation circuit, an ac impedance of a fresh cell was measured to obtain equivalent circuit parameters. The impedance was measured over a frequency range from 10 mHz to 100 kHz with an amplitude of 5 mV by using an impedance analyzer (PARSTAT 2263, Princeton Applied Research).

Fig. 5.4.7 shows an equivalent circuit consisting of ideal elements; V_{cell}, R_{sol}, L, and R_L are the electromotive force, electrolyte resistance, inductance, and resistance in parallel with the inductance, respectively. A measured Nyquist plot was fitted to the equivalent circuit by using impedance analysis software (ZSimpWin™, Princeton Applied Research). To facilitate an equivalent circuit-based simulation, a constant-phase element (CPE) [10], which reflects a depressed semicircle of a Nyquist plot, was not employed. Warburg impedance, which is dominant at very low frequencies, was excluded. The inductance component originating from a connection cable used for the high-frequency cycling tests, and geometry of electrodes and current collectors, was included because inductive behavior was not negligible at high

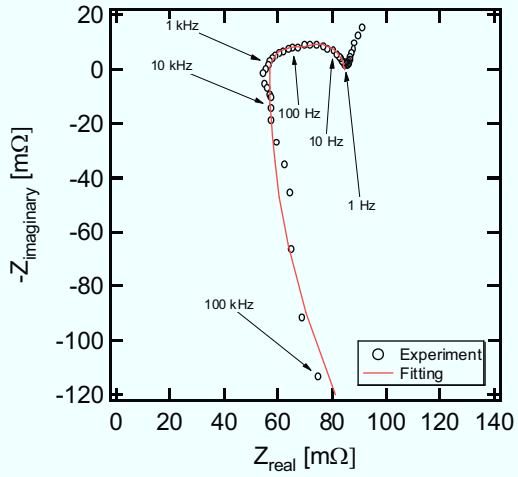


Fig. 5.4.8. Experimental Nyquist plot and corresponding fitting curve of a fresh cell.

Table 5.1. Equivalent circuit parameters obtained by fitting to an experimental Nyquist plot of the fresh cell

Parameter	Value
R_{sol} (mΩ)	56.85
R_{ct_anode} (mΩ)	12.41
C_{dl_anode} (mF)	82.41
τ_{anode} (ms)	1.02
$R_{ct\_cathode}$ (mΩ)	15.22
$C_{dl\_cathode}$ (mF)	580.3
$\tau_{cathode}$ (ms)	8.87
L (nH)	202.6
R_L (mΩ)	612.3

frequencies.

Fig. 5.4.8 shows the experimental Nyquist plot and a fitting curve of the fresh cell. Despite the absence of a CPE, the fitting curve agreed with the experimental result. Circuit parameters obtained from the fitting are shown in Table 5.1; τ_{anode} and $\tau_{cathode}$ are the anode and cathode time constants obtained by multiplying C_{dl_anode} and R_{ct_anode}, and $C_{dl\_cathode}$ and $R_{ct\_cathode}$, respectively. The cathode is well known to be the major source of cell impedance [11]–[13], and therefore, the larger time constant was assigned to the cathode impedance. A time constant can be regarded as an index of response time in terms of voltage and current; the smaller the time constant, the quicker the cell responds. The impedance of the connection cable was measured separately, and the inductive impedance in Fig. 5.4.8 was found to originate mainly from the connection cable.

Fig. 5.4.9 shows a trend of measured Nyquist plots and fitting curves of a cell cycled at 1 Hz as representative data. With the aging of the cell, the intersection point on the x-axis, which reflects R_{sol} in the equivalent circuit, consistently shifted to the right and increased by approximately 12%. Although the increase in R_{sol} insignificantly leads to a decrease in the charge-discharge current determined by the 1-Ω resistor shown in Fig. 5.4.5, the response characteristics, such as the response time and current distribution to C_{dl} and R_{ct}, are not affected by the increase of R_{sol} because the response characteristics are determined by time constants of τ_{anode} and $\tau_{cathode}$. τ_{anode} and $\tau_{cathode}$ of the aged cell were determined by fitting the experimental

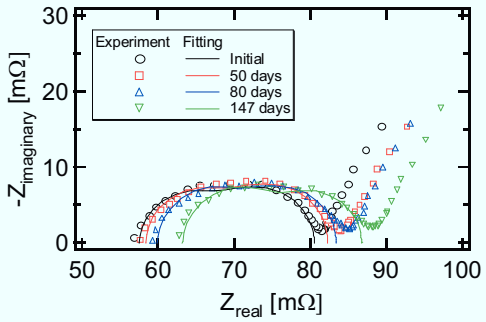


Fig. 5.4.9. Trend of measured Nyquist plots and fitting curves of the cell cycled at 1 Hz.

Nyquist plots shown in Fig. 5.4.9. Consistent changes in τ_{anode} and $\tau_{cathode}$ were not observed—they remained within ±20% (depending on accuracy of fitting) of their initial values. In the high-frequency cycling test, the frequency varied in a six figure (i.e., from 1 Hz to 100 kHz) while the changes in τ_{anode} and $\tau_{cathode}$ were within ±20%. Therefore, the impedance change due to the cell aging was considered not to have significant impacts on the overall trend of current response and distribution. Thus, for the sake of simplicity, the parameters of the fresh cell shown in Table 5.1 were used for the following simulation analyses.

5.4.3.2 Correlation between Degradation Trends and Current Distribution

Current response and distribution inside the cell were simulated using circuit simulation software (SCAT K.488, Keisoku Giken). The simulation circuit shown in Fig. 5.4.7 was cycled under the same conditions as the actual experiments, as described in Section III.

Cell voltage and current waveforms of each element at a cycle frequency of 10 kHz are shown in Fig. 5.4.10. Experimental waveforms measured during the cycle test are also presented as reference data. I_{sol}, I_{anode}, and $I_{cathode}$ are currents flowing through R_{sol}, anode components, and cathode components, respectively. Experimental and simulation waveforms were in good agreement with respect to cell voltage, showing overshoot behavior due to the inductive component. Because the impedance of the capacitor tended to be small at high frequencies, the charge-discharge current flowed primarily through C_{dl} at the high frequency condition of 10 kHz. Thus, current waveforms of I_{anode} and $I_{cathode}$ of C_{dl} showed almost identical to that of I_{sol}, whereas those of R_{ct} were nearly zero.

Thus, the high-frequency charge-discharge current was buffered by C_{dl}, and little current flowed through R_{ct}. This result can be interpreted that there was little substantial charge-transfer

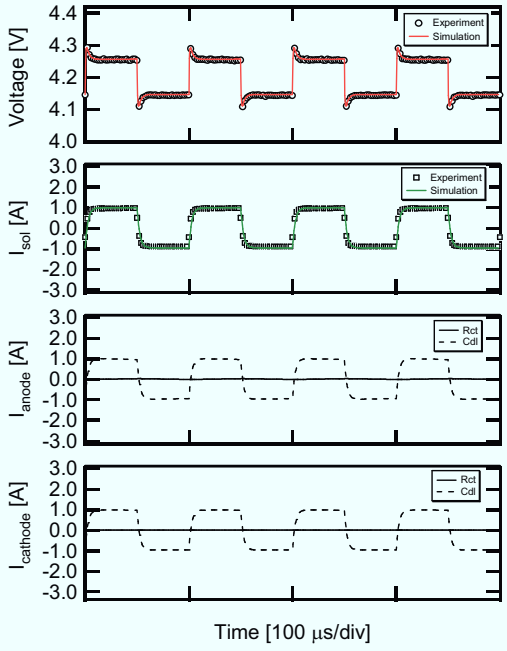


Fig. 5.4.10. Experimental and simulation waveforms of cell voltage, I_{sol}, I_{anode}, and $I_{cathode}$ at a cycle frequency of 10 kHz.

process indicating little cell reaction. Therefore, the current was used only for charging and discharging C_{dl} in the high-frequency region. In other words, the current direction was reversed before the charge-transfer process occurred at high cycle-frequency conditions.

Fig. 5.4.11 shows experimental and simulation waveforms at a cycle frequency of 10 Hz. Contrary to the case shown in Fig. 5.4.10, I_{anode} and $I_{cathode}$ of R_{ct} were dominant because the impedance of C_{dl} at the low frequency of 10 Hz was large, and the cell voltage waveform showed a capacitive response. When the current direction was reversed, a large current flowed to charge or discharge C_{dl}. Once C_{dl} was appreciably charged or discharged, the current of R_{ct} took over and dominated the total current. This result corresponded to the general fact that a high-frequency current component, such as at the beginning of pulse, is assigned to charge or discharge C_{dl}, and subsequently, a current associated to electrochemical-reaction (i.e., a current through R_{ct}) dominates [14],[15]. Previous studies regarding to the lead-acid batteries also reported the same tendency that the double-layer capacitance does not allow cell reactions to occur at high frequencies while the cell reaction processes become substantial at relatively low frequencies [8],[9]. The low cycle-frequency condition was considered to provide sufficient time for the charge-transfer process (i.e., the cell reaction) to occur. The cathode responded slower because $\tau_{cathode} > \tau_{anode}$, as shown in Table 5.1.

Fig. 5.4.12 shows the frequency dependence of root-mean-square (RMS) currents distributing to R_{ct} and C_{dl} in the anode and cathode during the high-frequency cycling. An explicit correlation between the degradation trends shown in Fig. 5.4.6(a) and the current distribution shown in Fig. 5.4.12 was found. Cells cycled at low frequencies, where the cycle periods were sufficiently longer than the time constants (τ_{anode} and $\tau_{cathode}$) and the current flowing through R_{ct} was dominant, degraded significantly, whereas the degradation of cells cycled at high

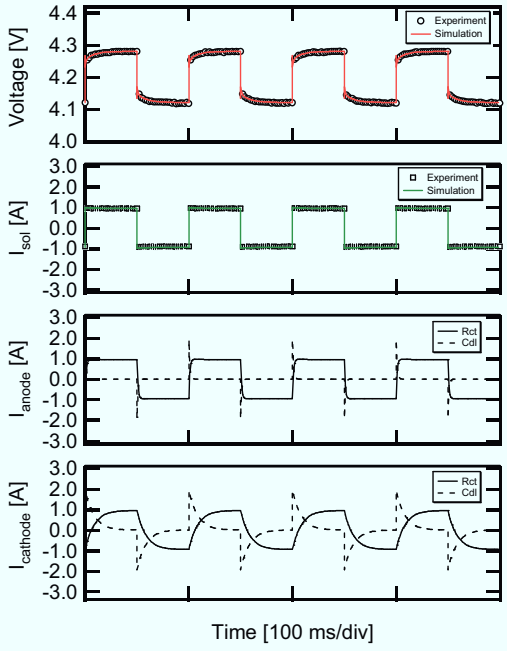


Fig. 5.4.11. Experimental and simulation waveforms of cell voltage, I_{sol}, I_{anode}, and $I_{cathode}$ at a cycle frequency of 10 Hz.

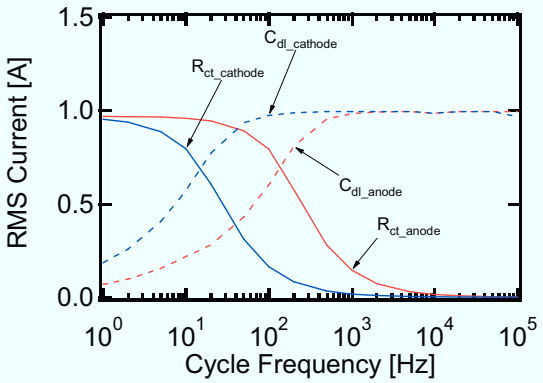


Fig. 5.4.12. Frequency dependence of RMS currents distributing to C_{dl} and R_{ct} in the anode and cathode during high-frequency cycling.

frequencies, where the cycle periods were sufficiently shorter than the time constants and the charging-discharging of C_{dl} dominated, was identical to the calendar degradation.

In general, cells during cycling deteriorate with side reactions, such as growth of passivation layers or deposition of Li on the electrodes [16], and these side reactions accompany the cell reaction or charge-transfer process. In other words, no degradation accompanying the cycling occurs unless current flows through R_{ct}. In addition, because the charging and discharging of C_{dl} represent the polarization of an electrode-electrolyte interface [17], the current flowing through C_{dl} causes neither an electrochemical reaction nor electrochemical degradation, which can be understood by the general fact that EDLCs which utilize their double-layer capacitance as energy storage resources, offer inherent outstanding life performance.

The correlation between Fig. 5.4.6(a) and Fig. 5.4.12 implied that the significant degradation at low frequencies was caused by not only calendar degradation but also degradation due to the side reactions accompanying the cell reactions. At high frequencies, on the other hand, the current was used only for cycling C_{dl}, and there was little current flowing through R_{ct}, i.e., insignificant cell reactions. Therefore, the degradations at high frequencies were almost identical to the calendar degradations. This correlation also implies that high-frequency cycling has no negative impact on life performance of SCs because SCs basically do not contain R_{ct} and no electrochemical reactions take place essentially in SCs.

In particular, the cathode charge-transfer that was dominant at frequencies below 10 Hz was directly correlated to the capacity fade trends. Previous studies have revealed that the major sources of cell degradation, such as capacity fade and impedance increase, mainly originate from the cathode [18]–[21]. The significant capacity fade at low frequencies was considered to originate from cathode degradation. Further investigation based on the electrochemical approach is necessary to elucidate the degradation mechanism, which is beyond the scope of this study.

5.4.4 Conclusions

Series-connected energy storage cells with nondissipative cell voltage equalizers, which allow cells to exchange their charges among themselves, exhibit complicated charging and

discharging profiles. An equalization experiment using switched capacitor equalizers provided qualitative understanding that high-frequency charge-discharge cycling can be imposed on cells during the equalization process.

LIB cells were cycled at frequencies ranging from 1 Hz to 100 kHz to investigate the qualitative influence of high-frequency cycling on the life performance of the cells. Cells cycled at high frequencies above 100 Hz showed only calendar degradation trends, whereas those cycled at low frequencies below 10 Hz deteriorated significantly.

The frequency dependence of the current response and distribution inside the LIB cells was analyzed on the basis of equivalent circuit simulations. Simulation analyses revealed that there was little current flowing through the charge-transfer resistance R_{ct} at high frequencies because the charge-discharge current was buffered by the double-layer capacitance C_{dl}, while the current through R_{ct} dominated at low frequencies. A correlation between the degradation trend and the current distribution of C_{dl} and R_{ct} was observed and implied that the significant degradation at low frequencies, where the cycle period was sufficiently longer than the time constants of the cells, was caused by not only calendar degradation but also side reactions accompanying the charge-transfer process (i.e., the cell reaction). On the other hand, at high frequencies, where the cycle period was sufficiently shorter than the time constants of the cells, the charge-discharge current was used only for cycling C_{dl}, and therefore, degradations were identical to the calendar degradation. The obtained correlation implies that high-frequency cycling has no negative impact on SC life performance, since no electrochemical reactions take place in SCs and R_{ct} does not basically exist.

The experimental degradation trends obtained in this study suggest that equalizers for LIB cells desirably operate in a proper frequency range in which the life performance of the LIB cells is not affected by the high-frequency equalization current. Cell voltage equalizers for LIBs can be designed appropriately by taking the time constants of LIB cells into account so that the switching period of the equalizer should be shorter enough than the time constants of the LIB cells.

5.4 Series-Parallel Reconfigurable Cell Equalizer

5.5.1 Circuit Description and Operation Principle

An example of the proposed equalization circuit is shown in Fig. 5.5.1. Three strings A, B, and C, consisting of SCs C_{1A}–C_{2A}, C_{1B}–C_{3B}, and C_{2C}–C_{3C}, are connected in parallel via two groups of switches, S_a and S_b. Capacitances of C_{1B} and C_{3B} (capacitances of 2C) are two times those of others (capacitances of 1C).

Two groups of switches are alternately turned on or off, as shown in Fig. 5.5.2. Connection combinations of the SCs are switched alternately with setting dead time to avoid any possibility of creating a short circuit. Fig. 5.5.3 shows two switching states in the series–parallel connected equalizers. SCs charge or discharge each other in each parallel circuit to maintain uniform cell voltages. There are two parallel-connected SCs in the top and bottom parallel circuits, whereas there are three in the center. However, the total capacitance of each parallel circuit is 3C because the capacitances of C_{1B} and C_{3B} are two times those of the others. Therefore, the total capacitance of each parallel circuit is maintained at 3C (from top to bottom, C + 2C, C + C + C, and 2C + C) during both switching states, whereas the number of parallel connections of each

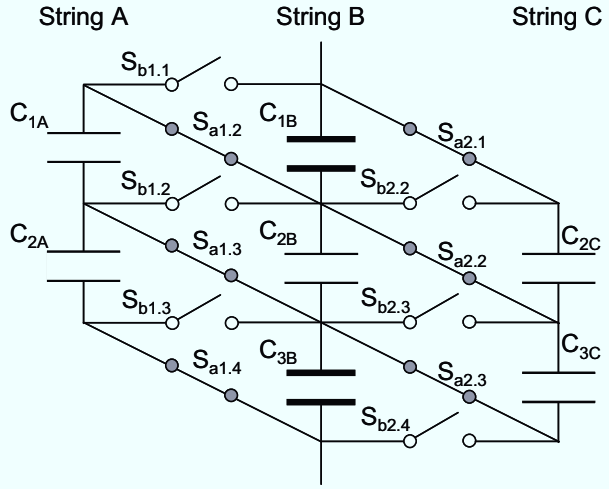


Fig. 5.5.1. Series–parallel reconfigurable equalization circuit.

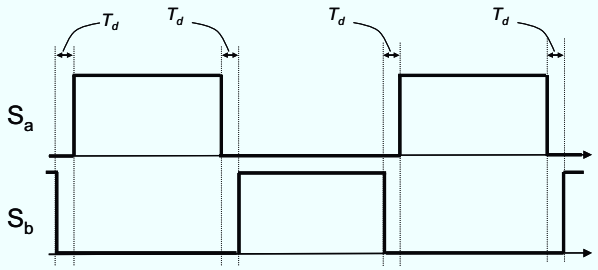
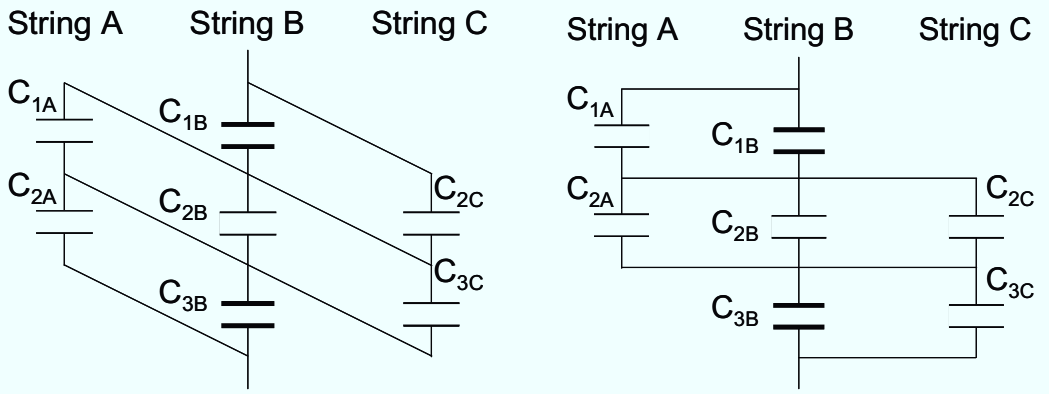


Fig. 5.5.2. Switching sequence.

parallel circuit is different. No voltage imbalance occurs because of the uniform total capacitance of each parallel circuit during the charging/discharging process.

The SCs shown in Fig. 5.5.1 are utilized not only for energy storage but also for equalization. The equalizers, whose main circuits consist only of the SCs and switches, require neither closed-loop control nor sensing; therefore, the system can reduce the number of components and circuit complexity. In addition, the equalizers are easily extended to an arbitrary number of series or parallel connections to form high-energy storage systems, providing good modularity. Since this equalizer essentially consists of three SC strings in parallel, and therefore, this equalizer is considered suitable for multi-string applications where relatively large energy and power are required.

The proposed circuit can provide very efficient equalization. Since the capacitance of an SC is quite large, its voltage does not vary quickly as compared with electrolytic capacitors. This means that the switching frequency can be lowered to reduce loss due to charging/discharging of the input capacitance of MOSFET switches. The loss is proportional to the switching frequency and can be negligible even at light loads because of a low operating frequency. As long as the voltages of SCs are well balanced, all the switches can be normally turned on/off at zero voltage conditions. When the voltages of SCs are uniform, there is no current flowing through the switches except for the charging/discharging current paths ($S_{a1.2}$, $S_{a1.4}$, $S_{a2.1}$, $S_{a2.3}$, $S_{b1.1}$, $S_{b1.3}$, $S_{b2.2}$, and $S_{b2.4}$), so that the equalization loss is minimum.



(a) (b)

Fig. 5.5.3. Switching states of the series–parallel reconfigurable equalizers during (a) state A and (b) state B.

5.5.2 Operation Analysis

An equivalent circuit for series–parallel connected equalizers consisting of two SCs is shown in Fig. 5.5.4. The SCs in Cells 1 and 2, with voltages of V_1 and V_2, are connected in parallel when the switches S_1 and S_2 with on-resistances of R_1 and R_2, respectively, are turned on. C_1–C_2 and r_1–r_2 are the capacitances and internal resistances of SCs, respectively. The total stored energy before equalization E_{before} is expressed as

$$E_{before} = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 . \tag{5.7}$$

Voltages of SCs after equalization are

$$V_{after} = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} . \tag{5.8}$$

The total stored energy after equalization E_{after} is therefore expressed as

$$E_{after} = \frac{1}{2}(C_1 + C_2)\left(\frac{C_1V_2 + C_2V_2}{C_1 + C_2}\right)^2 . \tag{5.9}$$

The equalization loss E_{loss} is given by

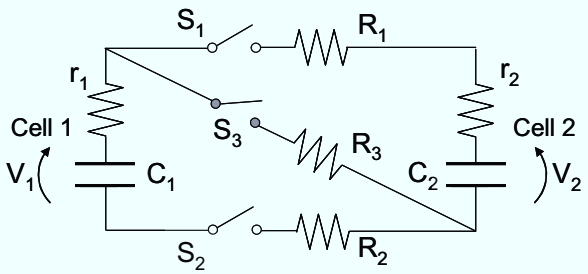


Fig. 5.5.4. Equivalent circuit for series—parallel connected equalizers consisting of two SCs.

$$E_{loss} = E_{before} - E_{after} = \frac{C_1 C_2 (V_1 - V_2)^2}{2(C_1 + C_2)}. \tag{5.10}$$

Thus, E_{loss} is proportional to the square of the voltage difference $V_1 - V_2$, which should be minimized as much as possible for achieving efficient equalization. Resistance only affects current and equalization time, not E_{loss} [22]. Individual differences in the SCs always cause voltage differences more or less during charging and discharging. Here, the voltage difference is always assumed to be zero after every switching. When Cells 1 and 2 are charged with current I for t_{on} (50% duty ratio) when S_3 is turned on, the voltage difference is

$$V_1 - V_2 = It_{on}\left(\frac{1}{C_1} - \frac{1}{C_2}\right) = \frac{I}{f}\left(\frac{C_2 - C_1}{C_1 C_2}\right), \tag{5.11}$$

where f is the switching frequency. Substituting (5.11) into (5.10), E_{loss} can be rewritten as

$$E_{loss} = \frac{(C_2 - C_1)^2}{2C_1 C_2 (C_1 + C_2)} \frac{I^2}{f^2}. \tag{5.12}$$

E_{loss} is inversely proportional to the square of the frequency; thus, a higher switching frequency is preferable. These equations mean that if C_1 and C_2 were completely equal, there would be no energy loss due to the voltage difference. However, the voltage difference practically remains more or less after every switching during charging and discharging. For instance, String B is charged/discharged during the entire period, whereas Strings A and C are not charged/discharged during the dead time period. The amount of charge during the dead time period causing voltage deviation can be expressed as

$$\Delta V_d = \frac{IT_d}{C}, \tag{5.13}$$

where ΔV_d is the voltage deviation caused by single dead time and T_d is the dead time. This equation does not express all factors that cause voltage deviation during charging/discharging. The voltage drop across switches and capacitance dispersion also cause voltage imbalance. Besides, transient characteristic, which is a function of resistances of cells and switches as well as capacitances, should also be considered to determine the voltage imbalance during a steady state.

Fast equalization, which can deliver a great amount of charge, is required to minimize the voltage difference. Cells 1 and 2 are equalized when S_1 and S_2 are turned on. Current flowing between cells during equalization is expressed as

$$I(t) = \frac{V_1 - V_2}{R} exp\left(\frac{-t}{CR}\right), \tag{5.14}$$

where

$$\begin{cases} C = \dfrac{C_1 C_2}{C_1 + C_2} \\ R = r_1 + r_2 + R_1 + R_2 \end{cases}. \tag{5.15}$$

This equation shows that faster equalization can be achieved with lower resistance.

5.5.3 Experiment

An experimental circuit, as that shown in Fig. 5.5.1, was tested using EDLCs as SCs. The capacitances of EDLCs with a rated voltage of 2.5 V were $C_{1A} = C_{2A} = C_{2C} = C_{3C} = 700$ F and $C_{1B} = C_{3B} = 1400$ F. An EDLC with a capacitance of 350 F, instead of 700 F, was used for C_{2B} (hereafter called "deteriorated cell") on the assumption that severe deterioration of a cell had occurred locally. The circuit was charged using a constant current–constant voltage (CC–CV) protocol and discharged with a CC of 1.46 A, which corresponds to a rate of 1C (the rate at which cells are fully charged/discharged for 1 h). For differentiation, charging and discharging were performed with/without equalization. The MOSFET switches were operated at a switching frequency of 100 Hz, which was judged to be high enough to realize fast equalization, while the dead time ratio was 10%. Voltage deviation due to capacitance difference, determined by (5.11), was 62.6 μV for this experimental condition. According to (5.13), voltage deviations of C_{1B}–C_{3B} caused during each dead time period were less than 2 μV, indicating that the dead time ratio of 10% was negligible for the experimental condition.

Fig. 5.5.5 shows the resulting charge/discharge curves of the EDLCs without equalization. As for the case of without equalization, the switches in S_a were turned on and those of S_b were

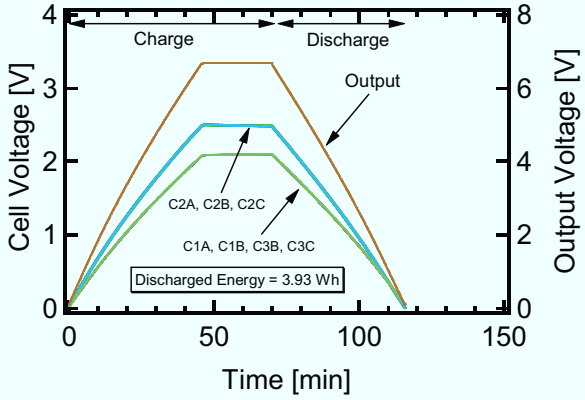


Fig. 5.5.5. Experimental charge/discharge curves of the output and cell voltages without equalization.

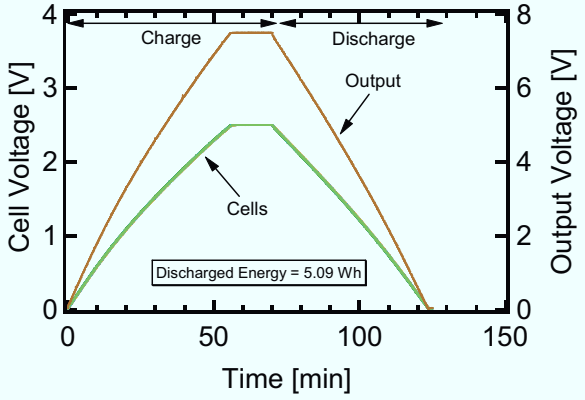


Fig. 5.5.6. Experimental charge/discharge curves of the output and cell voltages with equalization.

turned off during the entire period. Since the total capacitance of the parallel circuit containing the deteriorated cell (700 F // 350 F // 700 F = 1750 F) was smaller than those of the others (700 F // 1400 F = 2100 F), cell voltages increased more quickly and were about 400 mV higher than the others in a charged state. Only the EDLCs in the parallel circuit containing the deteriorated cell were fully charged to 2.5 V, while the others were not. Insufficient charging resulted in the discharged energy of 3.93 Wh, which was much smaller than the theoretical energy of 5.16 Wh.

The resulting charge/discharge curves with equalization are shown in Fig. 5.5.6. Voltage imbalance was diminished to less than 20 mV by equalization. Since the charging current was tapered to nearly zero during the CV charging period, the voltage imbalance was completely eliminated because of the absence of voltage drops across resistances of switches and cells during this period. All the cells in the circuit were fully charged to 2.5 V, providing a discharged energy of 5.09 Wh, which was much improved compared with that obtained without equalization. The loss was less than 1.5% for this experimental condition.

A large voltage difference between the EDLCs connected in parallel results in a large cross current, which acts as the charging/discharging current between the EDLCs. Fig. 5.5.7 shows the current waveforms of the EDLCs and the drive voltages for S_a and S_b during discharging. Positive and negative currents represent charging and discharging, respectively. During the dead

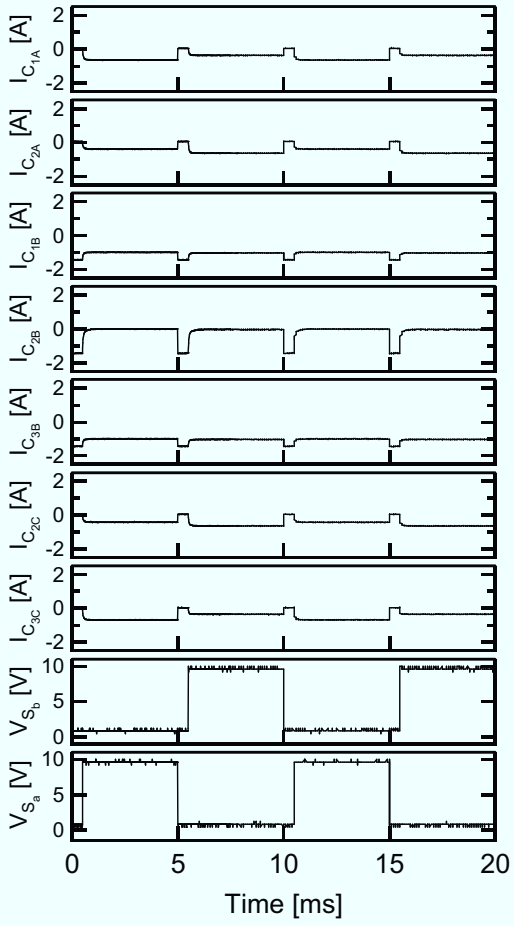


Fig. 5.5.7. Current waveforms of the cells and drive voltages for S_a and S_b during discharging.

time period, there was no current flowing through the cells in Strings A and C except for those in String B, as mentioned in Section 5.5.2. When S_a or S_b was on, the discharge current of the deteriorated cell (C_{2B}) was small compared with the others because the current of 1.46 A for each dead time period of 0.5 ms was large enough to discharge the deteriorated cell. When S_a was on, discharge currents of C_{1A} and C_{3C} were relatively larger than C_{2A} and C_{2C}, and vice versa when S_b was on. Since the discharge current of the deteriorated cell was quite small as mentioned above, other cells in the same parallel circuit had to discharge more.

The resultant current waveforms, whose average currents were proportional to their capacitances, showed that there was no large current due to a voltage difference between the cells connected in parallel. This result supports the high-efficiency performance shown in Fig. 5.5.6 because the large current causes large power dissipation in the form of voltage drops across the on-resistances of switches and internal resistances of EDLCs.

5.5.4 Conclusions

An equalizer utilizing series–parallel reconfigurable SCs, which consists of SCs and switches as its main circuit elements, was proposed in this paper. The proposed technique, in which the SCs can be used not only for energy storage but also for equalization, was considered to be suitable for energy storage systems consisting of multiple strings where relatively large energy and power are required.

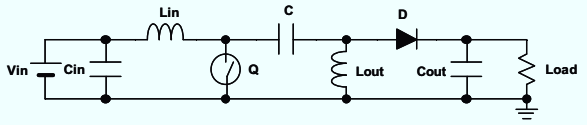
The proposed circuit containing the cell with inadequate capacitance was charged and discharged to demonstrate its performance on the assumption that severe deterioration had occurred locally. The resultant charge/discharge performance showed that the voltage imbalance due to the deteriorated cell was diminished, at the same time achieving high efficiency. No large current was observed due to the voltage difference between cells connected in parallel even though the experimental condition was very severe.

5.6 Single-Switch Cell Voltage Equalizer Using Multi-Stacked Buck-Boost Converters

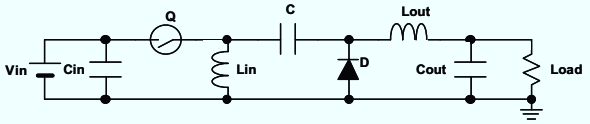
5.6.1 Circuit Description and Major Features

Fig. 5.6.1 shows traditional buck-boost converters that can be used as the basic topology for the proposed singel-switch cell voltage equalizers: a single ended primary inductor converter (SEPIC) and a Zeta converter containing two inductors and a coupling capacitor. A Ćuk converter, which is an inverting buck-boost converter, cannot be used as the basic topology because of its inverting property. However, incorporating a transformer into its design transforms it into a noninverting converter (shown in Fig. 5.6.1(c)), which can then be used as the basic topology. The proposed equalizers can be derived by stacking the circuits consisting of capacitors (C), diodes (D), and inductors (L_{out}) shown in Fig. 5.6.1.

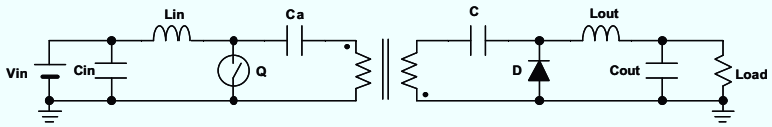
Figs. 5.6.2(a), (b), and (c) show SEPIC-, Zeta-, and isolated Ćuk-based topologies, respectively, for the proposed cell voltage equalizers for four series-connected energy storage cells, B_1–B_4. Instead of the dc power source V_{in} present in the traditional buck-boost converters (Fig. 5.6.1), the top of the series connection of B_1–B_4 is connected to C_{in} in Fig. 5.6.2. Both the SEPIC- and Zeta-based topologies can be implemented using a transformer, although these variations are not illustrated in Fig. 5.6.2. In this section, the SEPIC-based equalizer shown in



(a)



(b)



(c)

Fig. 5.6.1. Traditional buck-boost converters that can be used as the basic topology for the proposed cell voltage equalizers. (a) SEPIC, (b) Zeta, and (c) isolated Ćuk converters.

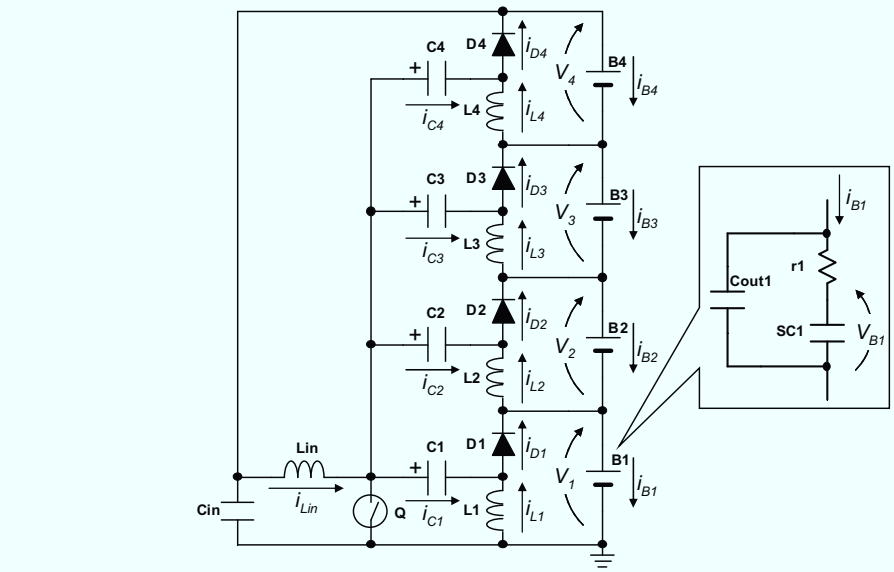
Fig. 5.6.2(a) is used as a representative topology.

The inset of Fig. 5.6.2(a) shows an equivalent circuit that represents the energy storage cell. The cell is represented as a series connection of an energy storage capacitor SC_1 and an equivalent series resistance (ESR) r_1 with a smoothing capacitor C_{out1} connected in parallel. B_1–B_4 are connected to four diode–inductor pairs, D_1-L_1, D_2-L_2, D_3-L_3, and D_4-L_4, whose junctions are connected to coupling capacitors C_1–C_4, respectively. These capacitors are connected to the switch Q and the input inductor L_{in}. The circuit consisting of C_{in}, L_{in}, Q, C_1, D_1, L_1, and B_1 is identical to the traditional SEPIC shown in Fig. 5.6.1(a). Except for Q and L_{in}, the circuit consisting of C_i-D_i-L_i (where i = 1…4) is multi-stacked, and hence, the proposed cell voltage equalizer can be regarded as a single-switch multi-stacked SEPICs.

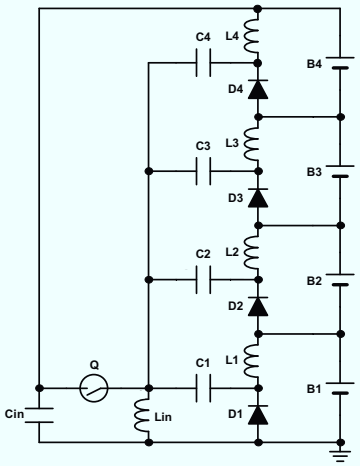
The proposed equalizer consists of a single active component (i.e., switch Q) and passive components, significantly reducing the circuit complexity as compared to those of conventional topologies. Detailed comparison with the conventional cell voltage equalizers in terms of circuit complexity will be made in Section 5.8.

5.6.2 Operation Analysis

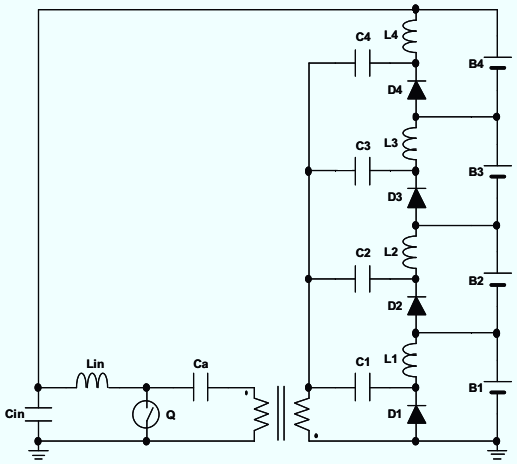
Similar to conventional buck-boost converters, the proposed equalizers operate in either continuous conduction mode (CCM) [23] or discontinuous conduction mode (DCM) [24]. Conventional buck-boost converters operating in DCM are used for power factor correction applications [25]. The boundary between CCM and DCM is a discontinuity in the diode current during the off period [23],[24]. In other words, the converter operates in CCM as long as the diode current is higher than zero during the off period. On the other hand, for DCM, the diode current must decrease to zero during the off period. In the proposed equalizers operating in



(a)



(b)



(c)

Fig. 5.6.2. Proposed single-switch cell voltage equalizers using multi-stacked buck-boost converters. (a) SEPIC-based, (b) Zeta-based, and (c) isolated Ćuk-based equalizers.

DCM with a fixed duty cycle, the input and output currents can be limited to a desired level without feed back control. This section focuses on the DCM operations under cell-voltage-balanced and -imbalanced conditions, and shows how the currents can be limited to a desired range without feedback control. This section focuses on only the SEPIC-based equalizer, but similar developments can be made for the Zeta- and Ćuk-based equalizers as well.

5.6.2.1 Operation under Cell-Voltage-Balanced Condition

Fig. 5.6.3 shows operating waveforms of the SEPIC-based equalizer operating in DCM under the cell-voltage-balanced condition, in which all cell voltages are uniform. Current flow

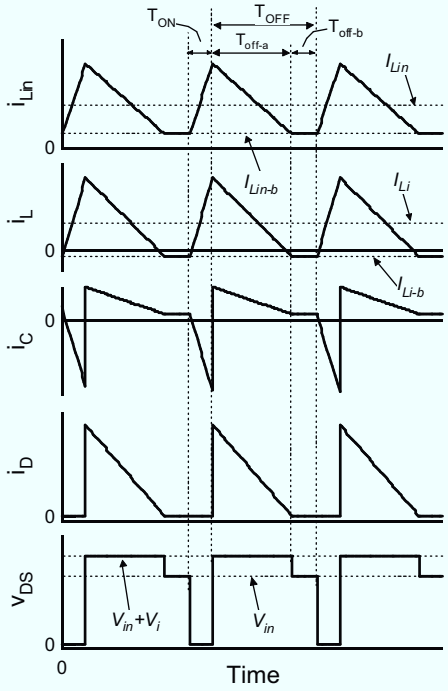


Fig. 5.6.3. Operating waveforms of the SEPIC-based equalizer under cell-voltage-balanced condition.

directions under the voltage-balanced condition are shown in Fig. 5.6.4. The fundamental operation is very similar to that of the conventional SEPIC. The DCM operation can be divided into on and off periods (T_{on} and T_{off}), and the off period can be subdivided into $T_{off\text{-}a}$ and $T_{off\text{-}b}$.

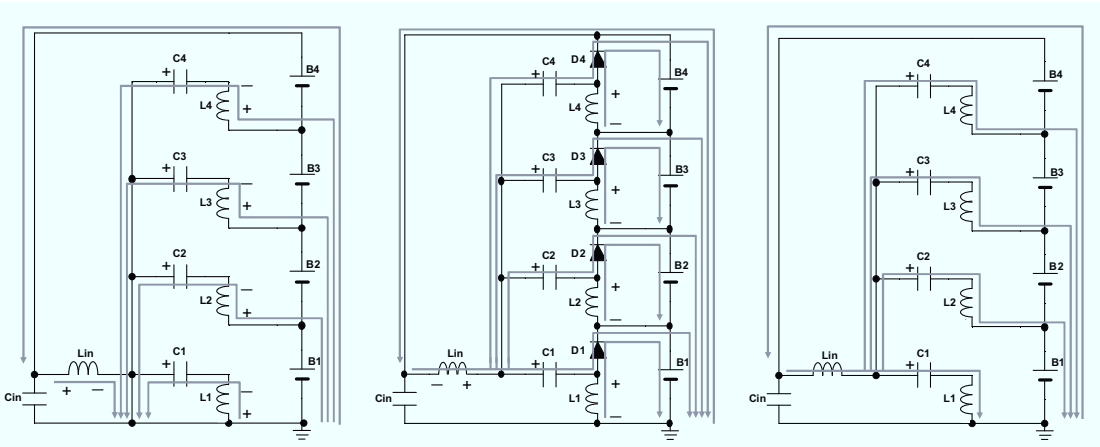
Under a steady state condition, the average voltage of inductors in a single switching cycle is zero even in DCM operation. Hence, the average voltages of C_1–C_4, given by V_{C1}–V_{C4}, can be expressed as

$$\begin{cases} V_{C1} = V_{in} \\ V_{C2} = V_{in} - V_1 \\ V_{C3} = V_{in} - (V_1 + V_2) \\ V_{C4} = V_{in} - (V_1 + V_2 + V_3) \end{cases}, \tag{5.16}$$

where V_1–V_4 are the voltages denoted in Fig. 5.6.2(a). V_{in} is the voltage of C_{in} and is given by

$$V_{in} = V_1 + V_2 + V_3 + V_4 . \tag{5.17}$$

During the on period, T_{on}, which is illustrated in Fig. 5.6.4(a), the switch turns on and all the inductor currents increase and are directed to Q. The diodes are off during the T_{on} period, and the current through L_i, i_{Li}, flows into each capacitor. The current to the input of the equalizer (i.e., the junction of L_{in} and C_{in}) is supplied by the cells B_1–B_4. However, the currents flowing through individual cells during this period are found to be different from each other. For example, B_1 discharges to L_2-C_2–L_4-C_4, while B_2 and B_3 discharge to L_3-C_3–L_4-C_4 and L_4-C_4, respectively. Thus, the lower the position of the cell in the circuit, the larger will be the discharge current that flows during the T_{on} period.



(a) (b) (c)

Fig. 5.6.4. Current flow directions during (a) T_{on}, (b) $T_{off\text{-}a}$, and (c) $T_{off\text{-}b}$ of the SEPIC-based equalizer under cell-voltage-balanced condition.

During the $T_{off\text{-}a}$ period shown in Fig. 5.6.4(b), all the inductor currents decrease and flow to each cell. The current through L_{in}, i_{Lin}, is distributed to C_1–C_4. Therefore, a diode current i_{Di}, which is the sum of i_{Li} and i_{Ci}, also decreases. The currents through each cell during $T_{off\text{-}a}$ are also different from each other, as similar during T_{on}. For example, i_{C1} flows only to B_1 via D_1, while i_{C4} flows to B_1–B_4 via D_4. Thus, the lower the position of the cell, the larger will be the charge current flowing during $T_{off\text{-}a}$.

After i_{Di} decreases to zero, the $T_{off\text{-}b}$ period begins and the current flow directions change, as shown in Fig. 5.6.4(c). This $T_{off\text{-}b}$ period is unique to DCM operations and is not found in CCM operations. The voltages applied to each inductor during $T_{off\text{-}b}$ are zero, and hence, the inductor currents are constant during the $T_{off\text{-}b}$ period, as in the traditional SEPIC [24], [25].

Under a steady-state condition, the voltage–time product of the inductors in a single switching cycle must be zero, and hence,

$$\begin{cases} DV_{C1} & = D_a\left(V_1 + V_{D1}\right) \\ D\left(V_{C2} + V_1\right) & = D_a\left(V_2 + V_{D2}\right) \\ D\left(V_{C3} + V_1 + V_2\right) & = D_a\left(V_3 + V_{D3}\right) \\ D\left(V_{C4} + V_1 + V_2 + V_3\right) & = D_a\left(V_4 + V_{D4}\right) \end{cases}, \tag{5.18}$$

where D is the duty cycle and D_a is given by

$$D_a = \frac{T_{off-a}}{T_S}, \tag{5.19}$$

where T_S is the switching period. From (5.16), (5.17), and (5.18), V_i and D_a can be rewritten as

$$V_i = \frac{D}{D_a} V_{in} - V_{Di}, \tag{5.20}$$

$$D_a = \frac{DV_{in}}{V_i + V_{Di}}, \tag{5.21}$$

where the subscript i represents the number of symbols (i.e., $i = 1 \ldots 4$). Equation (5.20) implies that the equalizer produces uniform output voltages regardless of the individual voltages of cells B_1–B_4.

In order for the equalizer to operate in DCM, $T_{off\text{-}b}$ periods must exist. In other words, the $T_{off\text{-}a}$ period must be shorter than the T_{off} period. Therefore, D_a must satisfy the condition $D_a < (1 - D)$. From (5.21), the critical duty cycle, $D_{Critical}$, is given by

$$D_{Critical} < \frac{V_i + V_{Di}}{V_{in} + V_i + V_{Di}}. \tag{5.22}$$

This equation needs to be satisfied for the equalizer to operate in DCM. If it is violated, the equalizer operates in CCM in which the equalizer cannot operate with a fixed duty cycle. Equation (5.22) implies that the smaller the value of D, the larger will be the range of the ratio of V_i to V_{in}. In other word, as D decreases, the DCM operation can be ensured in a wider range.

The average current through B_i, I_{Bi}, is

$$I_{Bi} = I_{Di} - I_{Lin}, \tag{5.23}$$

where I_{Di} is the average current through D_i and I_{Lin} is the average current through L_{in}, which is equal to the current flowing from the cells to the equalizer (i.e., the average input current to the equalizer). The average current flowing from the equalizer to B_i is the same as that flowing through D_i.

I_{Li} and I_{Lin} are expressed as

$$I_{Li} = (D + D_a)\frac{V_{in} D T_S}{2L_i} + I_{Li-b}, \tag{5.24}$$

$$I_{Lin} = (D + D_a)\frac{V_{in} D T_S}{2L_{in}} + I_{Lin-b}, \tag{5.25}$$

where $I_{Li\text{-}b}$ and $I_{Lin\text{-}b}$ are the currents flowing through L_i and L_{in}, respectively, during the $T_{off\text{-}b}$ period, as designated in Fig. 5.6.3. Assuming that the impedances of B_1–B_4 are negligible and i_{Lin} is equally distributed to C_1–C_4, the relationship between $I_{Li\text{-}b}$ and $I_{Lin\text{-}b}$ is given by

$$I_{Lin-b} = -I_{L1-b} - I_{L2-b} - I_{L3-b} - I_{L4-b} = -4I_{Li-b}, \tag{5.26}$$

and the average current through C_i, I_{Ci}, which must be zero under a steady-state condition, is expressed as

$$I_{Ci} = I_{Li-b} + D\frac{V_{in} D T_S}{2L_i} - D_a \frac{V_{in} D T_S}{2 \cdot 4L_{in}} = 0. \tag{5.27}$$

From (5.24)–(5.27),

$$\frac{I_{Li}}{I_{Lin}} = \frac{D_a}{4D}. \tag{5.28}$$

From Kirchhoff's current law, the average current flowing through L_i, I_{Li}, is

$$I_{Li} = I_{Di}, \tag{5.29}$$

because $I_{Ci} = 0$ under a steady-state condition, as expressed by (5.27). From (5.23), (5.28), and (5.29), I_{Bi} can be expressed as

$$I_{Bi} = I_{Di}\frac{D_a - 4D}{D_a}, \tag{5.30}$$

where

$$I_{Di} = D_a\frac{V_{in}DT_S}{2\cdot 4L_{in}} + D_a\frac{V_{in}DT_S}{2L_i} = \frac{V_{in}DD_aT_S}{2}\left(\frac{4L_{in}+L_i}{4L_{in}L_i}\right) \geq 0. \tag{5.31}$$

Equations (5.28), (5.29), and (5.31) yield

$$I_{Lin} = \frac{V_{in}D^2T_S}{2}\left(\frac{4L_{in}+L_i}{L_{in}L_i}\right). \tag{5.32}$$

The larger the values of V_{in}, D, and T_S, the larger will be the currents expressed by (5.30)–(5.32).

With the known operating voltage ranges of V_i and V_{in}, D can be arbitrarily determined in order to satisfy (5.22). With the known value for D, I_{Lin} can be a certain constant value according to (5.32). Similarly, with the known values for V_i, V_{in}, and D, a certain range is expected for D_a on the basis of (5.21). In (5.31), I_{Di} is expressed by the constant values of L_{in}, L_i, and T_S and the expected value of D_a, while D is determinable. Therefore, I_{Di} can be limited to a value below the desired current level by determining D properly. Similarly, I_{Bi} can also be limited below a desired value because it is determined by I_{Di}, D, and D_a, as indicated by (5.30). Thus, the DCM operation can limit currents without the need for feedback control.

In the case of $V_{Di} = 0$, (5.17), (5.21), and (5.30) yield a current I_{Bi} that is equal to zero, indicating that I_{Di} (the current flowing from the equalizer to the cells) and I_{Lin} (the current flowing from the cells to the equalizer) are balanced. This fact can be explained by applying the law of energy conservation and can be expressed as

$$V_{in}I_{Lin} = (V_1 + V_{D1})I_{D1} + (V_2 + V_{D2})I_{D2} + (V_3 + V_{D3})I_{D3} + (V_4 + V_{D4})I_{D4}, \tag{5.33}$$

in which $V_{Di} = 0$ yields $I_{Bi} = 0$ on the basis of (5.17) and (5.23).

I_{Di} can be expressed differently as

$$I_{Di} = \frac{V_i - V_{Bi}}{r_i} \geq 0, \tag{5.34}$$

where V_{Bi} and r_i are the electromotive force and ESR of B_i, respectively, as designated in the inset of Fig. 5.6.2(a).

5.6.2.2 Operation under Cell-Voltage-Imbalanced Condition

For voltage-imbalanced series-connected cells, (5.33) and (5.34) suggest that the current flowing from the equalizer tends to flow toward the cell(s) having the lowest voltage. This section analyzes the operation under the cell-voltage-imbalanced condition using $V_{B1} < V_{Bi}$ (i = 2…4) as an example.

The operating waveforms and current flow paths under the voltage-imbalanced condition are

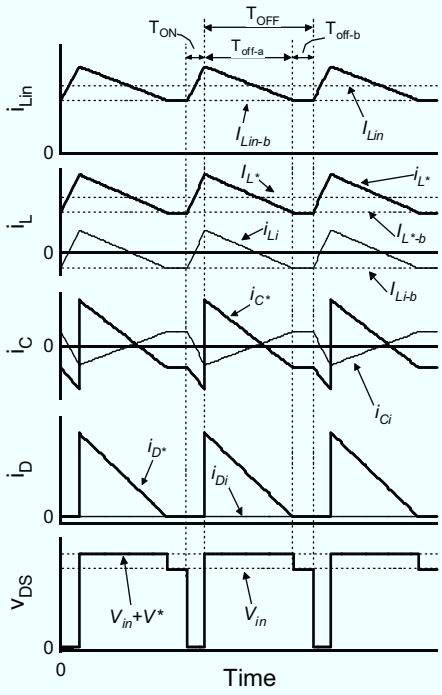
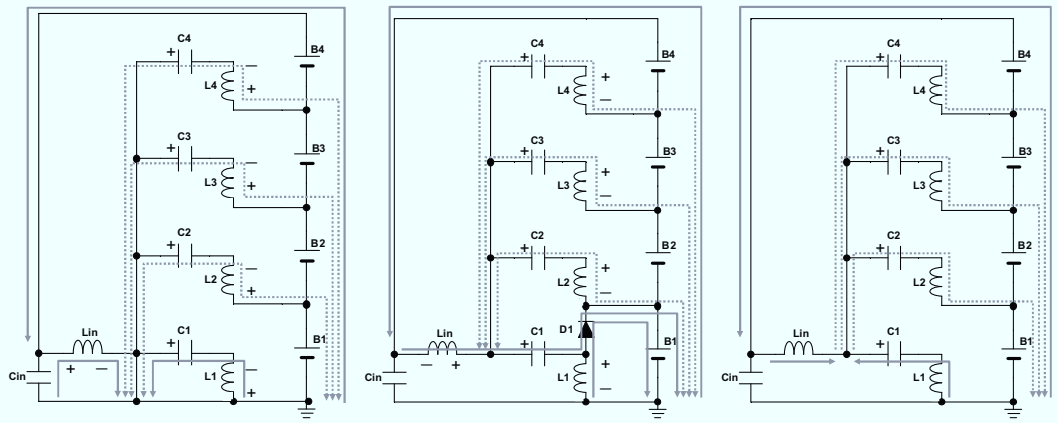


Fig. 5.6.5. Operating waveforms of the SEPIC-based equalizer under cell-voltage-imbalanced condition.

shown in Figs. 5.6.5 and 5.6.6, respectively. Asterisks (*) added to the symbols in Fig. 5.6.5 denote the subscript number of the cell(s) having the lowest voltage (i.e., $I_{L*} = I_{L1}$, $i_{L*} = i_{L1}$, $i_{C*} = i_{C1}$, $i_{D*} = i_{D1}$, and $V_* = V_1$ in the example condition). Fig. 5.6.5 shows that I_{Li} and I_{Di} are zero while I_{L*} and I_{D*} are positive, indicating that the current from the equalizer flows only to B_*.

Under the voltage-imbalanced condition, the current paths during the T_{on} period are similar to those under the voltage-balanced condition, although I_{L2}–I_{L4} are zero and only ripple current components flow through L_2–L_4 (as indicated by the dashed lines in Fig. 5.6.6(a)). During the



(a) (b) (c)

Fig. 5.6.6. Current flow directions during (a) T_{on}, (b) $T_{off\text{-}a}$, and (c) $T_{off\text{-}b}$ of the SEPIC-based equalizer under cell-voltage-imbalanced condition.

$T_{off\text{-}a}$ period shown in Fig. 5.6.6(b), only D$_*$ (D$_1$) is on while other diodes are off. i_{Lin} flows only to capacitor C$_*$ (C$_1$). During the $T_{off\text{-}b}$ period shown in Fig. 5.6.6(c), in which all the diode currents are zero, all the inductor currents are constant, as same under the cell-voltage-balanced condition. Under the cell-voltage-imbalanced condition, i_{L2}–i_{L4} are equal to i_{C2}–i_{C4} for the entire period, and therefore, I_{L2}–I_{L4} must be zero because the average capacitor current under a steady-state condition must be zero. Furthermore, currents i_{D2}–i_{D4} are also zero for the entire period because currents do not flow from the equalizer to B$_2$–B$_4$ in the example condition. Therefore, the input energies from B$_1$–B$_4$ to the equalizer are redistributed only to B$_1$, and a relatively large current flows through L$_1$, C$_1$, and D$_1$.

From Figs. 5.6.6(a) and (b), the voltage–time products of the inductors under the cell-voltage-imbalanced condition are given by

$$\begin{cases} DV_{C1} & = D_a\left(V_1 + V_{D1}\right) \\ D\left(V_{C2} + V_1\right) & = D_a\left(V_{C1} - V_{C2} + V_{D1}\right) \\ D\left(V_{C3} + V_1 + V_2\right) & = D_a\left(V_{C1} - V_{C3} - V_2 + V_{D1}\right) \\ D\left(V_{C4} + V_1 + V_2 + V_3\right) & = D_a\left(V_{C1} - V_{C4} - V_2 - V_3 + V_{D1}\right) \end{cases}. \tag{5.35}$$

From (5.16), (5.17), and (5.35), D_a can be generalized as

$$D_a = \frac{DV_{in}}{V_* + V_{D*}}, \tag{5.36}$$

where V_* and V_{D*} correspond to V_1 and V_{D1}, respectively, in the example condition. From (5.36) and $D_a < (1 - D)$, which is the boundary condition between CCM and DCM (as mentioned in the previous section), the critical duty cycle, $D_{Critical}$, under the voltage-imbalanced condition can be determined by

$$D_{Critical} < \frac{V_* + V_{D*}}{V_{in} + V_* + V_{D*}}. \tag{5.37}$$

Similar to the case in the cell-voltage-balanced condition explained in Section 5.6.2.1, the equalizer operates in DCM as long as this equation is satisfied. If the equalizer is operated in a voltage range that violates (5.37), the equalizer operates in CCM in which the fixed duty cycle operation is no longer feasible. The smaller the value of D, the larger will be the ratio of operable range of V_* to V_{in}. However, the decrease in D also decreases currents in the equalizer, as expressed by the equations later, resulting in slower equalization process in the cell-voltage-imbalanced condition.

The average currents of L$_*$ and L$_i$ under the cell-voltage-imbalanced condition are expressed as

$$I_{L*} = \left(D + D_a\right)\frac{V_{in}DT_S}{2L_*} + I_{L*-b}, \tag{5.38}$$

$$I_{Li} = \left(D + D_a\right)\frac{V_{in}DT_S}{2L_i} + I_{Li-b} = 0, \tag{5.39}$$

where $I_{L*\text{-}b}$ is the current flowing through L$_*$ during the $T_{off\text{-}b}$ period, as illustrated in Fig. 5.6.5.

Under the cell-voltage-imbalanced condition, (5.26) can be rewritten as

$$I_{Lin-b} = -I_{L*-b} - I_{L2-b} - I_{L3-b} - I_{L4-b} = -I_{L*-b} - 3I_{Li-b}\,. \tag{5.40}$$

During the T_{on} period, the current flowing through C_* is equal to that through L_* (i.e., i_{L1} flows to C_1), as shown in Fig. 5.6.6(a). However, during the $T_{off\text{-}a}$ period, i_{Lin} and i_{Li} (i.e., i_{L2}–i_{L4}) flow to C_*, as shown in Fig. 5.6.6(b). During the $T_{off\text{-}b}$ period, the current flowing through C_* is again equal to that through L_*. Under the steady-state condition, the average current flowing through C_*, given by I_{C*}, under the voltage-imbalanced condition is expressed as

$$I_{C*} = I_{L*-b} + D\frac{V_{in}DT_S}{2L_*} - D_a\frac{V_{in}DT_S}{2}\left(\frac{1}{L_{in}} + \frac{3}{L_i}\right) = 0\,. \tag{5.41}$$

From (5.25), (5.38), (5.39), (5.40), and (5.41),

$$\frac{I_{L*}}{I_{Lin}} = \frac{D_a}{D}\,. \tag{5.42}$$

From (5.23), (5.29), and (5.42), I_{B*} can be expressed as

$$I_{B*} = I_{D*}\frac{D_a - D}{D_a}\,. \tag{5.43}$$

By assuming that $L_* = L_i$, I_{D*}, which is the average current flowing through D_*, is given by

$$I_{D*} = D_a\frac{V_{in}DT_S}{2L_{in}} + D_a\frac{V_{in}DT_S}{2L_*} + D_a\frac{3V_{in}DT_S}{2L_i} = \frac{V_{in}DD_aT_S}{2}\left(\frac{4L_{in} + L_i}{L_{in}L_i}\right) \geq 0\,, \tag{5.44}$$

which is fourfold larger than that in (5.31). Equations (5.29), (5.42), and (5.43) yield

$$I_{Lin} = \frac{V_{in}D^2T_S}{2}\left(\frac{4L_{in} + L_i}{L_{in}L_i}\right), \tag{5.45}$$

which is identical with (5.32), indicating that I_{Lin} is independent on the cell voltage imbalance. Similar to the case in the cell-voltage-balanced condition, the currents expressed by (5.43)–(5.45) increase with the values of V_{in}, D, and T_S. Since a cell voltage imbalance is equalized at a rate proportional to the currents [26], the equalization process can be accelerated by increasing these values.

Under the cell-voltage-imbalanced condition, I_{D*} and I_{B*} can be arbitrarily limited in a manner similar to the operation under the cell-voltage-balanced condition (as explained in Section 5.6.2.1). This is because these parameters are determined by the constant values of L_{in}, L_i, and T_S and the expected value of D_a, and determinable D, which can be determined using (5.42), (5.43), and (5.44). Besides, I_{Lin} can be a certain constant value as indicated by (5.45). Therefore, even under the cell-voltage-imbalanced condition, the DCM operation can also limit the currents without feedback control. However, making a comparison between (5.28) and (5.42), and (5.31) and (5.44), the currents under the voltage-imbalanced condition are found to concentrate to the components with asterisk. Hence, the circuit components should be designed considering the cell voltage imbalance.

In this section, the representative case that B_1 is the only cell with the lowest voltage was

analyzed for the SEPIC-based equalizer, but the similar manner can be applied to other cases, e.g., other cell(s) having the lowest voltage. Similarly, operations of other topologies, Zeta- and Ćuk-based equalizers, can be analyzed in a similar manner explained in this section.

5.6.3 Experiment

Experimental equalization tests were performed for four series-connected EDLCs having capacitance of 500 F each (shown in Fig. 5.6.7). An equalization current rate of approximately C/100 is considered sufficient to overcome a charging current during float charging for secondary batteries [2],[6]. However, in order to expedite the experimental equalization tests in our study, the current of 0.12 A, which corresponds to approximately 0.35 C for 500 F cells, was used, although the optimal equalization current for SCs is still controversial.

A prototype of the SEPIC-based cell voltage equalizer, shown in Fig. 5.6.8, was designed for an input current (i.e., I_{Lin}) of 0.12 A at V_{in} = 7.0 V for four series-connected SCs as energy storage cells. Considering the case that V_{in} = 7.0 V and V_* = 1.0 V, the duty cycle, D, was determined to be 0.16 at the switching frequency, f_S, of 100 kHz. Component values are shown in Table 5.2.

Fig. 5.6.7. Photograph of a 500-F-EDLC.

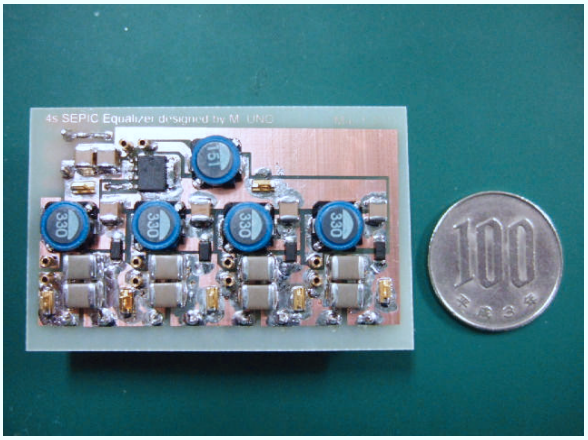


Fig. 5.6.8. Photograph of a prototype of the SEPIC-based cell voltage equalizer.

Table 5.2 Component values.

Component	Value
C_{out1}–C_{out4}	Ceramic Capacitor, 200 µF, 6.3 V
C_1–C_4	Ceramic Capacitor, 22 µF, 25 V
L_{in}	150 µH
L_1–L_4	33 µH
Q	N-Ch MOSFET, RJK0329DPB, R_{on} = 1.8 mΩ
D_1–D_4	Schottky Diode, CRS08, V_D = 0.36 V

The experimental equalization test was performed under a cell-voltage-imbalanced condition where the initial voltages of V_{B1}–V_{B4} were 1.0, 1.5, 2.0, and 2.5 V, respectively. The resultant equalization profiles are shown in Fig. 5.6.9. The equalization process can be divided into four periods, A–D, as designated with the dashed lines in Fig. 5.6.9. Positive and negative current values in Fig. 5.6.9 represent the charging and discharging currents, respectively. Typical measured waveforms of i_{Lin}, i_{L1}–i_{L4}, and voltage of the switch, v_{DS}, during each period are shown in Fig. 5.6.10. The measured waveforms were almost identical to those in Figs. 5.6.3 and 5.6.5, although the oscillations caused by the parasitic capacitance of the MOSFET were observed.

During period A, (at the beginning of the equalization test) B_1 was charged and V_1 increased, while the other cells discharged and V_2–V_4 decreased. In other words, B_2–B_4 provided their energies to the equalizer's input, and the energies were redistributed only to B_1 via the equalizer. As shown in Fig. 5.6.10(a), except for i_{L1}, i_{L2}–i_{L4} were uniform and their averages were zero,

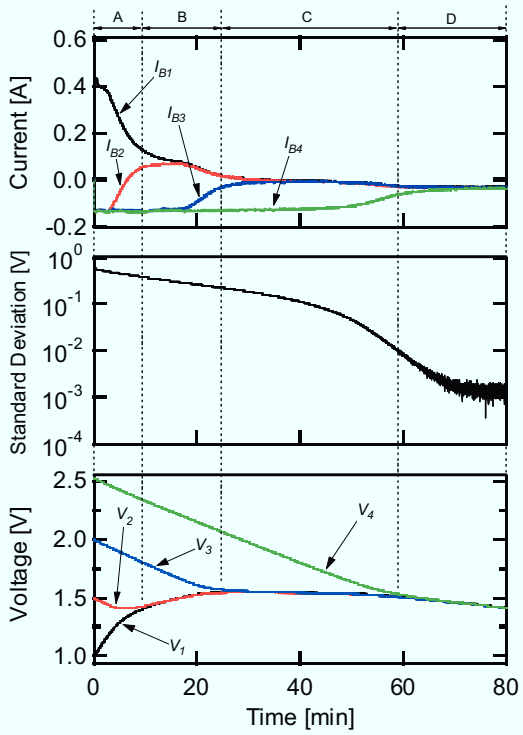


Fig. 5.6.9. Experimental equalization profiles of series-connected SCs whose initial voltages, V_{B1}–V_{B4}, were 1.0, 1.5, 2.0, and 2.5 V, respectively.

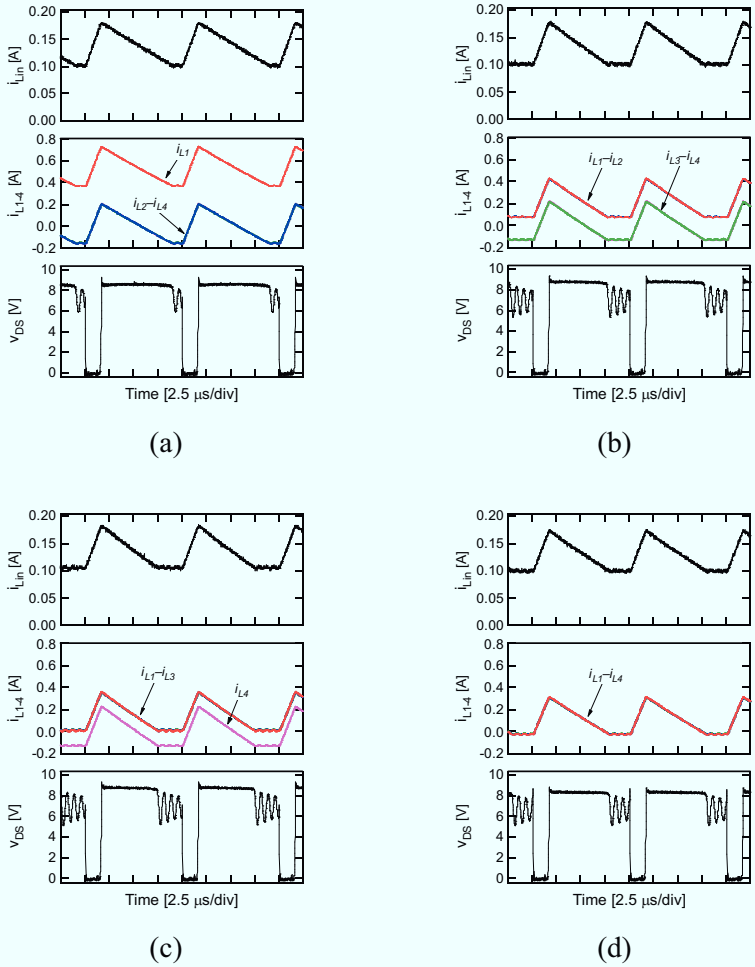


Fig. 5.6.10. Resultant waveforms during Periods (a) A, (b) B, (c) C, and (d) D.

while the average of i_{L1} was positive. According to (5.29), B_1, which was the cell with the lowest voltage during period A, was charged by the equalizer via D_1.

As V_1 approached V_2, I_{B2} changed from negative to positive and I_{B1} decreased because the equalizer started to redistributing the energies not only to B_1 but also B_2 during period B. During period B, I_{B1} and I_{B2} became identical and positive while I_{B3} and I_{B4} were almost the same as during period A. As shown in Fig. 5.6.10(b), i_{L1} and i_{L2} were uniform and their averages were positive, indicating that B_1 and B_2 were charged by the equalizer. On the other hand, the averages of i_{L3} and i_{L4} were still zero. These results indicate that B_3 and B_4 were still energizing the equalizer, while the energies were redistributed to B_1 and B_2 uniformly. Hence, V_1 and V_2 increased uniformly while V_3 and V_4 still decreased.

During period C, in which V_1–V_3 were uniform and only V_4 was higher, the equalizer began to charge B_3. I_{B3} became positive while I_{B4} was still negative. Finally, during period D, all the profiles and waveforms became uniform. During this period, the energies from the cells to the equalizer's input and those redistributed to the cells from the equalizer are supposed to be balanced as long as the equalizer operates ideally as mentioned in Section 5.6.2.1, but the cell voltages gradually decreased as all the cells discharged even after the cell voltage imbalance was eliminated. These gradual decreases in the cell voltage were due to the power conversion

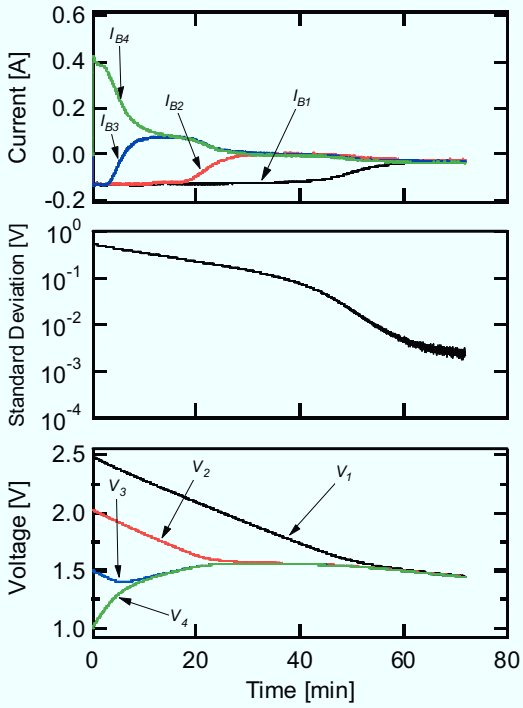


Fig. 5.6.11. Experimental equalization profiles of series-connected SCs whose initial voltages, V_{B1}–V_{B4}, were 2.5, 2.0, 1.5, and 1.0 V, respectively.

loss of the equalizer; the energies redistributed from the equalizers to the cells were smaller than those delivered from the cells to the equalizer because of the power conversion loss. Hence, the equalizer should be disabled after the cell voltage imbalance is eliminated in order not to waste the energies of the cells.

In summary, the cell(s) with the lowest voltage was (were) charged while those with higher voltages were discharged by the equalizer, as explained in Section 5.6.2.2. The cell voltage imbalance was gradually eliminated as time elapsed, and the standard deviation decreased to approximately 1 mV at the end of the experiment.

Fig. 5.6.11 shows another experimental equalization test result for a different imbalanced condition having initial voltages (V_{B1}–V_{B4}) of 2.5, 2.0, 1.5, and 1.0 V, respectively. The resultant profiles were similar to those in Fig. 5.6.10, confirming that the equalization process and energy redistribution were dependent only on the cell voltage level and were independent on the positions of cells within the series connection.

5.6.4 Conclusions

Single-switch cell voltage equalizers using multi-stacked buck-boost converters for series-connected energy storage cells were proposed. Traditional buck-boost converters such as SEPIC, Zeta, and Ćuk converters can be used as the basic topology for the proposed equalizers. In this section, the SEPIC-based equalizer was used as a representative topology for operation analyses and experimental tests.

The operations under both cell-voltage-balanced and -imbalanced conditions were

mathematically analyzed. The operation analyses revealed that the energies of the series-connected cells can be redistributed to the cell(s) having the lowest voltage. In addition, currents flowing through the cells and circuit components in DCM can be limited to a desired current level without the need for feedback control.

Experimental equalization tests were performed for four series EDLCs using the SEPIC-based equalizer operating in DCM with a fixed duty cycle. Resultant equalization profiles demonstrated that the energies of series-connected SCs were preferentially redistributed to the cell(s) with the lowest voltage at each time instant. The cell voltage imbalance was gradually eliminated as time elapsed, and all the cell voltages eventually became uniform. The cell voltage level was the only parameter found to be relevant to energy redistribution, and the positions of the cells within the series connection were verified to be irrelevant.

5.7 Single-Switch Cell Voltage Equalizer Using Voltage Multiplier

5.7.1 Circuit Description and Major Features

An example circuit description of the proposed cell voltage equalizer for six SCs connected in series is shown in Fig. 5.7.1. Each SC, SC_1–SC_6, is connected in parallel with two-series diodes whose junctions are tied to coupling capacitors, C_1–C_6. The SCs, capacitors, and diodes together constitute the voltage multiplier. The energies of the series-connected SCs are redistributed to each SC via a transformer and the voltage multiplier. The secondary winding of the transformer in the example description is tied to the junction of D_6–D_7 or SC_3–SC_4, which is the center of the series connection. The secondary winding can be connected to other junctions of SCs, including the ground and the top of the series connection, although the voltage stress of capacitors tends to be higher.

By stacking diodes and coupling capacitors, the number of series connection of SCs can be

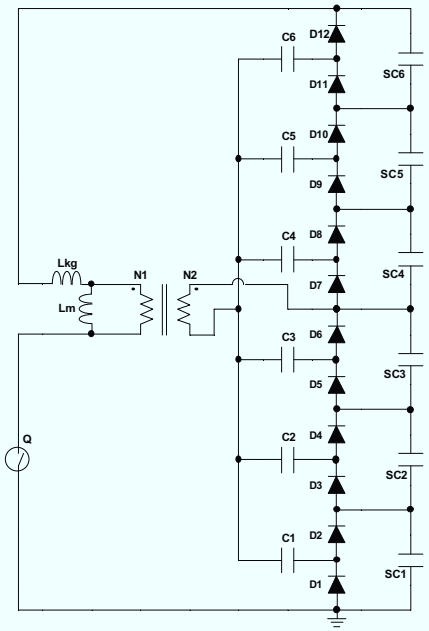


Fig. 5.7.1. Single-switch cell voltage equalizer using voltage multiplier for six SCs connected in series.

arbitrary extended without an additional switch or transformer. In other words, the proposed equalizer achieves good modularity (or extendibility) without additional switches.

Since switches require ancillary circuits consisting of driver ICs, opto-couplers, and passive components, the number of switches is considered as a good index to represent the circuit complexity. The number of required switches in the proposed equalizer is only one, whereas most conventional equalizers require numerous switches proportional to the number of series connections, as discussed in Section 5.3.

Thus, the circuit complexity can be reduced significantly, especially for applications needing a large number of series connections, when compared with conventional ones. In addition to a simple circuit configuration, the proposed equalizer can have a compact design because there is only one magnetic component. The single-switch single-transformer equalizer can be used in many applications, especially those having a large number of series connections.

5.7.2 Operation Analysis

5.7.2.1 Operation under Cell-Voltage-Balanced Condition

Fig. 5.7.2 shows key waveforms of the proposed equalizer operating in DCM under a cell-voltage-balanced condition. Current flow directions are illustrated in Fig. 5.7.3. The operation can be divided into on and off periods, T_{on} and T_{off}, and the off period can be further subdivided into $T_{off\text{-}a}$ and $T_{off\text{-}b}$. The transformer in the proposed equalizer operates in forward mode during T_{on}. On the other hand, the operation during T_{off} can be characterized as the discontinuous flyback mode.

The magnetizing current for the transformer, I_{LM}, which builds up during T_{on}, is released from the secondary winding to capacitors and SCs during $T_{off\text{-}a}$ as shown in Fig. 5.7.3(b). These currents correspond to flyback currents in conventional flyback converters. In DCM, I_{LM} is completely reset at every switching cycle, and hence, the peak of I_{LM} can be limited even with a fixed duty cycle. Therefore, currents during $T_{off\text{-}a}$ can be limited under a desired level even with fixed duty cycle operations. In other words, feedback control can be eliminated from the proposed equalizer by operating in DCM.

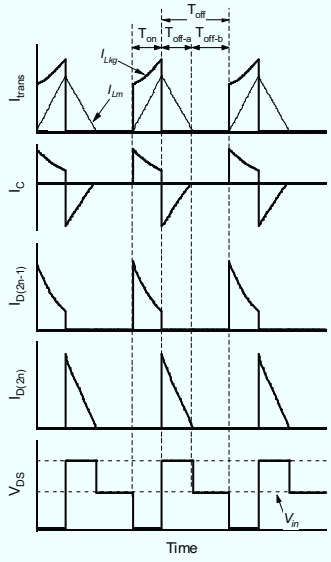
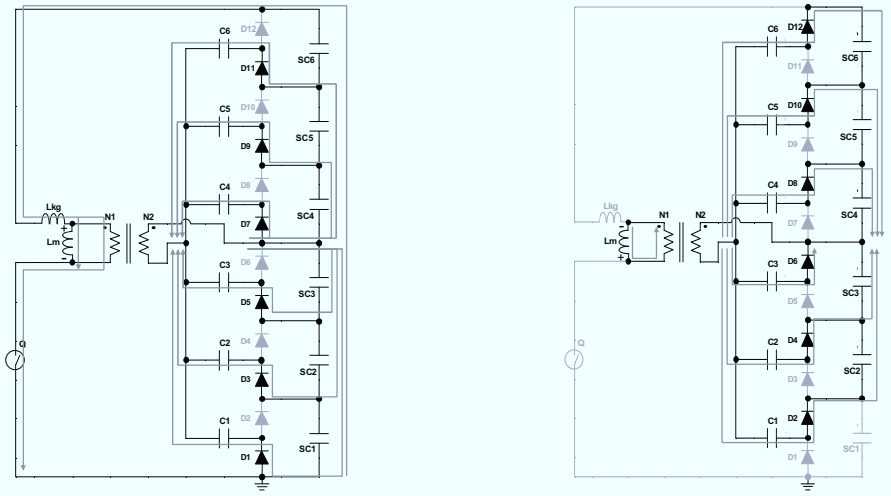


Fig. 5.7.2. Key waveforms in DCM under the cell voltage-balanced condition.



(a) (b)

Fig. 5.7.3. Current flow directions during (a) on and (b) off period ($T_{off\text{-}a}$).

During T_{on} period, in which the transformer operates in forward mode, the secondary winding behaves as a voltage source. The voltage of the secondary winding during the T_{on} period, $V_{S\text{-}on}$, is given by

$$V_{S-on} = \frac{N_S}{N_P}\left(V_{SC1} + V_{SC2} + V_{SC3} + V_{SC4} + V_{SC5} + V_{SC6}\right), \tag{5.46}$$

where N_P and N_S are the number of turns in the primary and secondary windings, respectively, and V_{SC1}–V_{SC6} are the voltage of SC_1–SC_6. I_{Lm} increases linearly, and the energy is stored in L_m.

Currents flow through odd-numbered diodes and the capacitors are charged during T_{on}. Since the capacitances of SC_1–SC_6 are rather larger than those of C_1–C_6, V_{SC1}–V_{SC6} can be assumed to be constant. The voltages of C_1–C_6, V_{C1}–V_{C6}, increase showing transient response characteristics. For example, the voltage waveforms of the upper half capacitors, C_4–C_6, are shown in Fig. 5.7.4. Since the capacitors during T_{on} are charged by voltage sources including the secondary winding and SCs, transient responses of the capacitors are governed by respective time constants of SCs,

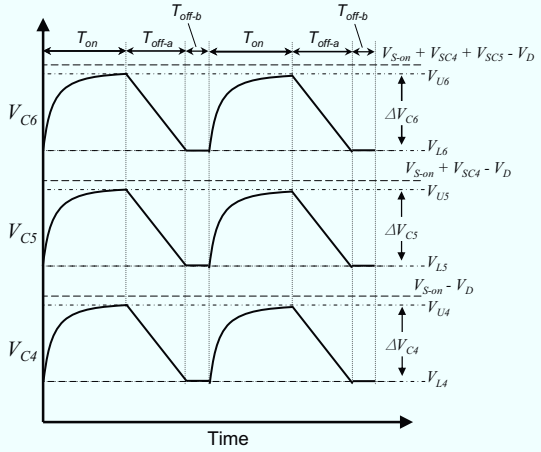


Fig. 5.7.4. Voltage waveforms of capacitors, C_4–C_6, under cell-voltage-balanced condition.

which are determined by ESR and capacitance. The voltages of C_1–C_6 at the end of T_{on}, V_{U1}–V_{U6}, are

$$\begin{cases} V_{U1} \le V_{S-on} - V_D - V_{SC3} - V_{SC2} - V_{SC1} \\ V_{U2} \le V_{S-on} - V_D - V_{SC3} - V_{SC2} \\ V_{U3} \le V_{S-on} - V_D - V_{SC3} \\ V_{U4} \le V_{S-on} - V_D \\ V_{U5} \le V_{S-on} - V_D + V_{SC4} \\ V_{U6} \le V_{S-on} - V_D + V_{SC4} + V_{SC5} \end{cases}. \tag{5.47}$$

The voltage variations of C_1–C_6 during operations, ΔV_{C1}–ΔV_{C6}, are expressed as

$$\begin{cases} \Delta V_{C1} = \left(V_{S-on} - V_D - V_{SC3} - V_{SC2} - V_{SC1} - V_{L1}\right)e_1 \\ \Delta V_{C2} = \left(V_{S-on} - V_D - V_{SC3} - V_{SC2} - V_{L2}\right)e_2 \\ \Delta V_{C3} = \left(V_{S-on} - V_D - V_{SC3} - V_{L3}\right)e_3 \\ \Delta V_{C4} = \left(V_{S-on} - V_D - V_{L4}\right)e_4 \\ \Delta V_{C5} = \left(V_{S-on} - V_D + V_{SC4} - V_{L5}\right)e_5 \\ \Delta V_{C6} = \left(V_{S-on} - V_D + V_{SC4} + V_{SC5} - V_{L6}\right)e_6 \end{cases}, \tag{5.48}$$

where e_i and τ_i ($i = 1 \ldots 6$) are given by

$$e_i = 1 - exp\left(\frac{-DT_S}{\tau_i}\right), \tag{5.49}$$

$$\tau_i = C_i r_i, \tag{5.50}$$

where D is the duty cycle, and C_i and r_i are the capacitance and ESR of capacitor C_i.

During $T_{off\text{-}a}$ period, the transformer operates in flyback mode, in which the secondary winding behaves as a current source. The stored energy in L_M is released from the secondary winding in the form of currents flowing through even-numbered diodes as shown in Fig. 5.7.3(b). $T_{off\text{-}a}$ period lasts until I_{LM} falls to zero. The voltages of C_1–C_6 at the end of $T_{off\text{-}a}$, V_{L1}–V_{L6}, are

$$\begin{cases} V_{L1} = -V_{S-off-a} + V_D - V_{SC3} - V_{SC2} \\ V_{L2} = -V_{S-off-a} + V_D - V_{SC3} \\ V_{L3} = -V_{S-off-a} + V_D \\ V_{L4} = -V_{S-off-a} + V_D + V_{SC4} \\ V_{L5} = -V_{S-off-a} + V_D + V_{SC4} + V_{SC5} \\ V_{L6} = -V_{S-off-a} + V_D + V_{SC4} + V_{SC5} + V_{SC6} \end{cases}, \tag{5.51}$$

where $V_{S\text{-}off\text{-}a}$ is the voltage of the secondary winding at the end of $T_{off\text{-}a}$. The voltage of C_i, V_{Ci}, varies between V_{Ui} and V_{Li};

$$V_{Li} \le V_{Ci} \le V_{Ui}. \tag{5.52}$$

After I_{LM} decreases to zero, the operation shifts to $T_{off\text{-}b}$ periods, in which all the diodes and switches are turned off and no current flows. By repeating these three periods (T_{on}, $T_{off\text{-}a}$, and

$T_{off\text{-}b}$), the energies of the series-connected SCs are redistributed to the SCs via the equalizer. Throughout the energy redistribution process, cell voltage imbalance is automatically eliminated. The voltage equalization mechanism will be mathematically proven using a dc equivalent circuit in the following section.

5.7.2.2 DC Equivalent Circuit

Substituting (5.51) into (5.48) yields

$$\Delta V_{Ci} = \left(V_{S-on} + V_{S-off-a} - 2V_D - V_{SCi}\right)e_i . \tag{5.53}$$

In general, the amount of charge delivered by a capacitor is given by

$$\Delta Q = C\Delta V = It = \frac{I}{f} . \tag{5.54}$$

From (5.53) and (5.54),

$$\left(V_{S-on} + V_{S-off-a}\right) - V_{SCi} - 2V_D = \frac{I_i}{C_i f e_i} , \tag{5.55}$$

where I_i is the average current flowing toward SC_i. From Ohm's law, the inverse of $C_i f$ is found to have a unit of resistance and can be replaced with an equivalent resistance of R_{eqi}, yielding

$$\left(V_{S-on} + V_{S-off-a}\right) - V_{SCi} - 2V_D = \frac{I_i R_{eqi}}{e_i} . \tag{5.56}$$

Equation (5.56) derives the dc equivalent circuit for the proposed equalizer, shown in Fig. 5.7.5. All SCs are connected to the voltage sources, $V_{S\text{-}on}$ and $V_{S\text{-}off\text{-}a}$, via two diodes and one equivalent resistor. $V_{S\text{-}on}$ is constant as long as the total voltage of V_{SC1}–V_{SC6} is constant, as expressed by (5.46), whereas $V_{S\text{-}off\text{-}a}$ varies depending on V_{Li}, as expressed by (5.51). Hence, $V_{S\text{-}on}$ and $V_{S\text{-}off\text{-}a}$ in (5.56) are expressed as a constant voltage source and a variable voltage source, respectively, in the dc equivalent circuit.

The dc equivalent circuit indicates that SCs with low voltage are preferentially charged by $V_{S\text{-}on}$ and $V_{S\text{-}off\text{-}a}$ via the equivalent resistors because of the common voltage sources. On the other hand, SCs with higher voltages in a practical circuit discharge to the input of the equalizer, and their voltages decrease. Finally, all SC voltages converge to ($V_{S\text{-}on} + V_{S\text{-}off\text{-}a} - 2V_D$).

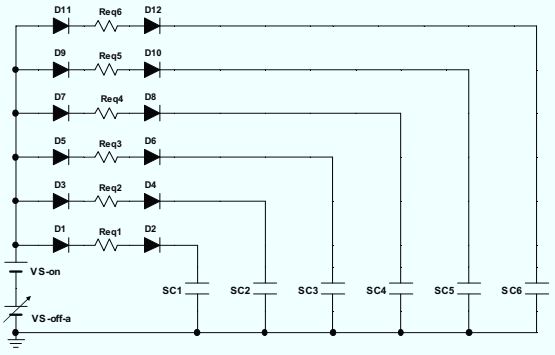


Fig. 5.7.5. DC equivalent circuit of the proposed equalizer.

5.7.2.3 Operation under Cell-Voltage-Imbalanced Condition

The fundamental operations under the cell-voltage-balanced condition in the previous section are conserved even under cell-voltage-imbalanced conditions. However, currents under voltage-imbalanced conditions preferentially flow toward the SC(s) with the lowest voltage. The current flow directions in an example case where V_{SC1} is lowest are shown in Fig. 5.7.6. The secondary winding provides only a current flowing through C_1. This indicates that only V_{C1} varies while others remain constant. In other words, ΔV_{C2}–ΔV_{C6} in (5.48) and (5.53) are zero. Based on (5.54) and (5.55), $\Delta V_{Ci} = 0$ which means $I_i = 0$ in the dc equivalent circuit, and hence, no currents flow toward SC_2–SC_6 in the example case. The energies of SC_1–SC_6 are preferentially redistributed to SC_1, which has the lowest voltage.

5.7.2.4 Duty Cycle Limitation

In order for the proposed equalizer to operate in DCM, duty cycle, D, must be properly chosen so that the $T_{off\text{-}b}$ period exists. The criterion to ensure DCM operation is given by

$$D_a < 1 - D, \tag{5.57}$$

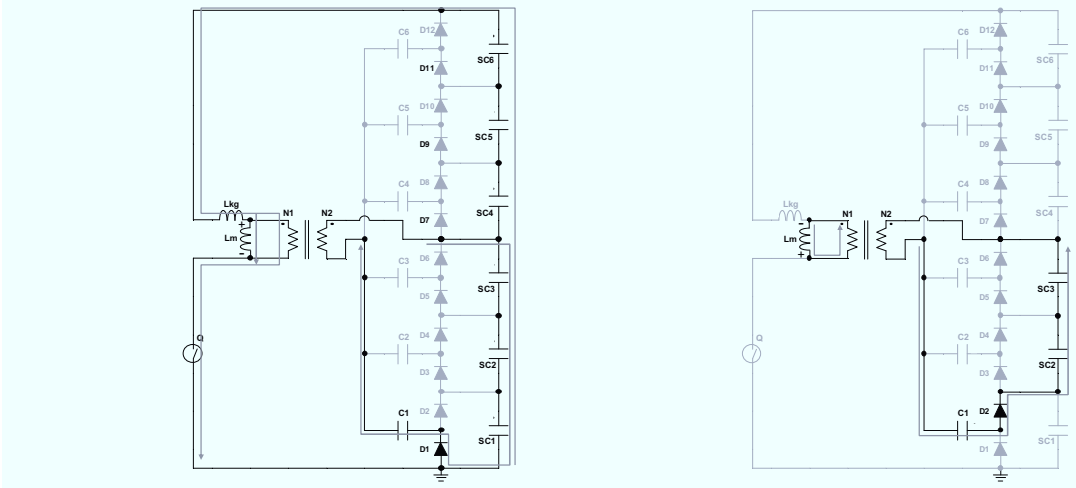
where

$$D_a = \frac{T_{off-a}}{T_S}, \tag{5.58}$$

where T_S is the switching period. The voltage-time product of the secondary winding must be zero, yielding

$$DV_{S-on} = D_a V_{S-off-a}. \tag{5.59}$$

From (5.57) and (5.59),



(a) (b)

Fig. 5.7.6. Current flow directions during (a) T_{on} and (b) $T_{off\text{-}a}$ under cell-voltage-imbalanced condition.

$$D < \frac{V_{S-off-a}}{V_{S-on} + V_{S-off-a}}. \tag{5.60}$$

Equations (5.47), (5.51), (5.52), and (5.60) yield the critical duty cycle to ensure DCM operations, $D_{critical}$, which is expressed as

$$D_{critical} < 1 - \frac{V_{S-on}}{V_{SCi} + 2V_D}. \tag{5.61}$$

This equation indicates that $D_{critical}$ needs to be determined considering the lowest possible value of V_{SCi}, with which $D_{critical}$ is the smallest.

5.7.3 Experiment

Fig. 5.7.7 shows a prototype of the proposed single-switch cell voltage equalizer for six cells. Smoothing capacitors, C_{out1}–C_{out6}, which are not illustrated in Fig. 5.7.1, were connected to SC_1–SC_6 in parallel. Component values of the prototype are shown in Table 5.3. The prototype was operated with a fixed duty cycle D = 0.3 at a switching frequency of 50 kHz. An experimental equalization test was performed for six SCs connected in series. SCs each with a capacitance of 500 F at a rated charge voltage of 2.5 V were equalized from an initially cell-voltage-imbalanced condition.

The resultant equalization profiles are shown in Fig. 5.7.8. Voltages of SCs with low initial voltages (V_{SC1} and V_{SC2}) increased, while others with high initial voltages decreased. The voltage imbalance was gradually eliminated as time elapsed, and the standard deviation of cell voltages 4 h after the start of the experiment decreased to approximately 3 mV. The SC voltages at that moment were 1.8 V, and the average power conversion efficiency during experimental

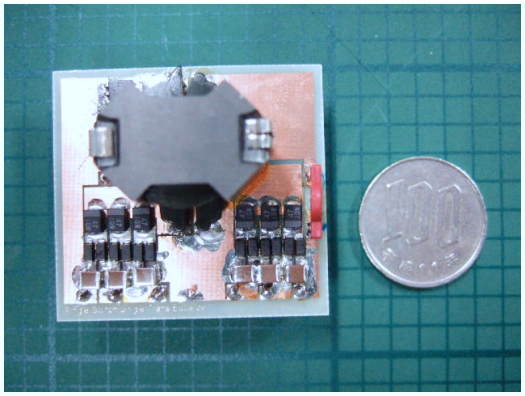


Fig. 5.7.7. Photographs of the prototype of the proposed equalizer.

Table 5.3. Component values for the prototype.

C_1–C_6	Tantalum Capacitor, 47 μF, 16 V
C_{out1}–C_{out6}	Ceramic Capacitor, 100 μF, 6.3 V
D_1–D_{12}	Schottky Diode, CRS08, V_D = 0.36 V
Transformer	$N_1:N_2$ = 17:2, L_m = 1.13 mH, L_{kg} = 44 μH
Q	N-Ch MOSFET, HAT2266H, R_{on} = 9.2 mΩ

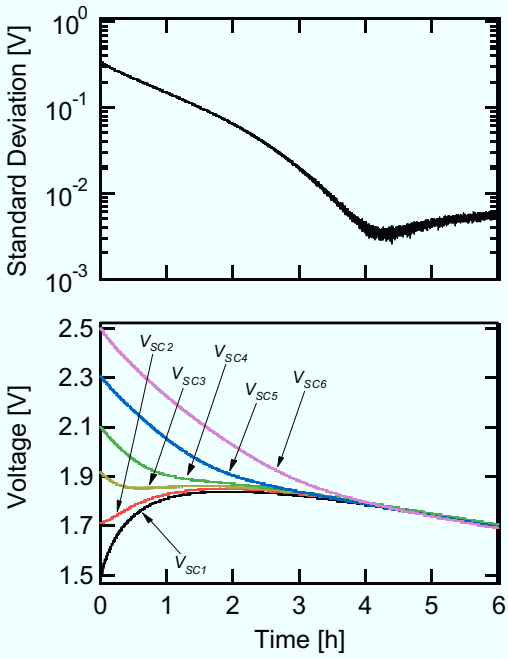


Fig. 5.7.8. Experimental equalization profiles.

equalization was calculated to be 78.7%.

The SC voltages continued decreasing even after the cell voltage imbalance was eliminated. This gradual decrease was due to the power conversion loss in the equalizer during energy circulations. Although energies extracted from the SCs are then redistributed to SCs via the cell voltage equalizer, some amount of energy is dissipated during energy redistribution processes. Therefore, the equalizer should be disabled after the equalization is completed in order not to waste the energies of SCs.

5.7.4 Conclusions

The single-switch cell voltage equalizers using voltage multipliers for series-connected energy storage cells was proposed. The transformer in the proposed equalizer operate in two modes; forward- and flyback-mode during the switch is on and off, respectively. In the DCM operation, the magnetizing current of the transformer can be limited without feedback control, and hence the proposed equalizer can be operate even with fixed duty cycle, eliminating the feedback control loop.

Experimental equalization tests were performed for six series EDLCs using the prototype operating in DCM with a fixed duty cycle. Cell voltage imbalance was gradually eliminated, and the standard deviation of cell voltages decreased approximately 3 mV at the end of the experiment, demonstrating the effectiveness of the proposed equalizer.

5.8 Comparison

In order to discuss the circuit complexity, the proposed equalizers are compared with conventional ones in terms of the number of active and passive components required in Table

Table 5.4. Comparison between conventional and proposed cell voltage equalizers in terms of number of circuit components required.

Topology		Active Component	Passive Component				
		Switch	Resistor	Inductor	Capacitor	Diode	Transformer
Dissipative Equalizer	Resistor Equalizer	-	n	-	-	-	-
	Zener Diode Equalizer	-	-	-	-	n	-
	Shunting Equalizer	n	n	-	-	-	-
Individual Cell Equalizer	Switched Capacitor	$2n$	-	-	n - 1	-	-
	Buck-Boost Converter	$2n - 1$	-	n - 1	-	-	-
Multi-Winding Transformer Equalizer	Flyback Converter	1	-	-	-	n	1 (Single core with (n + 1) windings)
	Forward Converter	2	-	-	-	n + 2	1 (Single core with (n + 1) windings)
Selection Switch Equalizer	Flying Capacitor	$2n$	-	-	1	-	1 (Single core with $2n$ windings)
	Flyback Converter	$2n$ + 1	-	-	-	1	1
Series-Parallel Reconfigurable Equazlier		$4n$	-	-	-	-	-
Single-Switch Multi-Stacked Buck-Boost Converter	SEPIC- and Zeta-based	1	-	n + 1	n	n	-
	SEPIC, Zeta, and Ćuk with a Transformer	1	-	n + 1	n + 1	n	1
Single-Switch Voltage Multiplier		1	-	-	n	$2n$	1

(Smoothing capacitor is excluded)

5.4. Since the proposed series-parallel reconfigurable equalizer essentially consists of three strings in parallel, its circuit complexity can not be fairly compared with other topologies. Hence, the series-parallel equalizer is excluded in the following comparisons.

The number of switches required in conventional equalizers, except for dissipative equalizers using resistors or diodes, and multi-winding transformer-based equalizers, is directly proportional to the number of series connections of energy storage cells, n. As already explained in Section 5.2, the number of switches is considered to be a good index for representing a circuit's complexity because switches require driver ICs and/or ancillary components. For example, drive circuits consisting of opto-couplers and auxiliary transistors can be found elsewhere [1], [29]–[31]. In conventional equalizers, in addition to multiple switches and drive circuits, floating drive circuits are required in cases where N-channel MOSFETs are used as high-side switches. However, the proposed multi-stacked SEPIC- and Ćuk-based equalizers shown in Figs. 5.6.2(a) and (c), and the voltage multiplier-based equalizer shown in Fig. 5.7.1, do not require floating drivers because the switch is connected to the ground. Therefore, in the proposed cell voltage equalizers, both the number of switches and the complexity of the drive circuit can be reduced in comparison with conventional equalizers.

Multi-winding transformer-based equalizers [4],[5] can reduce the number of switches and/or passive components. They are advantageous over other topologies in terms of the number of circuit components required. However, they need a multi-winding transformer, resulting in a poor design flexibility in terms of modularity and design difficulty (i.e., parameter matching among multiple secondary windings), as discussed in Section 5.3.2.2. In contrast, the proposed multi-stacked buck-boost converter equalizers and voltage multiplier equalizer are operable with a normal transformer; and besides, the SEPIC- and Zeta-based multi-stacked equalizers are operable even without the use of transformers. The lack of feedback control, which was discussed in Sections 5.6.2 and 5.7.1, is another major advantage provided by the proposed cell voltage equalizers. Thus, the proposed equalizers offer both circuit simplicity and better design flexibility. Although the proposed single-switch equalizers are considered reliable because of reduced component count, a safety measure against cell failures, such as short and open failures, need to be taken as similar to conventional battery systems.

The equalizers using multi-stacked buck-boost converters require multiple inductors

proportional to the number of series connection. The voltage multiplier-based equalizer, on the other hand, requires only one magnetic component (i.e., a transformer). Therefore, in a comparison between the proposed two equalizers, the multi-stacked buck-boost converter-based equalizers would find applications in which relatively small number of series connections is required, while the equalizer using a voltage multiplier would be advantageous for applications needing relatively large number of series connections.

5.9 Chapter Conclusions

This chapter described cell voltage equalizers for SCs in spacecraft power systems. Conventional dissipative and nondissipative cell voltage equalizers were reviewed, and their features and underlying drawbacks were explained.

During equalization process, high-frequency charge-discharge cycling, which may cause premature deterioration of energy storage cells, is likely to be induced by cell voltage equalizers. Experimental high-frequency cycling tests were performed, and the experimental results suggest that switching frequency of cell equalizers should be properly determined if equalizers are designed for lithium-ion cells. Meanwhile, the high-frequency cycling is expected not to have negative impact on SCs.

Three novel cell voltage equalizers were proposed, and their equalization performances were experimentally demonstrated using series-connected EDLCs. The proposed equalizers were compared with the conventional ones in terms of the number of circuit components required. The proposed equalizers are considered advantageous over the conventional ones in terms of not only the number of component but also modularity and design flexibility including the lack of parameter matching and feedback control.

References

[1] C. Pascual and P. T. Krein, "Switched capacitor system for automatic series battery equalization," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, pp. 848–854, Feb. 1997.

[2] J. W. Kimball, B. T. Kuhn and P. T. Krein, "Increased performance of battery packs by active equalization," in *Proc. IEEE Vehicle Power Propulsion Conference*, pp. 323–327, Sep. 2007.

[3] K. Nishijima, H. Sakamoto and K. Harada, "A PWM controlled simple and high performance battery balancing system," in *Proc. IEEE Power Electronics Specialist Conference*, pp. 517–520, Jun. 2000.

[4] N. H. Kutkut, D. M. Divan and D. W. Novotny, "Charge equalization for series connected battery strings," *IEEE Transactions on Industry Applications*, vol. 31, no. 3, pp. 562–568, May/Jun. 1995.

[5] N. H. Kutkut, H. L. N. Wiegman, D. M. Divan and D. W. Novotny, "Design considerations for charge equalization of an electric vehicle battery system," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 28–35, Jan. 1999.

[6] S. West and P. T. Krein, "Equalization of valve-regulated lead-acid batteries: issues and life test results," in *Proc. International Telecommunications Energy Conference*, pp. 439–446, Sep. 2000.

[7] K. Asakura, M. Shimomura and T. Shodai, “Study of life evaluation methods for Li-ion batteries for backup applications,” *J. Power Sources*, vol. 119–121, pp. 902–905, 2003.
[8] S. D. Gerner and T. E. Ruhlmann, “Effect of ac ripple on VRLA battery performance,” in *Proc. Battocom 99*, pp. 12.1–12.8, 1999.
[9] R. F. Nelson and M. A. Kepros, “AC ripple effects on VRLA batteries in float applications,” in *Proc. Annual Battery Conference on Applications and Advances*, pp. 281–289, Jan. 1999.
[10] A. Cuadras and O. Kanoun, “SoC Li-ion battery monitoring with impedance spectroscopy,” in *Proc. International Multi-Conference on System, Signals and Devices*, pp. 1–5, Mar. 2009.
[11] J. Y. Song, H. H. Lee, Y. Y. Wang and C. C. Wan, “Two- and three-electrode impedance spectroscopy of lithium-ion batteries,” *J. Power Sources*, vol. 111, pp. 255–267, 2002.
[12] D. Zhang, B. S. Haran, A. Durairajan, R. E. White, Y. Podrazhansky and B. N. Popov, “Studies on capacity fade of lithium-ion batteries,” *J. Power Sources*, vol. 91, pp. 122–129, 2000.
[13] G. Nagasubramanian, “Two- and three-electrode impedance studies on 18650 Li-ion cells,” *J. Power Sources*, vol. 87, pp. 226–229, 2000.
[14] J. C. Puippe and N. Ibl, “Influence of charge and discharge of electric double layer in pulse plating,” *J. Applied Electrochemistry*, vol. 10, pp. 775–784, 1980.
[15] T. Amemiya, K. Hashimoto and A. Fujishima, “Faradic charge transfer with double-layer charging and/or adsorption-related charging at polymer-modified electrodes as observed by color impedance spectroscopy,” *J. Physical Chemistry*, vol. 97, pp. 9736–9740, 1993.
[16] M. Broussely, Ph. Biensan, F. Bonhomme, Ph. Blanchard, S. Herreyre, K. Nechev and R. J. Staniewicz, “Main aging mechanisms in Li ion batteries,” *J. Power Sources*, vol. 146, pp. 90–96, 2005.
[17] B. E. Conway, “Electrochemical supercapacitors: scientific fundamentals and technological applications,” New York: Springer, 1999, pp. 121–124.
[18] K. Amine, C. H. Chen, J. Liu, M. Hammond, A. Jansen, D. Dees, I. Bloom, D. Vissers and G. Henriksen, “Factors responsible for impedance rise in high power lithium ion batteries,” *J. Power Sources*, vol. 97–98, pp. 684–687, 2001.
[19] X. Wang, Y. Sakiyama, Y. Takahashi, C. Yamada, H. Naito, G. Segami, T. Hironaka, E. Hayashi and K. Kibe, “Electrode structure analysis and surface characterization for lithium-ion cells simulated low-Earth orbit satellite operation I. Electrochemical behavior and structure analysis,” *J. Power Sources*, vol. 167, pp. 162–170, 2007.
[20] B. Markovsky, A. Rodkin, Y. S. Cohen, O. Palchik, E. Levi, D. Aurbach, H. J. Kim and M. Schmidt, “The study of capacity fading processes of Li-ion batteries: major factor that play a role,” *J. Power Sources*, vol. 119–121, pp. 119–121, 2003.
[21] X. Wang, Y. Sone and S. Kuwajima, “Effect of operation conditions on simulated low-earth orbit cycle-life testing of commercial lithium-ion polymer cells,” *J. Power Sources*, vol. 142, pp. 313–322, 2005.
[22] F. Z. Peng, “A Generalized Multilevel Inverter Topology with Self Voltage Balancing,” *Transactions on Industry Applications, IEEE*, vol. 37, no. 2, pp. 611–618, March/April 2000.

[23] V. Eng and C. Bunlaksananusorn, “Modeling of a SEPIC converter operating in continuous conduction mode,” in *Proc. 6th ECTI-CON*, pp. 136–139, May 2009.
[24] V. Eng and C. Bunlaksananusorn, “Modeling of a SEPIC converter operating in discontinuous conduction mode,” in *Proc. 6th ECTI-CON*, pp. 140–143, May 2009.
[25] D. S. L. Simonetti, J. Sebastián and J. Uceda, “The ciscontinuous conduction mode Sepic and Ćuk power factor preregulators: analysis and design,” *IEEE Transactions on Industrial. Electronics*, vol. 44, no. 5, pp.630–637, Oct. 1997.
[26] C. H. Kim, H. S. Park, C. E. Kim, G. W. Moon, and J. H. Lee, “Individual charge equalization converter with parallel primary winding of transformer for series connected lithium-ion battery strings in an HEV,” *J. Power Electronics*, vol. 9, no. 3, pp.472–480, May 2009.
[27] M. Uno and A. Kukita, “Charge equalizer using a Cockcroft-Walton voltage multiplier for series-connected supercapacitors,” *IEEE International Telecommunications Energy Conference*, pp. 1–4, Oct. 2009.
[28] M. Uno and K. Tanaka “Single-switch single-inductor equalization charger using a voltage multiplier for series-connected energy storage modules,” *IEEE International Conference on. Power Electronics, ICPE 2011-ECCE Asia*, pp. 2985–2989, May/Jun. 2011.
[29] H. S. Park, C. H. Kim, K. B. Park, G. W. Moon and J. H. Lee, “Design of a charge equalizer based on battery modularization,” *IEEE Transactions on Vehicular Technology*, vol. 58, pp. 3216–3223, Sep. 2009.
[30] C. H. Kim, M. Y. Kim, J. H. Kim and G. W. Moon, “Modularized charge equalizer with intelligent switch block for lithium-ion batteries in an HEV,” in *Proc. 31st Annual International Telecommunications Energy Conference*, pp. 1–6, Oct. 2009.
[31] M. Tang and T. Stuart, “Selective buck-boost equalizer for series battery pack,” *IEEE Transactions on Aerospace and. Electronic Systems*, vol. 36, no. 1, pp.201–211, Jan. 2000.

Chapter 6
Equalization Charger

6.1 Introduction

Some of nondissipative cell voltage equalization techniques, presented in the previous chapter, can be incorporated with chargers, and then can be transformed into an equalization charger that is a charger having cell voltage equalization function. By integrating a charger and equalizers into one unit, the configuration of the entire power system can be simplified compared with conventional systems which have a charger and equalizers separately.

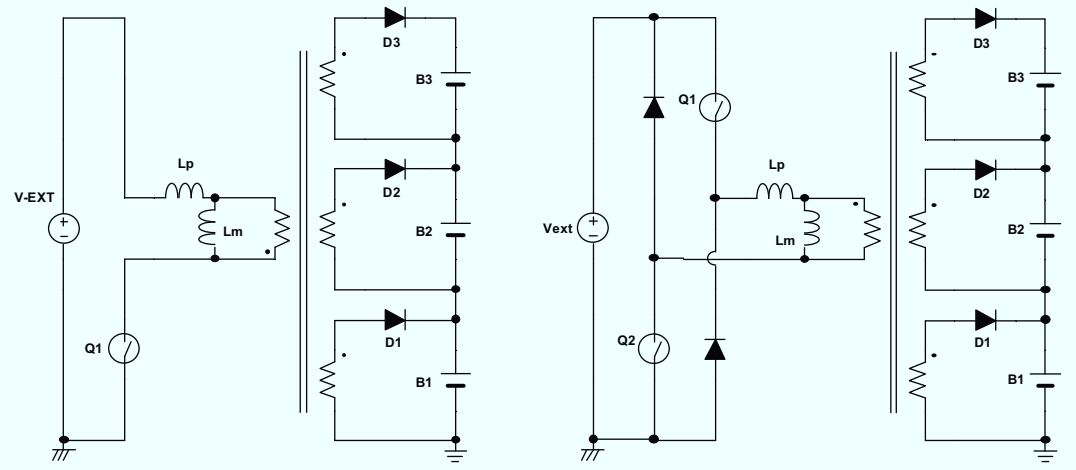
This chapter reviews conventional equalization chargers, and then proposes two novel topologies of single-switch equalization chargers which are based on the single-switch cell voltage equalizers introduced in the previous chapter.

6.2 Equalization Charger vs. Charger with Equalizers

Primary benefit of an integrated system (i.e., a system using an equalization charger) is that entire power system configuration can be simplified by integrating a charger and equalizers into one unit. However, since the two components, i.e., a charger and equalizers, are integrated, simultaneous optimization for both functions is difficult. Therefore, the integrated system is considered to find applications in relatively small power systems where reducing the number of power system components would be more effective than optimizing performance, such as efficiency and equalization speed, in order to contribute to system mass reduction.

On the other hand, in ordinary separate systems, which have a charger and equalizers separately, the efficiency improvement and optimal design for a charger can be done more effectively than in the integrated system. Therefore, the separate system would be more suitable for large energy systems, in which maximizing a power conversion efficiency of a charger would have greater impact on system mass reduction than eliminating equalizers by integrating. The impact of efficiency improvement for chargers on system mass was shown in Fig. 4.4.4.

Based on the mass calculation equations developed in Section 4, the integrated system and separate system can be compared from the viewpoint of the system mass. In order for the integrated system to be advantageous, the mass increase of PV arrays due to the lower efficiency of the equalization charger must be justified with the mass reduction thanks to the integration of charger and equalizers. Generally, power requirement for equalizers in the separate system is negligibly small compared with that for chargers as mentioned in the previous chapter; approximately 1/100 of the charge power requirement is necessary for equalizers to eliminate voltage imbalance originating from nonuniform cell properties [1],[2]. Therefore, the mass of equalizers is expected almost independent on charge power requirement, and assuming constant mass, which mainly comes from cables, connectors, and metal chassis, is deemed suitable. Assuming that ρ_{PV} of 60 W/kg, m_{cha} of 7 kg/kW for both the charger and equalization charger, η_{cha} of 90% and 85% for the charger and equalization charger, respectively, and a fixed mass of 0.3 kg for the equalizer, the integrated system would be advantageous over



(a) (b)

Fig. 6.3.1. Conventional equalization charger using a multi-winding transformer based on (a) flyback converter and (b) forward converter.

the integrated system below approximately 300 W charge power requirement. Therefore, all the experiments in this chapter are done with relatively low charge powers.

6.3 Conventional Equalization Chargers

Conventional equalization chargers, shown in Fig. 6.3.1, are basically multi-output converters using a multi-winding transformer [3],[4]. Flyback- and forward-based equalization chargers, shown Figs. 6.3.1(a) and (b), respectively, are very similar to the cell voltage equalizers using a multi-winding transformer shown in Figs. 5.3.6(a) and (b), in which energies of series-connected cells are preferentially redistributed to the cell(s) with the lowest voltage via the equalizers. Fundamental operation of the equalization charger shown in Figs. 6.3.1(a) and (b) is similar to that of the equalizers, except that the external power source supplies energies to the series-connected cells via the multi-winding transformer. Energies supplied from the external power source are preferentially redistributed to the cell(s) with the lowest voltage, and cell voltage imbalance is eventually eliminated as charging proceeds.

These equalization chargers have identical drawbacks as those of the multi-winding transformer-based equalizers; poor modularity, design difficulty of multi-winding transformers, and possible cell voltage imbalance caused by parameter mismatching among multiple secondary windings. Hence, the applications of these equalization chargers are limited to the batteries/modules with small number of series connection.

6.4 Single-Switch Equalization Charger Based on Multi-Stacked Buck-Boost Converters

The cell voltage equalizers, proposed in Section 5.6, can be transformed to equalization chargers. In this section, single-switch equalization chargers that are based on multi-stacked buck-boost converters are proposed. The proposed chargers not only equalize the individual SC voltages but also charge SCs at CP with a fixed duty cycle operation. Since the CP charging

scheme contributes to size and mass reduction of PV arrays, as discussed in Section 4.3, these equalization chargers having CP charging scheme are considered suitable for SC-based power systems. The single-switch operation without feedback control simplifies the circuit and eliminates the feedback loop, thus reducing the circuit complexity dramatically compared with the conventional equalizers and chargers.

6.4.1 Circuit Description and Major Features

Similar to the cell voltage equalizers presented in Section 5.6, the conventional buck-boost converters including single-ended primary inductor converter (SEPIC), Zeta, and Ćuk converters shown in Fig. 5.6.1 can be used as the basic topology for the proposed equalization chargers. For equalization chargers, Ćuk topology can be used without an isolation transformer because the input of the charger is not tied to the series connection of SCs. The proposed chargers can be derived by stacking a circuit consisting of C, D, and L_{out} of the conventional converters. Fig. 6.4.1 shows the representative circuit descriptions of the proposed chargers for four SCs connected in series. The circuit consisting of C_{in}, L_{in}, Q, C_1, L_1, D_1, and SC_1 is identical to the conventional converters shown in Fig. 5.6.1, and therefore, the proposed chargers can be considered multi-stacked buck-boost converters.

The required number of switches in chargers is a good indicator of circuit complexity because each switch requires a drive circuit that includes ICs and ancillary components such as resistors, capacitors, and diodes. Because the proposed equalizers need only one switch, only one drive circuit is required, thus dramatically reducing the circuit complexity compared with conventional equalizers that use multiple switches.

Modularity (or extendibility) is also important for equalization chargers because the number of series connections of SCs varies depending on the application and power requirement. As mentioned in the previous section, multi-winding transformer-based equalizers are rated poor in terms of modularity because of the difficulty of realizing parameter matching among multiple secondary windings. On the other hand, in the proposed equalization chargers, the number of series connections can be arbitrarily extended by stacking the circuit of C_i-D_i-L_i. Parameter matching is not a strict requirement because voltages and currents of SCs are not dependent on component values such as inductance and capacitance, as mathematically expressed in the following section.

In addition to the reduced number of switches and good modularity, the proposed equalization chargers can eliminate the feedback control circuit when operated in the discontinuous conduction mode (DCM). In DCM operations, the input power can be constant as long as the input voltage is constant, as discussed in the next section. Therefore, although a feedback control loop, which usually consists of error amplifiers, phase compensators, comparators, and voltage monitors, is eliminated from the charger, series-connected SCs can be charged at CP. The simplified circuit has increased reliability, and hence, the proposed CP equalization chargers are considered suitable for SCs in spacecraft power systems where reliability is of primary importance.

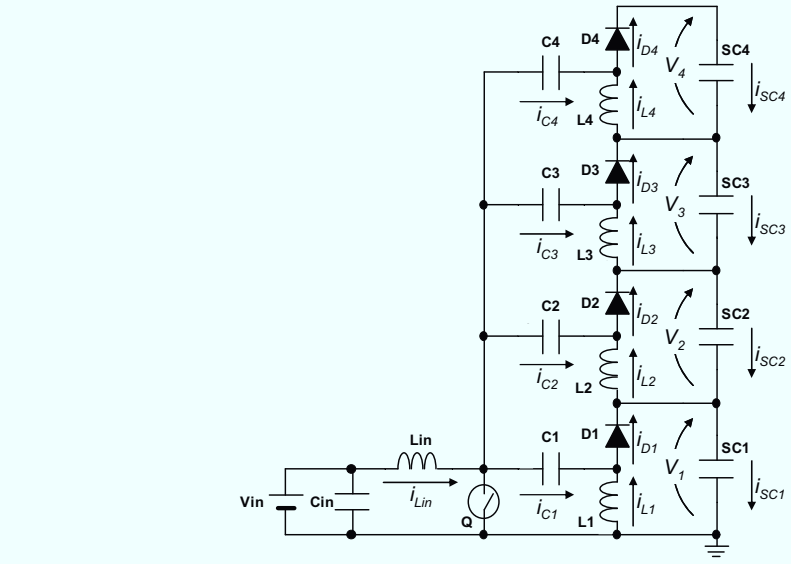
6.4.2 Operation Analysis

Operations of the proposed CP equalization chargers are very similar to that of conventional

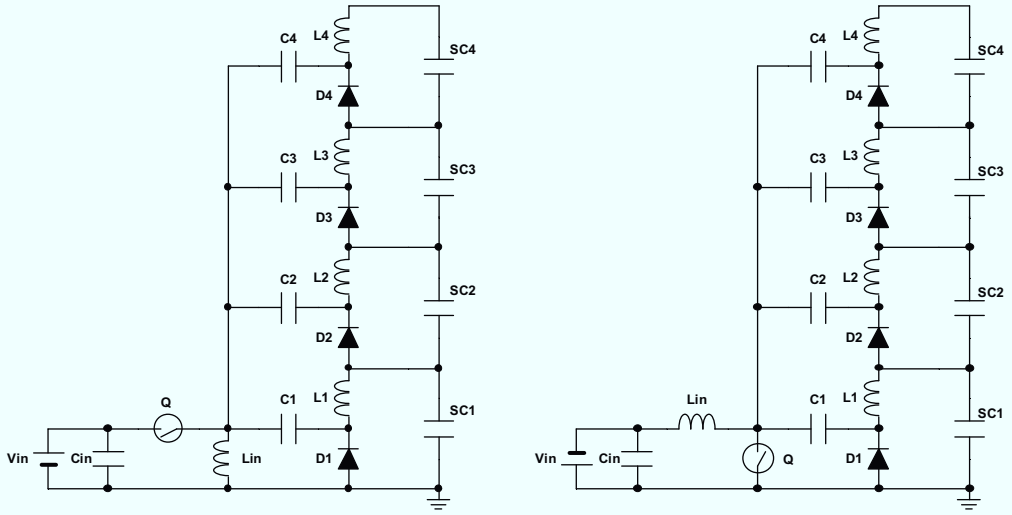
buck-boost converters. Conventional buck-boost converters operating in DCM have been used in power factor correction applications [5]. The input current of buck-boost converters can be restricted to desired levels in the DCM operation even without feedback control. In this section, as a representative case, we analyze the operation of the SEPIC-based topology shown in Fig. 6.4.1(a).

6.4.2.1 Operation under Cell-Voltage-Balanced Condition

Operation waveforms for the proposed equalization charger under a voltage-balanced condition are shown in Fig. 6.4.2 and are identical to those of the conventional SEPIC. The



(a)



(b) (c)

Fig. 6.4.1. Proposed single-switch equalization charger using multi-stacked buck-boost converters based on (a) SEPIC, (b) Zeta, and (c) Ćuk converters.

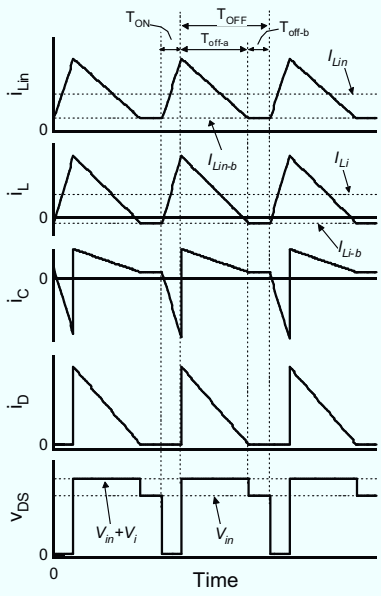


Fig. 6.4.2. Operation waveforms of the SEPIC-based equalization charger under a voltage-balanced condition.

current flow paths are shown in Fig. 6.4.3.

The average voltage of inductors under a steady state condition is zero. Therefore, the voltages of C_1–C_4, V_{C1}–V_{C4}, can be expressed as

$$\begin{cases} V_{C1} = V_{in} \\ V_{C2} = V_{in} - V_1 \\ V_{C3} = V_{in} - (V_1 + V_2) \\ V_{C4} = V_{in} - (V_1 + V_2 + V_3) \end{cases}, \tag{6.1}$$

where V_{in} is the input voltage and V_1–V_4 are the voltages of SCs as designated in Fig. 6.4.1(a).

The operation can be divided into three periods: T_{on}, $T_{off\text{-}a}$, and $T_{off\text{-}b}$ as shown in Fig. 6.4.2. When the switch is on, T_{on} period, all inductor currents increase and store the corresponding energies. During the $T_{off\text{-}a}$ period, the stored energies are delivered to each cell (SC_1–SC_4) through each diode. The diode currents linearly decrease during the $T_{off\text{-}a}$ period. After the diode currents become zero, the $T_{off\text{-}b}$ period starts and all inductor currents become constant.

The voltage–time product (or average voltage) of the inductors in a single switching cycle under a steady state condition must be zero, and hence

$$\begin{cases} DV_{C1} = D_a(V_1 - V_{D1}) \\ D(V_{C2} + V_1) = D_a(V_2 - V_{D2}) \\ D(V_{C3} + V_1 + V_2) = D_a(V_3 - V_{D3}) \\ D(V_{C4} + V_1 + V_2 + V_3) = D_a(V_4 - V_{D4}) \end{cases}, \tag{6.2}$$

where D is the duty cycle and V_{D1}–V_{D4} represent the forward voltage drop across diodes D_1–D_4, respectively. D_a is given by

$$D_a = \frac{T_{off-a}}{T_S}, \tag{6.3}$$

where T_S is the switching period. The voltage of SC_i (i = 1,…, 4), V_i, is expressed from (6.1)–(6.3) as

$$V_i = \frac{D}{D_a} V_{in} - V_{Di}. \tag{6.4}$$

This equation indicates that as long as V_{Di} is uniform, the equalization charger produces uniform output voltages for each individual SC.

For the equalization charger to operate in DCM, T_{off-b} period must exist and the following equation needs to be satisfied:

$$D_a < 1 - D. \tag{6.5}$$

From (6.4) and (6.5), the critical duty cycle to ensure DCM operation, $D_{critical}$, is given by

$$D_{critial} < \frac{V_i + V_{Di}}{V_{in} + V_i + V_{Di}}. \tag{6.6}$$

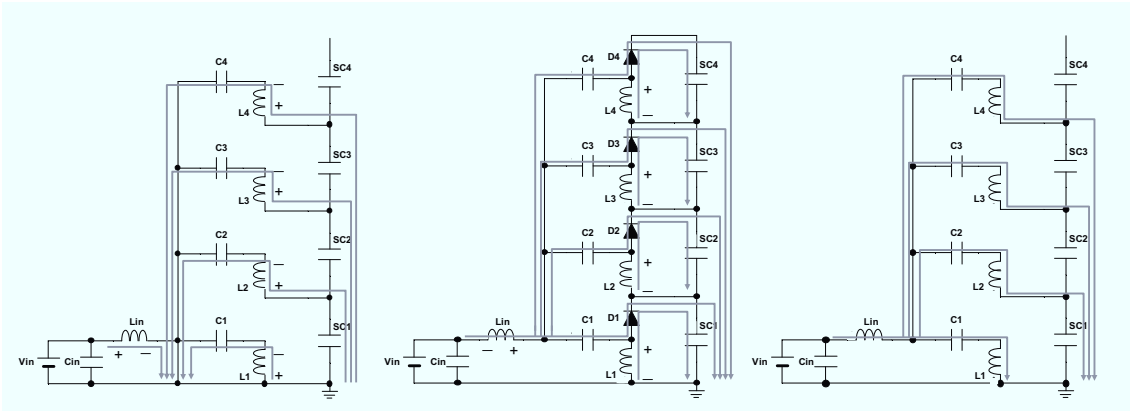
In the case where (6.6) is violated, the equalization charger starts to operate in the continuous conduction mode (CCM), in which feedback control is necessary.

From Fig. 6.4.2, the average currents of L_{in} and L_i, I_{Lin} and I_{Li}, are determined as

$$I_{Lin} = (D + D_a)\frac{V_{in} D T_S}{2L_{in}} + I_{Lin-b}, \tag{6.7}$$

$$I_{Li} = (D + D_a)\frac{V_{in} D T_S}{2L_i} + I_{Li-b}, \tag{6.8}$$

where I_{Lin-b} and I_{Li-b} are the currents through L_{in} and L_i, respectively, during the T_{off-b} period, as



(a) (b) (c)

Fig. 6.4.3. Current flow directions during (a) T_{on}, (b) T_{off-a}, and (c) T_{off-b} of the SEPIC-based equalization charger under a cell-voltage-balanced condition.

shown in Fig. 6.4.2. By assuming that the impedances of SC_1–SC_4 are negligible, $I_{Lin\text{-}b}$ is equally distributed among L_1–L_4 as long as the impedances of C_1-L_1–C_4-L_4 are uniform, thus yielding

$$I_{Lin-b} = -\left(I_{L1-b} + I_{L2-b} + I_{L3-b} + I_{L4-b}\right) = -4I_{Li-b}. \tag{6.9}$$

Similarly, during the $T_{off\text{-}a}$ period, i_{Lin} is also assumed to be distributed equally among C_1–C_4. The average current of C_i, I_{Ci}, which must be zero under a steady state condition, is determined from Fig. 6.4.2 as

$$I_{Ci} = I_{Li-b} + D\frac{V_{in}DT_S}{2L_i} - D_a\frac{V_{in}DT_S}{2\cdot 4L_{in}} = 0. \tag{6.10}$$

The relationship between I_{Lin} and I_{Li} is obtained from (6.7)–(6.10) as described below:

$$\frac{I_{Li}}{I_{Lin}} = \frac{D_a}{4D}. \tag{6.11}$$

From Fig. 6.4.2, the average current through D_i, I_{Di}, can be obtained as follows:

$$I_{Di} = D_a\left(\frac{V_{in}DT_S}{2\cdot 4L_{in}} + \frac{V_{in}DT_S}{2L_i}\right) = \frac{V_{in}DD_aT_S}{2}\left(\frac{4L_{in}+L_i}{4L_{in}L_i}\right). \tag{6.12}$$

As I_{Ci} is zero under a steady state condition, Kirchhoff's current law yields the relationship among I_{SCi}, I_{Li}, and I_{Di} as

$$I_{SCi} = I_{Li} = I_{Di}. \tag{6.13}$$

Equations (6.11)–(6.13) yield

$$I_{Lin} = \frac{V_{in}D^2T_S}{2}\left(\frac{4L_{in}+L_i}{L_{in}L_i}\right). \tag{6.14}$$

This equation indicates that I_{Lin} can be constant with a fixed value of D as long as V_{in} is kept constant. Hence, the proposed equalization charger operates as a CP charger in fixed duty cycle operations. However, because there is no feedback loop to regulate the SC voltages, SCs may become overcharged unless the charging process is stopped. Thus, although feedback control is not necessary, voltages of SCs should be monitored to disable the equalization charger when the voltages reach the desired charge voltage levels.

6.4.2.2 Operation under Cell-Voltage-Imbalanced Condition

Based on (6.4), the output voltages of the proposed charger are clamped by the SC(s) with the lowest voltage under a voltage-imbalanced condition. Therefore, only the SC(s) with the lowest voltage is (are) preferentially charged. In such cases, according to (6.13), only that inductor(s) and diode(s) connected to the SC(s) with the lowest voltage would exhibit nonzero values.

Fig. 6.4.4 shows the operation waveforms under a voltage-imbalanced condition. The asterisks (*) added to the symbols in Fig. 6.4.4 denote the subscript number of the SC(s) having the lowest voltage. Fig. 6.4.5 illustrates the current flow directions in the case where SC_1 has the lowest voltage. The current paths containing only ripple components are drawn as dashed lines. For example, I_{L*} in Fig. 6.4.5 corresponds to I_{L1}.

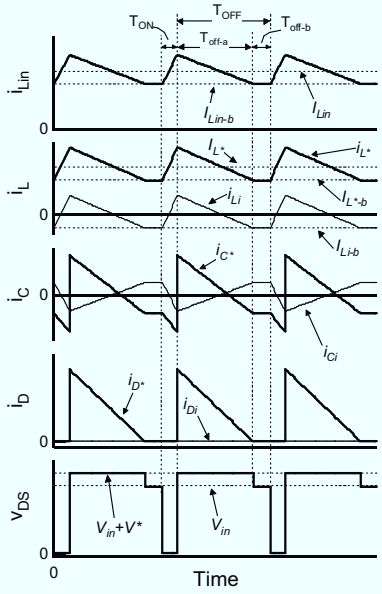


Fig. 6.4.4. Operation waveforms of the SEPIC-based equalization charger under a voltage-imbalanced condition.

The voltage–time product of inductors is zero even under a voltage-imbalanced condition, thus yielding

$$\begin{cases} DV_{C1} & = D_a\left(V_1 + V_{D1}\right) \\ D\left(V_{C2} + V_1\right) & = D_a\left(V_{C1} - V_{C2} + V_{D1}\right) \\ D\left(V_{C3} + V_1 + V_2\right) & = D_a\left(V_{C1} - V_{C3} - V_2 + V_{D1}\right) \\ D\left(V_{C4} + V_1 + V_2 + V_3\right) & = D_a\left(V_{C1} - V_{C4} - V_2 - V_3 + V_{D1}\right) \end{cases}. \tag{6.15}$$

From (6.1), (6.5), and (6.15), V_* and $D_{critical}$ under a voltage-imbalanced condition are obtained as

$$V_* = \frac{D}{D_a} V_{in} - V_{D*}, \tag{6.16}$$

$$D_{critial} < \frac{V_* + V_{D*}}{V_{in} + V_* + V_{D*}}. \tag{6.17}$$

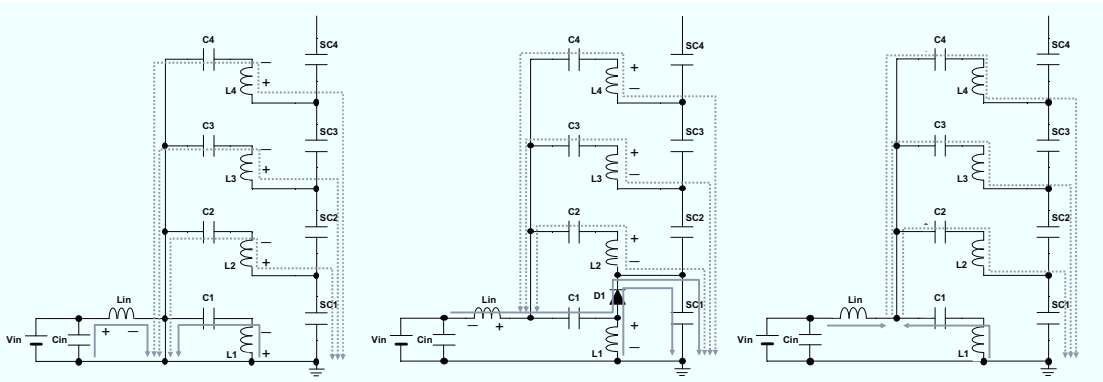
According to (6.16), output voltages from the equalization charger are clamped by the SC(s) having the lowest voltage V_*, and (6.17) indicates that $D_{critical}$ is not dependent on V_i (i.e., V_2–V_4 in the example case).

From Fig. 6.4.4, average currents of L$_*$ and L$_i$, I_{L*} and I_{Li}, are given by

$$I_{L*} = \left(D + D_a\right)\frac{V_{in} D T_S}{2L_*} + I_{L*-b}, \tag{6.18}$$

$$I_{Li} = \left(D + D_a\right)\frac{V_{in} D T_S}{2L_i} + I_{Li-b} = 0, \tag{6.19}$$

respectively.



(a) (b) (c)

Fig. 6.4.5. Current flow directions during (a) T_{on}, (b) $T_{off\text{-}a}$, and (c) $T_{off\text{-}b}$ of the SEPIC-based equalization charger under a cell voltage-imbalanced condition.

Equation (6.9) can be rewritten for a voltage-imbalanced condition as

$$I_{Lin-b} = -\left(I_{L*-b} + I_{L2-b} + I_{L3-b} + I_{L4-b}\right) = -\left(I_{L*-b} + 3I_{Li-b}\right). \tag{6.20}$$

Contrary to the voltage-balanced condition discussed in the previous section, i_{Li} (i.e., i_{L2}–i_{L4}) during the $T_{off\text{-}a}$ period flows toward C_1 under a voltage-imbalanced condition, as shown in Fig. 6.4.5(b). The average current of C_*, I_{C*}, is expressed as

$$I_{C*} = I_{L*-b} + D\frac{V_{in}DT_S}{2L_*} - D_a\frac{V_{in}DT_S}{2}\left(\frac{1}{L_{in}} + \frac{3}{L_i}\right) = 0. \tag{6.21}$$

Equations (6.7) and (6.18)–(6.21) yield

$$\frac{I_{L*}}{I_{Lin}} = \frac{D_a}{D}. \tag{6.22}$$

Assuming that $L_* = L_i$, I_{D*} is given by

$$I_{D*} = D_a\left(\frac{V_{in}DT_S}{2L_{in}} + \frac{V_{in}DT_S}{2L_*} + \frac{3V_{in}DT_S}{2L_i}\right) = \frac{V_{in}DD_aT_S}{2}\left(\frac{4L_{in} + L_i}{L_{in}L_i}\right). \tag{6.23}$$

This equation indicates that I_{D*} is four times larger than that under a voltage-balanced condition,

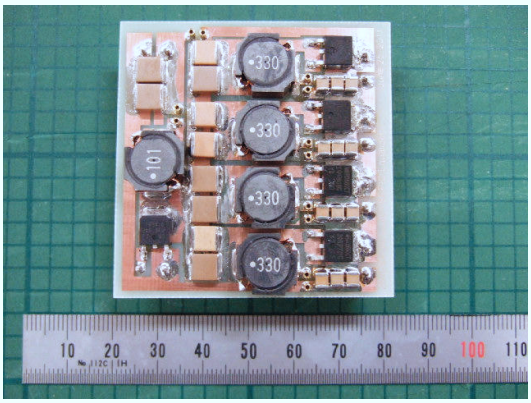


Fig. 6.4.6. A photograph of a 25 W prototype of the SEPIC-based CP equalization charger.

Table 6.1. Component values used for a 25 W prototype.

C_{in}	Ceramic Capacitor, 20 µF, 50 V
C_{out1}–C_{out4}	Ceramic Capacitor, 66 µF, 25 V
C_1–C_4	Ceramic Capacitor, 20 µF, 50 V
L_{in}	100 µH
L_1–L_4	33 µH
Q	N-Ch MOSFET, IRF3410, R_{on} = 39 mΩ
D_1–D_4	Schottky Diode, BRD660CT, V_D = 0.65 V

as expressed by (6.12). From (6.22) and (6.23), (6.14) is found to be conserved even under a voltage-imbalanced condition. Hence, the proposed equalization charger can operate as a CP charger even under a voltage-imbalanced condition.

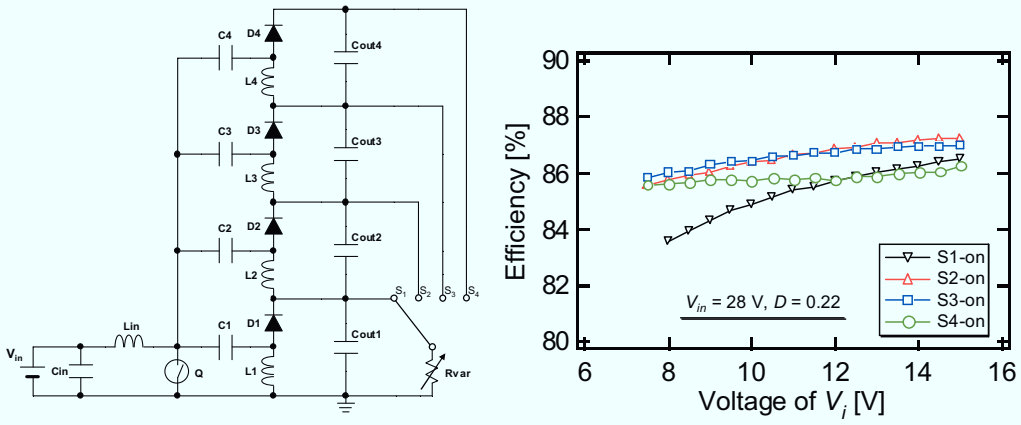
6.4.3 Experiment

A 25 W prototype of the SEPIC-based equalization charger for four series-connected SCs was designed, as shown in Fig. 6.4.6. The component values are shown in Table 6.1. The equalization charger was operated at 80 kHz with V_{in} = 28.0 V and a fixed duty cycle of 0.22.

Power conversion efficiencies of the prototype were measured by emulating both voltage-balanced and voltage imbalanced conditions. To this end, a variable resistor was connected to each intermediate tap, as shown in Fig. 6.4.7(a). For example, when S_1 is on, the voltage-imbalanced condition of $V_1 < V_i$ (i = 2, 3, and 4) can be emulated. Meanwhile, turning on S_2 emulates the case of $V_1 = V_2 < V_i$ (i = 3 and 4).

The measured power conversion efficiencies are shown in Fig. 6.4.7(b). The average efficiency was approximately 86%. Because the currents in the equalization charger were concentrated at L_*, C_*, and D_*, as discussed in Section 6.4.2.2, the lowest efficiency during the S_1-on period was believed to be because of the current concentrations at L_1, C_1, and D_1, which are prone to increase Joule losses.

An experimental charge test was performed for four EDLC modules in series, each with a capacitance of 220 F at a rated charge voltage of 15.0 V (shown in Fig. 6.4.8), from the



(a) (b)

Fig. 6.4.7. (a) Experimental setup for efficiency measurement and (b) the measured power conversion efficiencies.

Fig. 6.4.8. A photograph of an EDLC module.

voltage-imbalanced condition where the initial voltages of V_1–V_4 were 7.5, 9.5, 11.5, and 13.5 V, respectively.

The experimental charge profiles of the series-connected SCs are shown in Fig. 6.4.9. The input current was approximately 0.9 A during the entire experimental period. The charge current(s) flowed toward the EDLC(s) with the lowest voltage at each time instant, as can be seen from the top panel of Fig. 6.4.9. The voltage imbalance was gradually eliminated as charging progressed, and the equalization charger was disabled when V_1–V_4 reached 15.0 V. The standard deviation of the SC voltages decreased to approximately 50 mV at the end of the experiment.

The charging process was divided into four periods labeled as A–D, and the operation waveforms were measured during each period. The measured waveforms are shown in Fig. 6.4.10. During the $T_{off\text{-}b}$ periods, we observed oscillations due to the parasitic capacitance of the

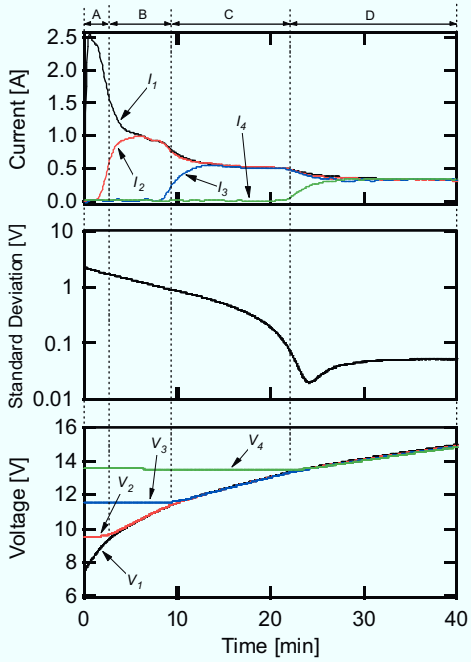


Fig. 6.4.9. Experimental charge profiles of the series-connected EDLC modules.

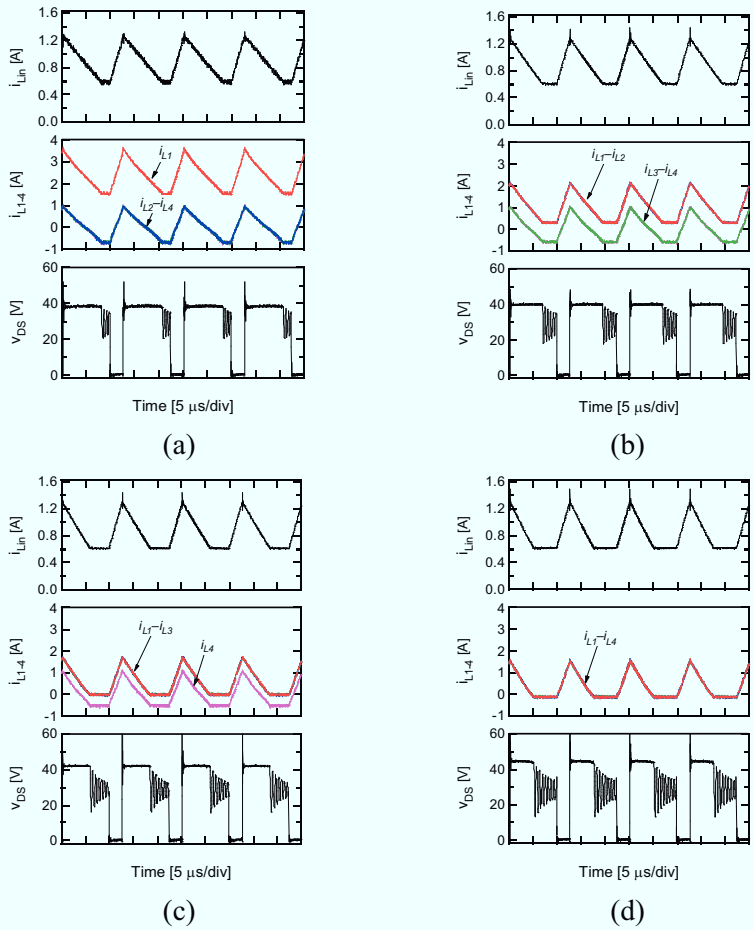


Fig. 6.4.10. Measured waveforms during the periods (a) A, (b) B, (c) C, and (d) D.

MOSFET switch and inductors. The average current of i_{Lin} was constant at approximately 0.9 A for the entire period and was independent of the voltage-imbalance, as can be seen from the top panels of Fig. 6.4.10(a)–(d). This demonstrates that the input power for the proposed equalization charger can remain constant without feedback control as long as the input voltage is constant.

During period A, in which V_1 was the lowest, the average of i_{L1} was positive, whereas i_{L2}–i_{L4} exhibited only ripple component and their averages were zero. During period B, when V_1 and V_2 were equal and the lowest, the averages of i_{L1} and i_{L2} were positive, whereas those of i_{L3} and i_{L4} were still zero. Similarly, as V_3 approached V_1 and V_2 during period C, i_{L1}–i_{L3} exhibited uniform current waveforms. Finally, during period D, all waveforms and averages of i_{L1}–i_{L4} became uniform and positive, respectively. According to (6.13), these results confirmed that the EDLC(s) with the lowest voltage at each time instant were preferentially charged using the equalization charger, as mathematically explained in Section 6.4.2.2.

6.4.4 Conclusions

Single-switch equalization chargers using multi-stacked buck-boost converters for the series-connected SCs were proposed in this section. The number of required switches can be dramatically reduced compared with conventional equalizers. In addition, to implement the CP

charging scheme, feedback control is not necessary for the proposed equalization chargers operating in DCM. The reduced number of switches and the elimination of feedback loops lead to increased reliability and suitability for satellite applications.

The SEPIC-based equalization charger was used as a representative topology, and its operations under both voltage-balanced and voltage-imbalanced conditions were mathematically analyzed. A 25 W prototype of the SEPIC-based equalization charger was designed and used for the experimental charge test performed for four EDLCs connected in series. The input power for the equalization charger was constant and independent of the voltages of EDLCs as long as the input voltage to the equalizer was constant. The resultant equalization charge profiles demonstrated that the EDLC(s) with the lowest voltage was (were) preferentially charged by the equalization charger. The voltage imbalance was gradually eliminated as charging progressed, and finally, all EDLCs were charged to a uniform voltage level.

6.5 Single-Switch Single-Inductor Equalization Charger Using Voltage Multiplier

The cell voltage equalizers based on voltage multiplier, presented in Section 5.7, also can be transformed into an equalization charger. This section proposes a single-switch single-inductor equalization charger based on voltage multiplier. The single-switch single-inductor operation can dramatically reduce the circuit complexity compared to that of conventional equalization chargers and equalizers.

6.5.1 Circuit Description and Major Features

Fig. 6.5.1 shows the proposed single-switch single-inductor equalization charger for three-series-connected energy storage modules. Each of the modules B_1–B_3 is connected in parallel to the two-series-connected diodes whose junctions are connected to energy-transfer capacitors, C_1–C_3. The circuit consisting of the series-connected diodes D_1–D_6, C_1–C_3, and B_1–B_3 can be regarded as a voltage multiplier.

Since magnetic components, such as inductors and transformers, are relatively large

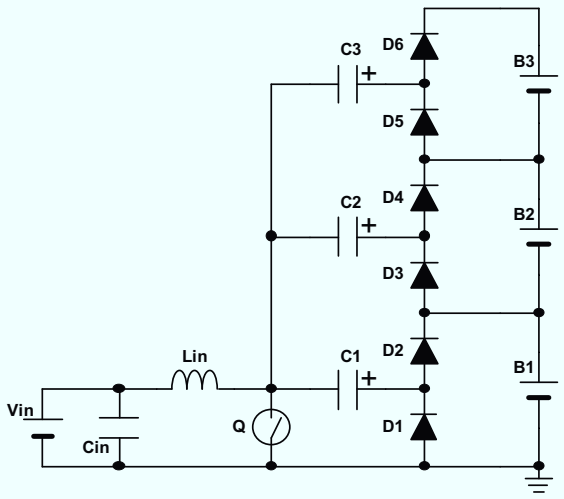


Fig. 6.5.1. Proposed single-switch single-inductor equalization charger using a voltage multiplier for series-connected energy storage modules.

components in electrical circuit, multiple use of magnetic components is not desirable from the viewpoint of the circuit size. The number of switch is considered to be a good index to represent a circuit complexity because switches require drive circuits including ICs and ancillary components. The proposed equalization charger consists of passive components, a solo magnetic component, L_{in}, and a sole active component, Q, so that the circuit size, complexity, and number of circuit components, such as switches and inductors, can be dramatically reduced compared with conventional equalization chargers and equalizers which consist of multi-winding transformer, numerous switches and/or inductors. However, since the currents of capacitors during on period in this equalization charger, shown in Fig. 6.5.2(a), are not limited with magnetic components such as inductors, possible large inrush current and consequent electro magnetic interference (EMI) are anticipated to make this topology less attractive.

The reliability is one of the most important consideration for energy storage applications because unwanted failures could cause dangerous consequences. In the conventional equalizers, in which switches are connected to energy storage cells/modules in parallel, short failures of switches may short cells/modules. In the proposed equalization charger, on the other hand, since the two-series-connected diodes are connected to each module, the possibility of short failures of modules through diodes is quite low. Moreover, the energy-transfer capacitors can protect the modules from being shorted in case of a short failure of Q. Thus, the proposed equalization charger is considered highly reliable. Metalized film capacitors, which offer very high reliability with self-healing property, can be used if the reliability of capacitors is also a concern.

6.5.2 Operation Analysis

Fig. 6.5.2 shows the current flow directions during operation. During the on period, B_1–B_2 discharge through the even-numbered diodes as shown in Fig. 6.5.2(a). All currents in the circuit flow to Q in this period. Because the capacitances of the energy storage modules B_1–B_3 are much larger than those of the energy transfer capacitors C_1–C_3, the variations in the module voltages V_{B1}–V_{B3} are small enough to be negligible during a single switching cycle. The voltages V_{C1A}–V_{C3A} across C_1–C_3 at the end of the on period can be expressed as

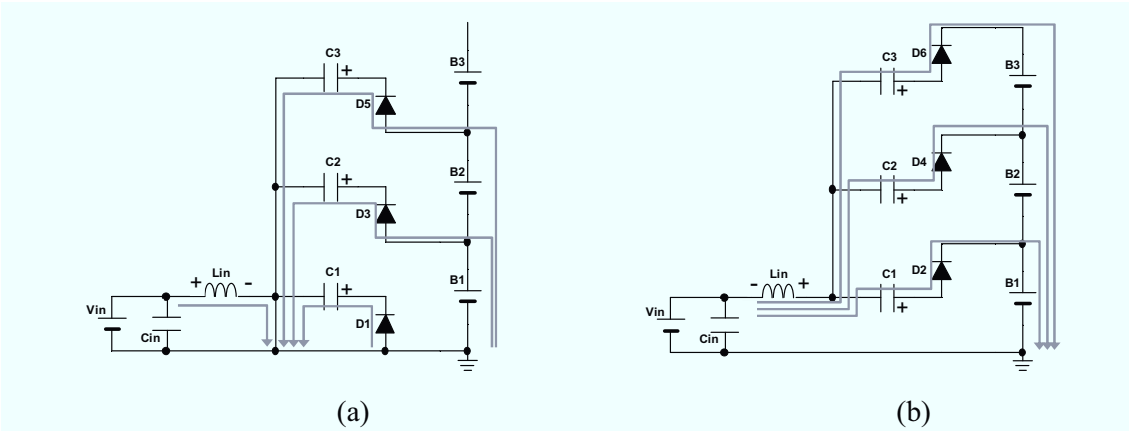
$$\begin{cases} V_{C1A} = -V_{D1} \\ V_{C2A} = V_{B1} - V_{D3} \\ V_{C3A} = V_{B1} + V_{B2} - V_{D5} \end{cases}, \tag{6.24}$$

where V_{Di} is the forward voltage drop of diode D_i (i = 1…6).

During the off period, the inductor current is distributed to C_1–C_3, and the modules B_1–B_3 are charged as shown in Fig. 6.5.2(b). The voltage across Q during the off period, V_Q, is determined by

$$V_Q = \frac{1}{1-d} V_{in}, \tag{6.25}$$

where d is the duty cycle of the switch; this equation is identical to the voltage conversion ratio of traditional boost converters. The voltages of C_1–C_3 at the end of the off period V_{C1B}–V_{C3B} can be expressed as



(a) (b)

Fig. 6.5.2. Current flow directions of the proposed single-switch single-inductor equalization charge.

$$\begin{cases} V_{C1B} = V_{B1} + V_{D2} - V_Q \\ V_{C2B} = V_{B1} + V_{B2} + V_{D4} - V_Q \\ V_{C3B} = V_{B1} + V_{B2} + V_{B3} + V_{D6} - V_Q \end{cases} . \tag{6.26}$$

Assuming V_{D1}–$V_{D6} = V_D$, by subtracting (6.26) from (6.24), the voltage variations ΔV_{C1}–ΔV_{C3} of C_1–C_3 in a single switching cycle are given by

$$\begin{cases} \Delta V_{C1} = \left(V_Q - 2V_D\right) - V_{B1} \\ \Delta V_{C2} = \left(V_Q - 2V_D\right) - V_{B2} \\ \Delta V_{C3} = \left(V_Q - 2V_D\right) - V_{B3} \end{cases} . \tag{6.27}$$

Since an average amount of charge delivered via a capacitor is $Q = C \times \Delta V = I \times t$, (6.27) can be rewritten as

$$\begin{cases} I_{C1} = C_1 f \left\{\left(V_Q - 2V_D\right) - V_{B1}\right\} \\ I_{C2} = C_2 f \left\{\left(V_Q - 2V_D\right) - V_{B2}\right\} \\ I_{C3} = C_3 f \left\{\left(V_Q - 2V_D\right) - V_{B3}\right\} \end{cases}, \tag{6.28}$$

where I_{C1}–I_{C3} and C_1–C_3 are the average currents and capacitances of C_1–C_3, respectively, and f is the switching frequency.

The product of capacitance and frequency (Cf) has a unit of conductance. Substituting equivalent resistances, R_1–R_3, for the inverses C_1f–C_3f in (6.28) yield

$$\begin{cases} V_Q - V_{B1} = I_{C1} R_1 + 2V_D \\ V_Q - V_{B2} = I_{C2} R_2 + 2V_D \\ V_Q - V_{B3} = I_{C3} R_3 + 2V_D \end{cases} . \tag{6.29}$$

$I_{Ci}R_i$ is the voltage drop at R_i, and $2V_D$ denotes the forward voltage drops across two diodes. Hence, an equivalent circuit of the proposed equalization charger can be derived from Ohm's Law, as shown in Fig. 6.5.3.

The modules B_1–B_3 are connected to a dc voltage source, V_Q, via two diodes and one equivalent resistor. The voltage across V_Q is given by (6.25) and is duty controllable. Based on the equivalent circuit, the charge currents for B_1–B_3 are found to be equal to I_{C1}–I_{C3}. The

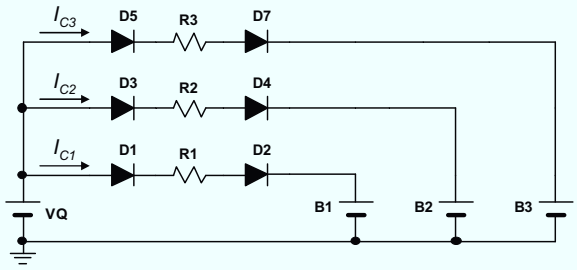


Fig. 6.5.3. Equivalent circuit of the proposed equalization charger for three-series-connected energy storage modules.

equivalent circuit indicates that identical charge currents flow to each module as long as the module voltages and equivalent resistances are uniform. For a voltage-imbalance condition, the modules with a voltage lower than $V_Q - 2V_D$ can be preferentially charged, and then all module voltages finally converge to the uniform voltage level of $V_Q - 2V_D$.

6.5.3 Constant Input Current–Constant Voltage Charging Scheme

Constant current–constant voltage (CC–CV) charging is the most common charging scheme for energy storage modules such as lithium-ion batteries and SC modules. Both the voltage and current of the module are measured to be controlled. In the proposed equalization charger, since all the module voltages theoretically become equal as long as V_{Di} is uniform as indicated by (6.29), it is sufficient to measure one of the module voltages for implementing CV charging.

For CC charging, on the other hand, all the module currents need to be measured to control the charge currents for each module. In case $V_{B1} < V_{B2} = V_{B3}$, for example, measuring I_{B2} and/or I_{B3} (i.e., not measuring I_{B1}) could lead to an extremely large charge current for B_1. To implement CC charging with the proposed equalization charger, three current measurement circuits are required, while conventional chargers need only one such circuit. Measuring all the currents is deemed to neutralize the major advantage of the proposed equalization method, namely, circuit simplicity.

Controlling an input current instead of the module currents is an alternative way. By controlling the input current, the equalization charger operates with a constant input current (CIC) charging scheme. With CIC charging at a known input voltage and a known operating range of module voltages, the module currents can be maintained below a desired level. In case of constant voltage V_{in}, CIC charging is equivalent to constant power (CP) charging. The number of current measurement circuits required for CIC charging is, of course, one.

With CIC charging at a constant input voltage (i.e., CP charging), relatively large currents flow to modules at the beginning of the charging process, and the currents gradually decrease as the module voltages increase. The input current should be determined such that the module currents never exceed the rated current of the modules.

6.5.4 Experiment

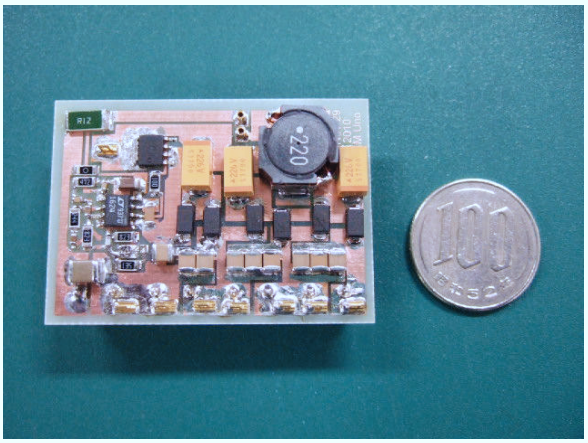


Fig. 6.5.4. Photograph of a 10-W prototype of the proposed equalization charger for three-series-connected energy storage modules.

Fig. 6.5.4 shows a photograph of a 10-W prototype of the proposed equalization charger designed for three-series-connected energy storage modules. The equalization charger was designed for V_{in} of 6.0 V and V_{Bi} of 7.0–15 V. An inductor of 22 μH, tantalum capacitors of 22 μF, Schottky diodes, and a MOSFET (HAT2266H, R_{on} = 9.2 mΩ, V_{DS} = 60 V) were used. A switching regulator controller IC (LTC1624) operating at 200 kHz was used to control I_{in} and V_{B1} to be 2.0 A and 14.5 V, respectively, for a CIC–CV charging scheme. Charging with CIC was equivalent to that with CP because of a constant input voltage of 6.0 V in the experiment.

Fig. 6.5.5 shows the experimental power conversion efficiency performance and output current of the 10-W prototype as a function of the total output voltage (i.e., a sum of V_{B1}–V_{B3}) when V_{B1}–V_{B3} were uniform. Since the prototype operated with CP, the output current decreased as the total output voltage increased. The efficiency increased with decreasing the output current. The average power conversion efficiency was measured to be approximately 88%.

EDLC modules with a capacitance of 220 F, shown in Fig. 6.4.8, were used as energy storage modules for the experiment. The three-series-connected EDLC modules with initial voltages of 7.0, 9.0, and 11.0 V, respectively, were charged by the prototype. Fig. 6.5.6 shows the resultant charge profiles of the module currents, standard deviation, and module voltages. The currents

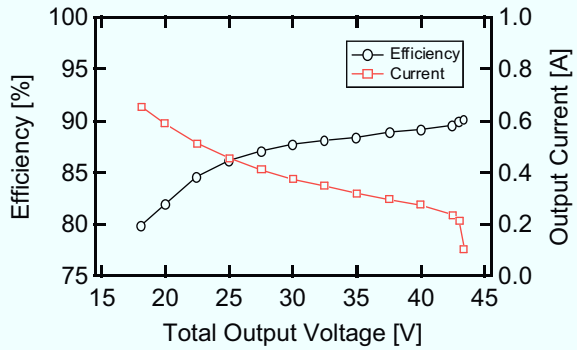


Fig. 6.5.5. Experimental efficiency performance and output current as a function of total output voltage (sum of V_1–V_3) when V_1–V_3 are uniform.

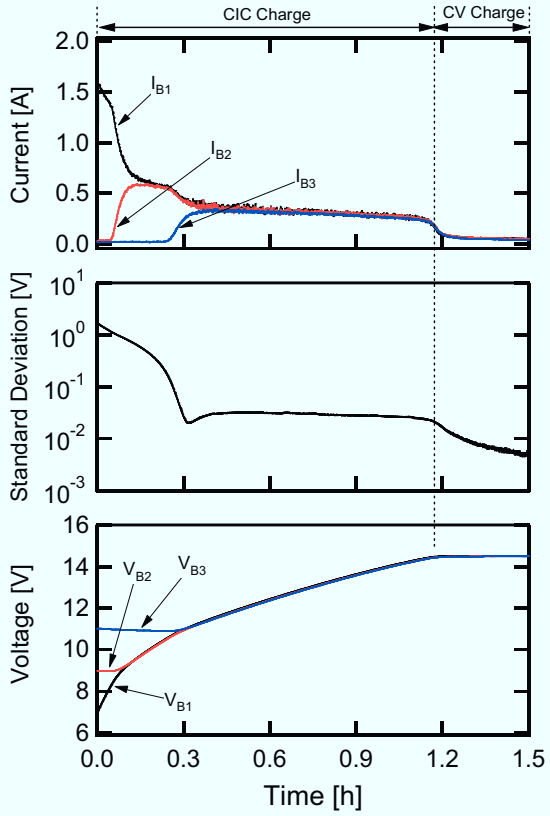


Fig. 6.5.6. Experimental charge profiles of series-connected EDLCs charged from an initially voltage-imbalanced condition.

were measured by current probes (KEYENCE, OP-72983).

The module(s) with the lowest voltage was (were) preferentially charged at each moment. At the beginning of the charge test, for example, only the current for B_1 flowed while the others did not. After V_{B1} overtook V_{B2}, the current for B_2 started to flow and V_{B2} began to increase. Finally, uniform charge currents flowed to each module after all module voltages become uniform.

Since the modules were charged with CP charging (i.e., CIC charging with a constant input voltage), the increase rates of the module voltage decreased as the module voltages increased. Finally, all the modules were charged to a uniform voltage level of 14.5 V.

The standard deviation decreased rapidly until all the module voltages become uniform during the CIC charging period. After the charging mode shifted from CIC to CV, all the module currents began to taper, and the standard deviation decreased further. The standard deviation at the end of the charge test was approximately 5 mV.

6.5.5 Conclusions

A single-switch single-inductor equalization charger using a voltage multiplier was proposed for series-connected energy storage modules in this chapter. The single-switch single-inductor operation can dramatically reduce the circuit size, complexity, and numbers of circuit components compared to conventional equalizers. The operating principle and derivation of an equivalent circuit for the proposed equalization charger were mathematically presented. A constant input current–constant voltage (CIC–CV) charging scheme—considered suitable for

the proposed equalization charger from the viewpoint of circuit and control simplicity—was also proposed and demonstrated experimentally.

Three EDLC modules connected in series, whose initial voltages were intentionally imbalanced, were charged by the prototype of the proposed equalization charger. The resultant charge profiles demonstrated that the modules can be charged preferentially in the order of increasing module voltage. The voltage imbalance was eliminated as the charging progressed, and all the modules were eventually charged to the desired uniform voltage level.

6.6 Comparison

Both the proposed equalization chargers can operate without a multi-winding transformer, and are considered advantageous over the conventional equalization chargers using a multi-winding transformer because of the lack of drawbacks originating from the existence of multi-winding transformer.

Although the equalization charger using multi-stacked buck-boost converters can operate with a CP charging scheme without feedback control when operated in DCM, multiple inductors are necessary. Therefore, it finds applications where required charge power is relatively low and an increase in size and mass of the charger due to multiple inductors is not a significant matter. On the other hand, the number of magnetic components can be dramatically reduced in the single-switch single-inductor equalization charger, although feedback control is necessary. This feature is considered suitable for SCs needing relatively large charge power. However, possible large inrush currents as well as consequent EMI are anticipated to cause unforeseen problems, as mentioned in Section 6.5.1.

6.7 Chapter Conclusions

Equalization chargers, which are chargers having equalization function, can simplify the entire power system configuration by integrating a charger and equalizers into one unit. The equalization charger is considered suitable for relatively small power systems, where reducing the number of power system components provides great benefit from the viewpoint of system mass reduction. Based on a brief calculation, the integrated system, in which a charger and equalizers are integrated into one unit, would be advantageous for charger power requirement higher than around 300 W, while the separate system, which have a charger and equalizers separately, would outperform in terms of system mass.

Two novel single-switch equalization chargers, which can be derived from the single-switch cell voltage equalizers introduced in the previous chapter, were proposed in this chapter. In comparison with the conventional equalization chargers using a multi-winding transformer, the proposed topologies are considered advantageous by eliminating a number of drawbacks originating from the existence of a multi-winding transformer. The equalization charger based on multi-stacked buck-boost converters can charge series-connected SCs with a CP charging scheme, which is a suitable charging scheme for SCs as discussed in Chapter 4, without a feedback control loop. Meanwhile, the single-switch single-inductor equalization charger offers even simpler circuit configuration because of the less number of magnetic components. Based on the comparison made for the proposed single-switch equalization chargers, the equalization charger using multi-stacked buck-boost converters are considered to find applications having

relatively small charge power requirement. On the other hand, the single-switch single-inductor equalization charger is deemed suitable for relatively large charge power requirement, although a few anxieties, such as large inrush current and consequent EMI, remain.

References

[1] J. W. Kimball, B. T. Kuhn and P. T. Krein, "Increased performance of battery packs by active equalization," in *Proc. IEEE Vehicle Power Propulsion Conference*, pp. 323–327, Sep. 2007.

[2] S. West and P. T. Krein, "Equalization of valve-regulated lead-acid batteries: issues and life test results," in *Proc. International Telecommunications Energy Conference*, pp. 439–446, Sep. 2000.

[3] N. H. Kutkut, D. M. Divan and D. W. Novotny, "Charge equalization for series connected battery strings," *IEEE Transactions on Industry Applications*, vol. 31, no. 3, pp. 562–568, May/Jun. 1995.

[4] N. H. Kutkut, H. L. N. Wiegman, D. M. Divan and D. W. Novotny, "Design considerations for charge equalization of an electric vehicle battery system," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 28–35, Jan. 1999.

[5] D. S. L. Simonetti, J. Sebastián and J. Uceda, "The ciscontinuous conduction mode Sepic and Ćuk power factor preregulators: analysis and design," *IEEE Transactions on Industrial. Electronics*, vol. 44, no. 5, pp.630–637, Oct. 1997.

Chapter 7
Unregulated Interface Converter

7.1 Introduction

For SCs to be used as alternatives to traditional secondary batteries, their two major drawbacks should be considered while designing power conversion electronics. The first drawback is their low specific energies compared with those of secondary batteries, as discussed in Section 2.4. This implies that the stored energy of SCs is precious and should be delivered to loads with maximum possible efficiency. The another drawback is the large voltage variation during cycling, as shown in Fig. 2.4.2. Since the available energy of SCs is proportional to the square of its terminal voltage, the SCs should be operated over a wide voltage range to maximize the utilization of its stored energy. Meanwhile, the bus voltage variation range of an SC-based power system needs to be as narrow as that of LIB-based power systems. Therefore, considering the abovementioned drawbacks of SCs, power conversion electronics that can efficiently operate in a wide voltage range are required for SCs to be used as alternatives to conventional batteries.

As mentioned in Section 2.4.3, extending operational voltage range of traditional dc-dc converters using magnetic components usually has negative impacts on converters' performance in terms of size, mass, and power conversion efficiency. Power conversion efficiencies, especially for discharging, have a great impact on system mass, as discussed based on sensitivity analyses in Section 4.4.3. In spite of such negative aspects, the traditional dc-dc converters will be considered to be a baseline even for SCs because of their technical maturity and increasing performance. However, an even-higher power conversion efficiency at reduced size and mass can be realized with unregulated converters which are basically a dc-dc converter without voltage regulation.

Two types of magnetic-less unregulated interface converters (UICs) are proposed in this chapter. The UICs are essentially bidirectional converters designed focusing on maximizing power conversion efficiencies by leaving voltage regulations to charge/discharge regulators or load converters installed in spacecraft instruments. Although their voltage conversion ratios are unregulated, bus voltage variations can be maintained within a desired range. Hence, SCs with a UIC can be replaced with a conventional secondary battery.

7.2 Review of Conventional Techniques

Various types of dc–dc switching power converters using magnetic components, such as inductors and transformers, have been proposed for SCs in high-power applications [1]−[3]. For applications requiring wide operational voltage range, the traditional converters must be designed so that their duty cycle can vary widely to extend voltage conversion ratios. However, the size of magnetic components and power conversion loss in converters tend to increase with

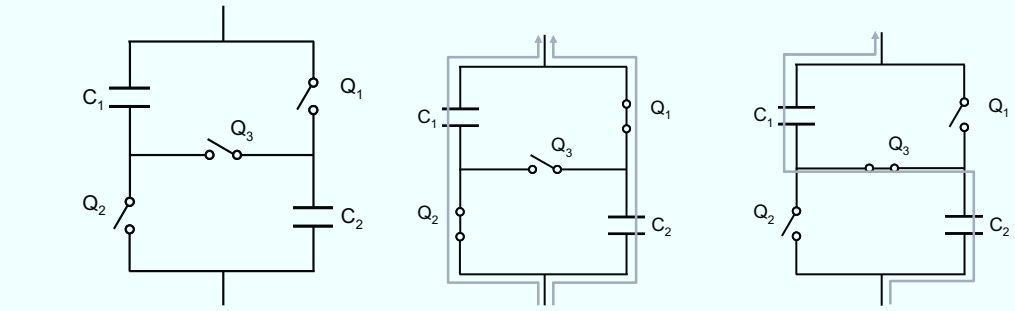


Fig. 7.2.1. Series–parallel changeover circuit. (a) Circuit description, (b) 1-series 2-parallel configuration, and (c) 2-series 1-parallel configuration.

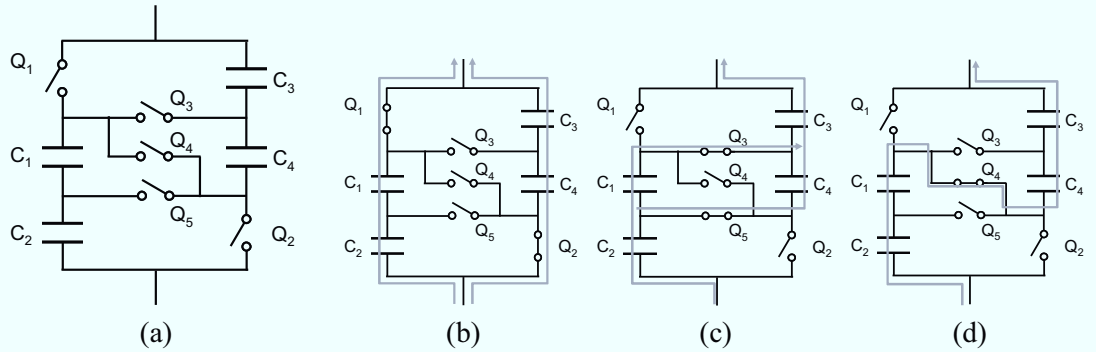


Fig. 7.2.2. Series–parallel changeover circuit. (a) Circuit description, (b) 2-series 2-parallel configuration, (c) 3-series 1- or 2-parallel configuration, and (d) 4-series 1-prallel configuration.

expanding the duty cycle, resulting in increased mass of not only power converters but also SCs and PV arrays, as discussed in Section 4.4.3 where the impact of power conversion efficiencies of charge/discharge regulators on power system mass was analyzed.

On the other hand, series–parallel changeover circuits that limit output voltage variation using only switches to recombine SCs have been proposed for energy storage applications [4]. These circuits do not require magnetic components and are more efficient than conventional dc–dc converters. Fig. 7.2.1(a) shows a series–parallel changeover circuit. Two SCs are initially connected in parallel via Q_1 and Q_2, as shown in Fig. 7.2.1(b). When the SC voltages fall to a particular value due to discharging, Q_3 turns on to shift the SC connection from parallel to series so that output terminal voltage can recover (Fig. 7.2.1(c)). However, reconfiguring the circuit from 1-series 2-paralle to 2-series 1-parallel causes a large voltage variation as high as 50%, which is not acceptable in most applications.

Fig. 7.2.2(a) shows a shift-type changeover circuit. It can operate with multiple stages so that terminal voltage variation can be significantly reduced. Initially, series connections C_1–C_2 and C_3–C_4 are connected in parallel via Q_1 and Q_2, as shown in Fig. 7.2.2(b). When the SC voltages fall to a particular value due to discharging, Q_3 and Q_5 turn on and Q_1 and Q_2 turn off at that time (Fig. 7.2.2(c)). At that moment, series connections C_1–C_2 and C_3–C_4 are partially

connected in parallel, i.e., C_1 and C_4 are connected in parallel and C_2 and C_3 shift to connect in series. After a further drop in SC voltage, Q_4 turns on to connect all SCs in series (Fig. 7.2.2(d)). This configuration can realize both reduced voltage variation and the deep depth of discharge, i.e., high energy utilization. However, the partial parallel connection period during which Q_3 and Q_5 are on (Fig. 7.2.2(c)), leads to unequal utilization of the SCs because currents flowing through C_2 and C_3 are two times larger than those through C_1 and C_4. In other words, this configuration inevitably causes voltage imbalance that leads to a short SC life and poor energy utilization.

7.3 Cascaded Switched Capacitor Converter with Selectable Intermediate Taps

7.3.1 Fundamentals

Switched capacitor converters (SCCs) that do not require bulky magnetic components such as transformers and inductors have been proposed and demonstrated for nonisolated intermediate bus converters [5]–[7], automotive applications [8], and cell voltage equalizers [9]–[11]. SCCs achieve high power conversion efficiency and power density. However, their voltage conversion ratio is not controllable and is determined by the number of capacitors stacked in series, unless inductive components are incorporated as resonant switched capacitor converters (RSSC) [12]. Hence, the use of SCCs has been limited to applications where voltage regulation is not necessary.

In this section, a UIC using cascaded SCCs with selectable intermediate taps is proposed. In the proposed interface converter, the desired multi-voltage levels are produced at high efficiency by the cascaded SCCs, and the voltage conversion ratio is roughly regulated by the selectable intermediate taps.

7.3.1.1 Circuit Description

Fig. 7.3.1 shows the generalized circuit description of the proposed UIC. It consists of two cascaded SCCs, SCC_1 and SCC_2, and selectable intermediate taps that are connected to SCC_2. Charge is delivered between SC and the load/charger via the cascaded SCCs and intermediate taps.

In the interface converter, each SCC acts as a voltage divider. The voltage of SC is divided into y levels at SCC_1, which consists of y stationary capacitors stacked in series and $(y - 1)$ energy transfer capacitors. Because the series connection of $C_{1a.1}$–$C_{1.x}$ in SCC_1 is connected to SCC_2, the divided voltage at SCC_1 is further divided into other z levels at SCC_2, which consists of z stationary capacitors stacked in series and $(z - 1)$ energy transfer capacitors. The selectable intermediate taps select one of z levels such that the voltage of the load/charger is maintained in a desired voltage range.

7.3.1.2 Operation Principle

In SCCs, odd- and even-numbered switches are alternately turned on and off with an appropriate dead-time period. Charge is delivered among capacitors at a high frequency so that the voltages across the capacitors in each SCC become almost uniform. The voltage difference among capacitors connected in parallel before the switches are turned off is almost zero, and therefore, the switches in each SCC are turned off at zero voltage, thus achieving zero-voltage

switching [5].

The voltage of SC, V_{SC}, is divided into y levels in SCC_1 and is expressed by

$$V_{SC} = yV_{C1}, \tag{7.1}$$

where V_{C1} represents the voltages of the capacitors in SCC_1. Because SCC_2 is cascaded to the series connection of $C_{1a.1}$–$C_{1a.x}$ in SCC_1, the voltages of the capacitors in SCC_2, V_{C2}, are given by

$$xV_{C1} = zV_{C2}. \tag{7.2}$$

In the proposed UIC, the voltage of the load/charger V_{SCC} is equal to the voltage level of the selected intermediate tap. For example, when S_{za}–S_{zb} are selected, V_{SCC} equals the sum of the voltages of $C_{1a.(x+1)}$–$C_{1a.y}$. On the other hand, turning on $S_{(z-1)a}$–$S_{(z-1)b}$ causes V_{SCC} to be equal to the sum of the voltages of $C_{1a.(x+1)}$–$C_{1a.y}$ and $C_{2a.z}$. The relationship between V_{SCC} and V_{SC} can be generalized using (7.1) and (7.2) as

$$V_{SCC} = (y-x)V_{C1} + (z-n)V_{C2} = V_{SC}\frac{yz-xn}{yz}, \tag{7.3}$$

where n is the subscript number of the selected intermediate tap. This equation suggests that V_{SCC} can represent the discrete voltage levels determined by the fixed values of x, y, and z, and

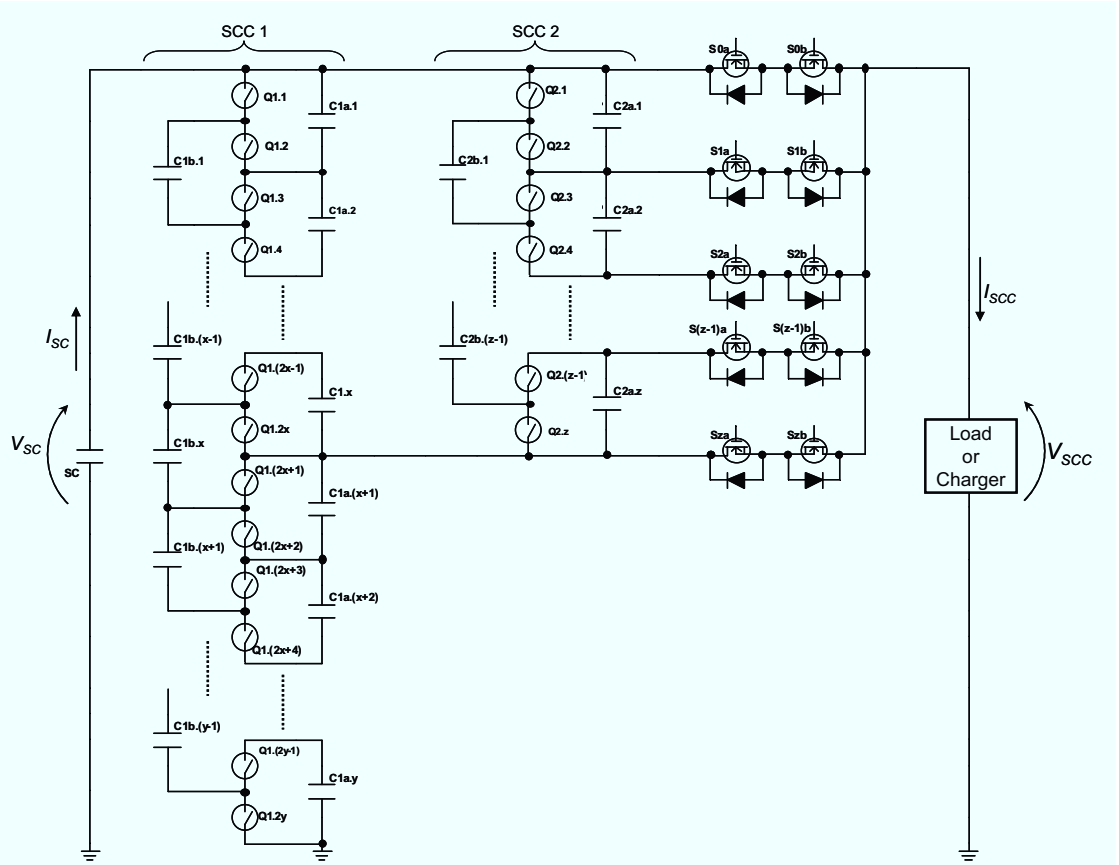


Fig. 7.3.1. General schematic of the circuit illustrating the proposed unregulated interface converter using cascaded SCCs with selectable intermediate taps for SCs.

the variables V_{SC} and n. Because V_{SCC} is always lower than V_{SC}, this UIC operates as a step-down and step-up unregulated converter during discharging and charging, respectively.

Assuming the ideal operation of the interface converter, i.e., without power conversion loss, the energy conservation law yields the following:

$$I_{SC} = I_{SCC} \frac{yz - xn}{yz}, \tag{7.4}$$

where I_{SC} and I_{SCC} are the currents of SC and the load/charger, respectively, as designated in Fig. 7.3.1. In the case where I_{SCC} is constant, I_{SC} changes stepwise as the selected tap changes. The discharging characteristics of an SC with the proposed interface converter are discussed in the following section.

7.3.1.3 Characteristics of SC with Unregulated Interface Converter

Fig. 7.3.2 shows the characteristics of an SC discharged at a constant current with the proposed UIC. At the beginning of discharging, the SC is fully charged at $V_{SC} = V_{cha}$ and discharges through S_{za}–S_{zb} (i.e., $n = z$). As discharging proceeds, both V_{SC} and V_{SCC} decrease. When it is detected that V_{SCC} is below the lower voltage limit of V_L, the selected intermediate tap is shifted to an upper tap, i.e., from S_{za}–S_{zb} to $S_{(z-1)a}$–$S_{(z-1)b}$. At that moment, V_{SCC} jumps to the next discrete voltage level, as expressed by (7.3). Because I_{SC} during the $S_{(z-1)a}$–$S_{(z-1)b}$-on period is larger than that during the S_{za}–S_{zb}-on period, as expressed by (7.4), the decrease rates of V_{SC} and V_{SCC} increase. V_{SC} and V_{SCC} decrease with further discharging. When V_{SCC} begins to decline to V_L again, the next intermediate tap $S_{(z-2)a}$–$S_{(z-2)b}$ is turned on to increase V_{SCC} to the next discrete level and I_{SC} increases again. The above sequence is repeated until the last tap S_{0a}–S_{0b} is selected. During the S_{0a}–S_{0b}-on period, the voltage and current of SC are equal to those of the load because the SC and the load are connected directly.

As the selected intermediate tap changes, I_{SC} increases incrementally. Thus, the stepwise

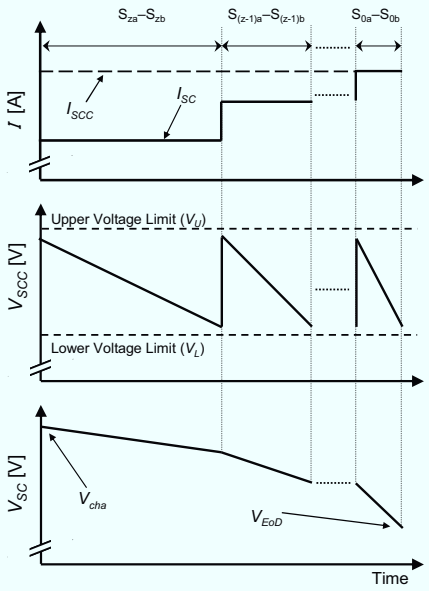


Fig. 7.3.2. Discharging characteristics of an SC with the proposed interface converter using cascaded SCCs with selectable intermediate taps.

increases in I_{SC} result in voltage inflection points in the discharge curve of V_{SC}. With the abovementioned sequence, the SC can be deeply discharged while maintaining V_{SCC} in a desired voltage range.

The energy utilization of the SC, λ, is given by

$$\lambda = \frac{U_{Initial} - U_{Residual}}{U_{Initial}}, \tag{7.5}$$

where $U_{Initial}$ and $U_{Residual}$ are the initial stored energy and residual energy at the end of discharging, respectively. $U_{Initial}$ and $U_{Residual}$ are given by

$$U_{Initial} = \frac{1}{2} C_{SC} V_{cha}^2, \tag{7.6}$$

$$U_{Residual} = \frac{1}{2} C_{SC} V_{EoD}^2, \tag{7.7}$$

where C_{SC} is the capacitance of the SC and V_{EoD} is the voltage at the end of discharging. These equations imply that high energy utilization can be achieved by deeply discharging SC to low voltages.

In this section, only the discharging sequence was discussed. The sequence for the tap changes during charging is the opposite of that during discharging.

7.3.1.4 Operation Range

The relationship among the upper and lower voltage limits V_U and V_L, and V_{SCC} are defined as

$$V_U \geq V_{SCC} \geq V_L. \tag{7.8}$$

From (7.3), the voltage variation in V_{SCC} caused by tap changes ΔV_{SCC} can be expressed as

$$\Delta V_{SCC} = V_{SC}^* \left\{ \frac{yz - x\left(n^* - 1\right)}{yz} - \frac{yz - xn^*}{yz} \right\} = V_{SC}^* \frac{x}{yz}, \tag{7.9}$$

where V^*_{SC} and n^* are the SC voltage and subscript number, respectively, of the selected tap immediately before the tap changes. Assuming that $V_{SCC} = V_L$ just before the tap changes, (7.3) yields

$$V_{SC}^* = V_L \frac{yz}{yz - xn^*}. \tag{7.10}$$

Equations (7.9) and (7.10) give

$$\Delta V_{SCC} = V_L \frac{x}{yz - xn^*}. \tag{7.11}$$

This equation suggests that ΔV_{SCC} can be arbitrarily designed using the appropriate values of x, y, and z so that (7.8) is satisfied:

$$V_U - V_L \geq V_L \frac{x}{yz - xn^*}. \tag{7.12}$$

At the beginning of discharging or the end of charging, V_{SC} is the highest because $V_{SC} = V_{cha}$. Equations (7.3) and (7.8) yield

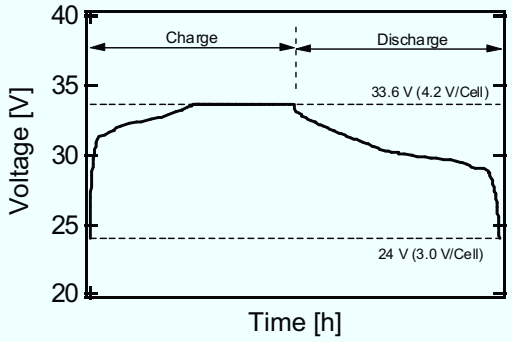


Fig. 7.3.3. Typical charge–discharge profile of a lithium-ion battery consisting of eight cells in series.

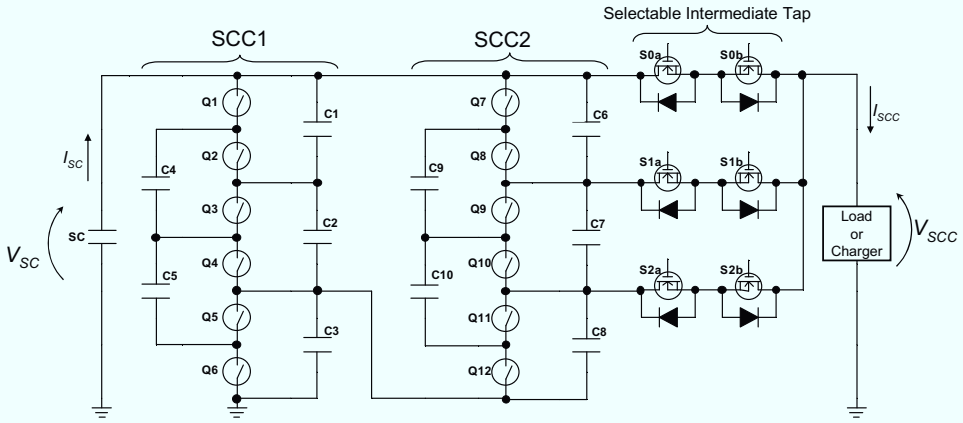


Fig. 7.3.4. Unregulated interface converter designed for an SC with V_{cha} = 60.0 V to satisfy V_U = 33.6 V and V_L = 24.0 V.

$$V_U \geq V_{cha} \frac{yz - xn}{yz}. \tag{7.13}$$

Similarly, the lowest SC voltage $V_{SC} = V_{EoD}$ is observed at the end of discharging or the beginning of charging and is given by

$$V_{EoD} \geq V_L. \tag{7.14}$$

Here after in this chapter, the example description of the proposed UIC for SC as an alternative to LIB consisting of eight cells connected in series, whose typical charge–discharge cycle profile is shown in Fig. 7.3.3, is dealt with. The typical voltage range of LIB cells is 3.0–4.2 V that corresponds to 24.0–33.6 V for an 8-cell battery pack. To satisfy V_U = 33.6 V and V_L = 24.0 V, the UIC was designed for SC with V_{cha} = 60.0 V. From (7.12) and (7.13), the number of capacitors stacked in series in the interface converter were determined as x = 2, y = 3, and z = 3. The circuit description of the designed UIC is shown in Fig. 7.3.4.

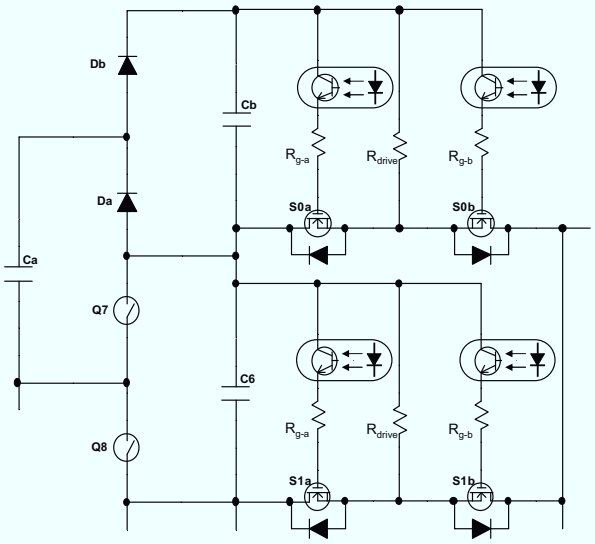
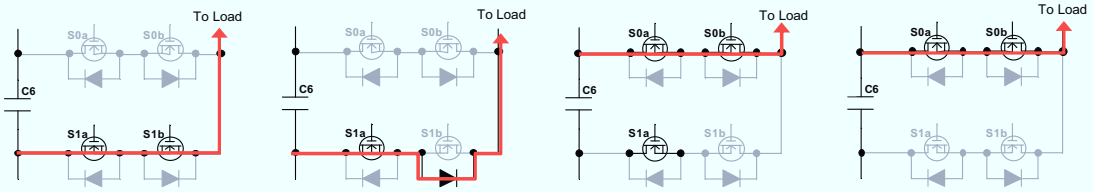


Fig. 7.3.5. Drive circuits for selectable intermediate taps.

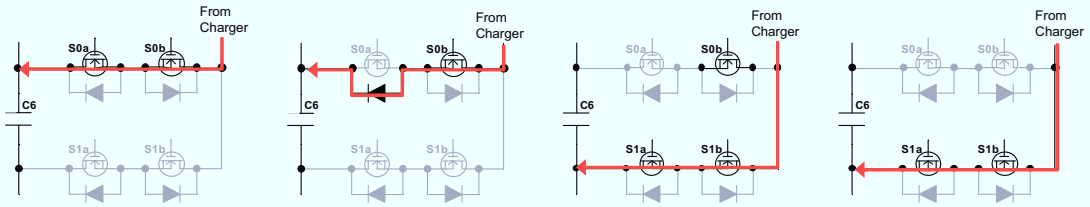
7.3.1.5 Selectable Intermediate Taps

The selectable intermediate taps and their drive circuits are shown in Fig. 7.3.5. In this section, the taps consisting of S_{0a}–S_{0b} and S_{1a}–S_{1b} are focused to explain their drive sequence. The voltage for driving gates of S_{1a}–S_{1b} is produced by C_6 and the resistor R_{drive}, and a bias current flows through R_{drive} and the body diode of S_{1a}. The opto-couplers that connect each MOSFET are turned on in order to select the desired intermediate tap. To produce a drive voltage for S_{0a}–S_{0b}, which is the tap placed at the highest voltage level, the capacitors C_a and C_b and the diodes D_a and D_b are included as shown in Fig. 7.3.5. While Q_8 is on, charge is delivered to C_a from C_6 via D_a. On the other hand, while Q_7 is on, the charge of C_a is transferred



(a) (b) (c) (d)

Fig. 7.3.6. Switching sequence of selectable intermediate taps for discharging.



(a) (b) (c) (d)

Fig. 7.3.7. Switching sequence of selectable intermediate taps for charging.

to C_b via D_b. The voltages of C_a and C_b are almost equal to that of C_6. S_{0a}–S_{0b} are driven by the voltages produced by C_b and R_{drive}.

The representative switching sequences of the selectable intermediate taps during discharging are described in Fig. 7.3.6, which focuses on the taps of S_{0a}–S_{0b} and S_{1a}–S_{1b}. To prevent a short-through current through C_6 during the transition period from the S_{1a}–S_{1b}-on period to the S_{0a}–S_{0b}-on period, the body diode of S_{1b} conducts as shown in Fig. 7.3.6(b) before turning on S_{0a}–S_{0b}.

Fig. 7.3.7 shows the representative switching sequence for charging. Similar to the discharging sequence illustrated in Fig. 7.3.6, the body diode of S_{0a} is utilized to prevent shorting of C_6 as shown in Fig. 7.3.7(b) before turning on S_{1a}–S_{1b}.

7.3.2 Analysis of Switched Capacitor Converter

The capacitors in SCCs deliver charges depending on their positions and load/charge currents. These capacitors need to be designed such that they can handle the generated RMS current that depends on the amount of charge delivered during operation. In this section, the amount of charge delivered by each capacitor is determined by a charge vector analysis [7],[13].

As a representative case, the charge that flows during S_{2a}–S_{2b} are on, are considered as shown in Fig. 7.3.8. In modes A and B, where odd- and even-numbered switches are turned on, respectively, the charges flowing through C_i are referred to as q_{iA} and q_{iB} (i = 1, … , 10). Kirchhoff's current law yields the following:

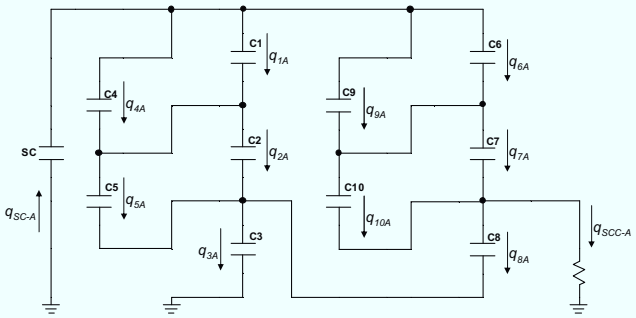
$$\begin{cases} 0 = -q_{1A} - q_{4A} - q_{6A} - q_{9A} + q_{SC-A} \\ 0 = q_{1A} - q_{2A} + q_{4A} - q_{5A} \\ 0 = q_{2A} - q_{3A} + q_{5A} + q_{8A} \\ 0 = q_{6A} - q_{7A} + q_{9A} - q_{10A} \\ 0 = q_{7A} - q_{8A} + q_{10A} - q_{SCC-A} \end{cases}, \tag{7.15}$$

$$\begin{cases} 0 = q_{1B} + q_{6B} + q_{SC-B} \\ 0 = -q_{1B} + q_{2B} + q_{4B} \\ 0 = -q_{2B} + q_{3B} - q_{4B} + q_{5B} - q_{8B} - q_{10B} \\ 0 = -q_{6B} + q_{7B} + q_{9B} \\ 0 = -q_{7B} + q_{8B} - q_{9B} + q_{10B} - q_{SCC-B} \end{cases}. \tag{7.16}$$

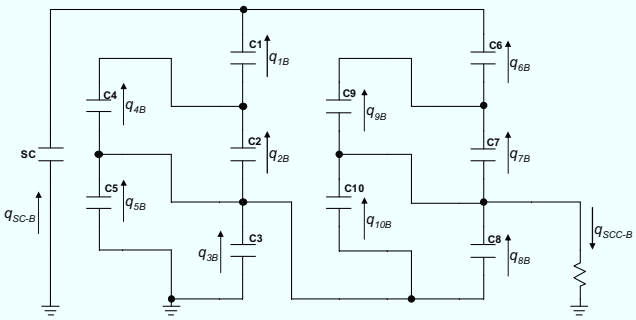
Under steady state conditions where the average voltages of the capacitors are constant for all switching cycles, the average currents of the capacitors must be zero. In other words, the charge delivered to and from the capacitors is balanced. Therefore, the direction of the charge flow in modes A and B are opposite and the charge amounts must be equal, as expressed by

$$q_{iA} = -q_{iB} = q_i . \tag{7.17}$$

By assuming that the SC is a constant voltage source, variation of the total voltage of C_1–C_3 can be considered zero because the series connection of C_1–C_3 is directly connected to the SC. Similarly, the total voltage of C_3 and C_8 can also be zero by assuming that the load voltage (i.e., V_{SCC}) is constant. These assumptions give



(a)



(b)

Fig. 7.3.8. Charge flow directions during (a) Mode A and (b) B.

$$\begin{cases} 0 = q_1 + q_2 + q_3 \\ 0 = q_3 + q_8 \end{cases}. \tag{7.18}$$

C_1–C_2 and C_6–C_8 are always connected in parallel so that variation of the total voltage of C_1–C_2 is equal to that of C_6–C_8, thus yielding

$$0 = q_1 + q_2 - q_6 - q_7 - q_8 . \tag{7.19}$$

The amount of charge delivered to the load in a single switching cycle is assumed to be 1, as expressed by

$$1 = q_{SCC-A} + q_{SCC-B} . \tag{7.20}$$

From (7.15)–(7.20), the relative charge flowing through each capacitor is determined as shown in Table 7.1 in which the relative charge amounts during the S_{0a}–S_{0b}-on and S_{1a}–S_{1b}-on periods are also shown. Because these values show the charge amount delivered in half a switching cycle, that delivered in a time period shorter than half a switching cycle is not reflected. This implies that even the capacitors whose charge amount is shown as zero in Table 7.1 may deliver some amount of charge in practical operations. Therefore, simulation analyses are also necessary to determine the RMS current rating for each capacitor.

As shown in Table 7.1, each capacitor delivers a different amount of charge depending on the selected intermediate tap. When S_{0a}–S_{0b} are on, the charge of C_1–C_{10} is zero because the charge

Table 7.1. Relative charge flowing through each capacitor determined by charge vector analysis.

	S_{2a}–S_{2b}	S_{1a}–S_{1b}	S_{0a}–S_{0b}
$q_{SC\text{-}A}$	23/30	3/4	1/2
$q_{SC\text{-}B}$	- 19/90	0	1/2
q_1	- 2/45	0	0
q_2	8/45	1/7	0
q_3	- 2/15	- 1/6	0
q_4	- 2/9	- 1/9	0
q_5	- 4/9	- 2/9	0
q_6	- 1/6	0	0
q_7	1/6	1/4	0
q_8	2/15	0	0
q_9	- 1/3	- 2/3	0
q_{10}	- 2/3	- 1/3	0
$q_{SCC\text{-}A}$	19/30	4/7	1/2
$q_{SCC\text{-}B}$	11/30	3/7	1/2

from the SC is directly transferred to the load without traveling through the capacitors in SCCs. Because the RMS current is strongly dependent on the amount of charge delivered, the capacitor design should factor the maximum charge amounts highlighted with gray in Table 7.1.

Each capacitor needs to be designed such that it is capable of handling the RMS current during practical operations. The current waveforms of capacitors in practical circuits exhibit transient responses that are dependent on resistive components such as the ESRs of capacitors, on-resistance of switches, and capacitance. For simplicity, we assume the current waveforms of capacitors to be square waveforms. The RMS current of C_i, $I_{i\text{-}RMS}$, is expressed by

$$I_{i-RMS} = \left| \frac{q_i f_S}{D} \right|, \tag{7.21}$$

where f_S is the switching frequency and D is the duty cycle. I_{SCC} is given by

$$I_{SCC} = \left(q_{SCC-A} + q_{SCC-B} \right) f_S . \tag{7.22}$$

Assuming $D = 0.5$, (7.20)–(7.22) yield

$$I_{SCC} : I_{i-RMS} = 1 : \left| 2q_i \right| . \tag{7.23}$$

This equation can roughly determine the RMS currents for each capacitor. However, as aforementioned, the resistive components that strongly influence the RMS current during practical operation are not considered in the above analysis, and therefore, simulation analyses are necessary to determine the RMS current rating for each capacitor. In the simulation analyses discussed in the following sections, the obtained relative charge amounts shown in Table 7.1 and the RMS current expressed by (7.23) are used as guidelines in the rough design of SCCs.

7.3.3 Simulation Analysis

In this section, the simulation analyses were performed by considering that multi-layer ceramic capacitors (MLCCs) are used for each capacitor, and the RMS current rating and the number of MLCCs required for each capacitor were determined. First, the required RMS current ratings and the number of MLCCs for each capacitor are preliminary determined by (7.23).

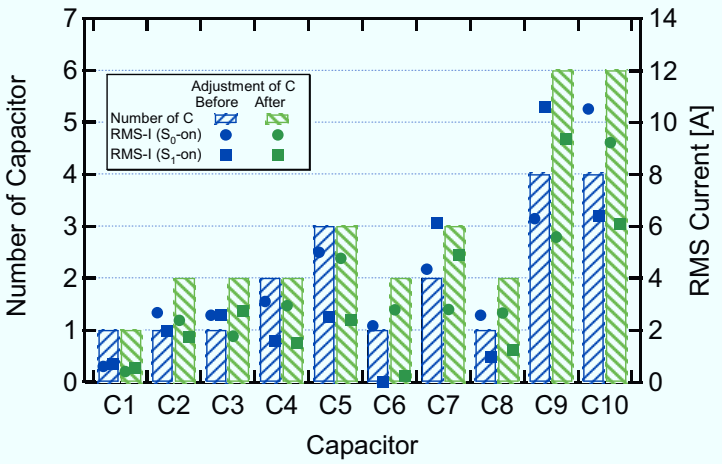


Fig. 7.3.9. The number of MLCCs and the RMS current of each capacitor before and after adjustment of the number of MLCCs.

Second, simulation analyses by considering the resistive components are performed to investigate RMS currents during practical operations. Finally, the number of MLCCs is adjusted so that the RMS current ratings of capacitors are satisfied with the minimum number of MLCCs.

Assuming that MLCCs with the capacitance of 22 μF, ESR of 4.0 mΩ, and RMS current rating of 2.0 A are used, the number of MLCCs used for C_1–C_{10} were approximated by (7.23). The on-resistances of Q_1–Q_6 and Q_7–Q_{12} were 9.2 and 1.8 mΩ, respectively, which are the same as those for the MOSFETs used in the experiments, as mentioned in the next section. The simulation analyses were performed for I_{SCC} = 4.5 A at an f_S of 300 kHz with D = 0.5.

The number of MLCCs used and the RMS current obtained by the simulation analyses are shown in Fig. 7.3.9. The markers enveloped by bars indicate that the RMS current rating is satisfied. The number of MLCCs determined by (7.23) (designated as "before adjustment" in Fig. 7.3.9) could not fulfill the RMS current ratings of C_2–C_3 and C_6–C_{10}. The number of MLCCs was increased so that each capacitor satisfies the RMS current ratings. After increasing the number of MLCCs (designated as "after adjustment" in Fig. 7.3.9), all markers were successfully enveloped by bars.

The design procedure explained in this section needs mathematical equations for rough calculations and simulation analyses for fine tuning the results. Simulation analyses alone, without using (7.23), can certainly determine the number of MLCCs required for each capacitor. However, because the RMS currents of the capacitors are mutually dependent, as seen in Table 7.1, it would require several iterations of simulation analyses before the number of MLCCs is determined. On the other hand, by using the combination of (7.23) and simulation analyses, the number of MLCCs can be efficiently determined, as demonstrated in this section.

7.3.4 Experiment

Fig. 7.3.10 shows the photograph of a 150 W prototype of the proposed UIC. The MOSFETs HAT2266H (V_{DS} = 60 V, R_{on} = 9.2 mΩ) and RJK0329DPB (V_{DS} = 30 V, R_{on} = 1.8 mΩ) for

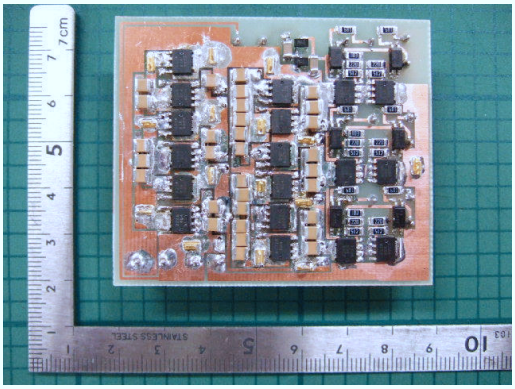
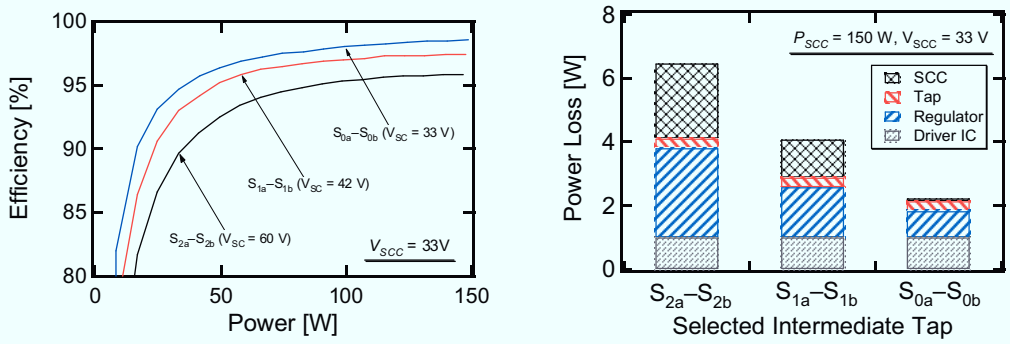


Fig. 7.3.10. Photograph of a 150 W prototype of the proposed unregulated interface converter.

Q_1–Q_6 and Q_7–Q_{12}, respectively, were driven by synchronous rectified MOSFET driver ICs (ISL6596) at a fixed switching frequency of 300 kHz with $D = 0.5$. Each driver IC was powered by each capacitor C_1–C_{10} via a linear regulator IC. The selectable intermediate taps also employed the MOSFETs HAT2266H.

Power conversion efficiencies were measured when V_{SCC} was approximately 33 V, as shown in Fig. 7.3.11(a). The measured efficiencies were higher than 95% above 100 W. The relatively poor efficiencies in low-power regions were due to power dissipation at the regulator ICs and the power consumption of the driver ICs operated at fixed frequencies. The variable switching frequency technique proposed in previous studies [5],[7] can be adopted to improve the light load efficiencies.

Breakdowns of the power conversion losses are shown in Fig. 7.3.11(b). The measured losses at the intermediate taps, which are determined by the Joule loss proportional to I_{SCC}, were the same in all three cases because I_{SCC} was equal to 4.5 A in all cases. On the other hand, the SCC loss was the smallest when S_{0a}–S_{0b} were selected. As shown in Table 7.1, the capacitors in each SCC did not deliver charge while S_{0a}–S_{0b} were on; thus the loss in SCCs was infinitesimal. In addition, the loss of the linear regulator ICs also decreased when S_{0a}–S_{0b} were on because this loss is proportional to the voltages of C_1–C_{10} determined by (7.1) and (7.2). On the other hand, because the regulated voltage was supplied to the driver ICs, the power consumption of the



(a) (b)

Fig. 7.3.11. (a) Experimental power conversion efficiencies and (b) power loss breakdown at $V_{SCC} = 33$ V and $P_{SCC} = 150$ W.

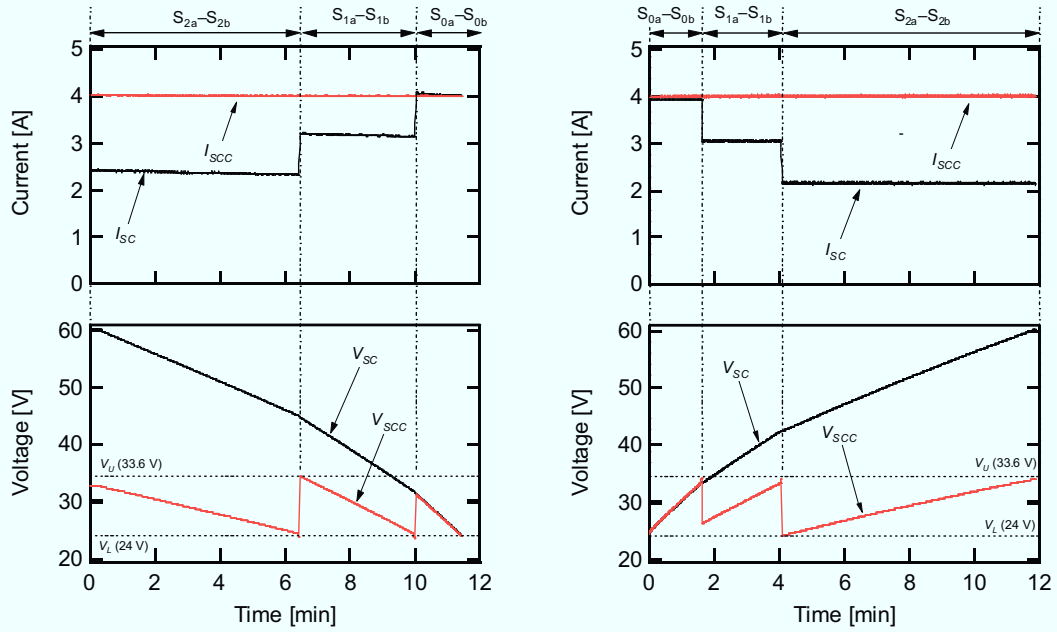


Fig. 7.3.12. Experimental (a) discharge and (b) charge curves of the EDLC module with the proposed unregulated interface converter.

driver ICs was independent of the selected tap.

An EDLC module with a capacitance of 55 F at a rated charge voltage of 60.0 V was discharged and charged at I_{SCC} = 4.0 A with the UIC. The selected intermediate taps were shifted when V_{SC} decreased below (exceeded) V_L = 24.0 V (V_U = 33.6 V) during discharging (charging). The resultant discharge and charge characteristics of the EDLC module are shown in Figs. 7.3.12(a) and (b), respectively. V_{SCC} was maintained between 24.0−33.6 V, which is comparable with the voltage variation range of a LIB consisting of eight cells connected in series as shown in Fig. 7.3.3. As explained in Section 7.3.1.2, I_{SC} changed stepwise and the curves of V_{SC} exhibited reflection points as the selected intermediate tap changed. The average power conversion efficiency during discharging was approximately 95%, and the energy utilization at V_{EoD} = 24.0 V was determined to be 84% by (7.5).

7.3.5 Conclusions

In this section, a UIC using cascaded SCCs with selectable intermediate taps was proposed for SCs to be used as alternatives to batteries. The proposed UIC achieves high efficiency using the cascaded SCCs, and its voltage conversion ratio is roughly regulated by the selectable intermediate taps. The operation principle and characteristics of SCs with the proposed UIC were mathematically explained.

A charge vector analysis was performed to quantify the amount of charge delivered through each capacitor in SCCs. The RMS current and the number of MLCCs required were determined by combining the results of the charge vector analysis and simulation analyses.

Based on the results of the analyses, a 150 W prototype of the proposed UIC was designed. Power conversion efficiencies higher than 95% were achieved above 100 W. An EDLC module

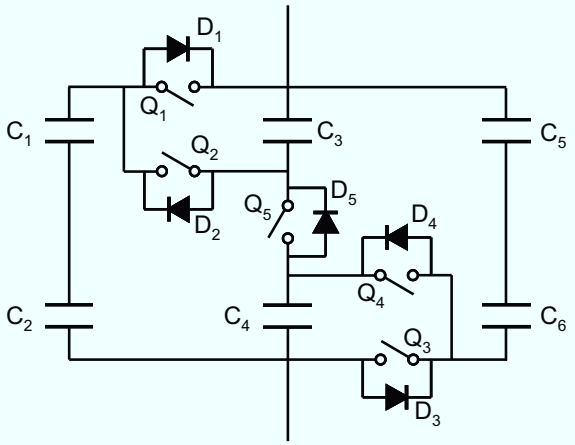


Fig. 7.4.1. Proposed SC reconfiguration circuit.

with a rated charge voltage of 60.0 V was cycled in the voltage range of 24.0−60.0 V, and the voltage of the load/charger was maintained between 24.0−33.6 V, which is comparable with the voltage variation range of a LIB consisting of eight cells connected in series.

7.4 Series-Parallel Reconfiguration Technique

7.4.1 Fundamentals

7.4.1.1 Operation Principle

Fig. 7.4.1 shows the proposed SC reconfiguration circuit. The circuit consists of SCs C_1−C_6, switches Q_1−Q_5, and diodes D_1−D_5. It can be formed into 2- or 3-series configurations according to switching states.

Figs. 7.4.2 and 7.4.3 show switching modes and voltage curves during constant current discharging. Assume that all SCs have identical capacitances and are fully charged. Initially, in Mode 1, switches Q_1, Q_3, and Q_5 are on, and strings C_1−C_2, C_3−C_4, and C_5−C_6 form a 2-series 3-parallel configuration. Each string consists of two SCs in series and one switch so that discharge current is uniformly distributed to each string. Module and cell voltages decrease with discharging. When the module/cell voltage falls to a particular level, the switches are operated to reconfigure the circuit from a 2-series 3-parallel to a 3-series 2-parallel configuration. First, Q_1, Q_3, and Q_5 turn off to shift to Mode 2 in which current flows through diodes D_1, D_3, and D_5,

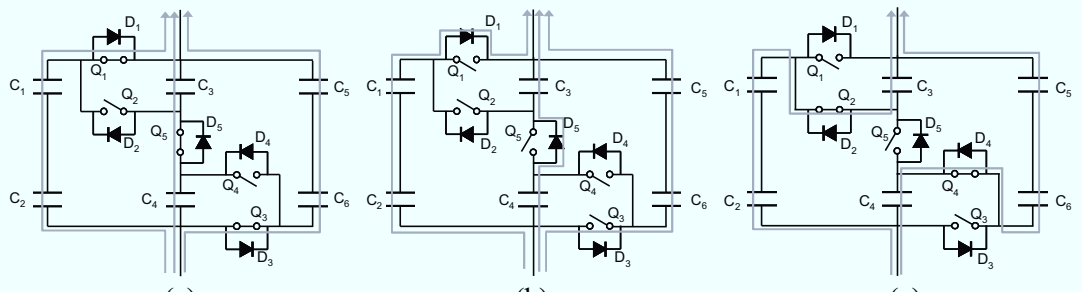


Fig. 7.4.2. Current flow directions during discharging in modes (a) 1, (b) 2, and (c) 3 of the proposed circuit.

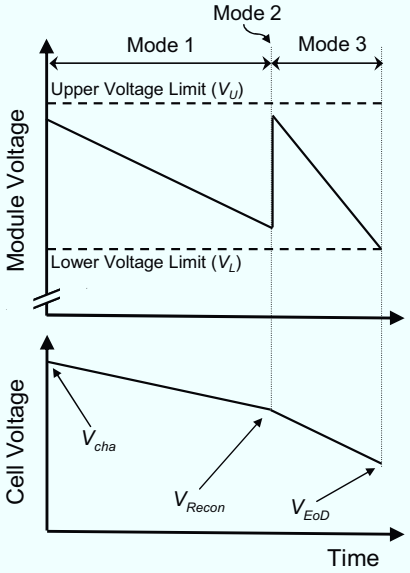


Fig. 7.4.3. Module and cell voltage curves during constant current discharging.

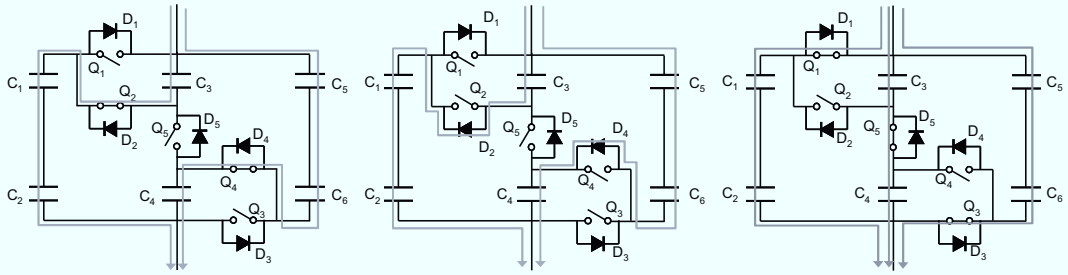


Fig. 7.4.4. Current flow directions during charging in modes (a) 4, (b) 5, and (c) 6 of the proposed circuit.

and the circuit is still in a 2-series 3-parallel configuration. Mode 2 corresponds to a dead time period to prevent short-through current. Switches Q_2 and Q_4 turn on to shift to Mode 3 in which strings C_1–C_3 and C_4–C_6 form a 3-series 2-parallel configuration and the module voltage becomes 1.5 times higher than at the end of Mode 1. Discharge current is uniformly distributed to each string. In this mode, however, half the discharge current flows through each string and therefore, inclinations of the module and cell voltages are steeper than those during Mode 1 in which only one-third of the discharge current flows through each string. The change in discharge current rate of each SC causes an inflection point in the cell voltage curve. This switching sequence does not produce cell voltage imbalance because the current is equally distributed to each SC for all periods.

Fig. 7.4.4 shows switching modes during charging. The principle is similar to that for discharging. In Mode 4, switches Q_2 and Q_4 are on, and strings C_1–C_3 and C_4–C_6 form a 3-series 2-parallel configuration. Module and cell voltages increase with charging. When the module voltage rises to a particular level, Q_2 and Q_4 turn off to shift to Mode 5. Diodes D_2 and D_4 now

conduct the charge current instead of switches. Switches Q_1, Q_3, and Q_5 turn on to shift to Mode 6 in which strings C_1−C_2, C_3−C_4, and C_5−C_6 form a 2-series 3-parallel configuration. Similar to the discharging process, the change in charge current rate of each SC causes an inflection point in the cell voltage curve.

The proposed technique achieves high efficiency because there are only conduction losses of switches. Besides, slow switching devices such as power relays can be used because the circuit is reconfigured only once per charge/discharge period, and hence fast switching is not required.

7.4.1.2 Operating Condition

Fig. 7.4.3 shows that module voltage varies with charging/discharging progress. The variation range should be designed to be smaller than the operating voltage range of loads. Upper and lower voltage limits V_U and V_L define the required voltage range determined by load. At the beginning of discharge, 2-series fully charged SCs with voltage V_{cha} should satisfy the condition,

$$V_U \geq 2V_{cha}. \tag{7.24}$$

Module and cell voltages decrease with discharging, and the module configuration shifts from 2-series 3-parallel to 3-series 2-parallel. The upper and lower voltage limits are as follows:

$$V_L \leq 2V_{Recon}, \tag{7.25}$$

$$V_U \geq 3V_{Recon}, \tag{7.26}$$

where V_{Recon} is the cell voltage at the moment of circuit reconfiguration. From (7.25) and (7.26), the relationship between V_U and V_L is

$$V_U \geq 3V_{Recon} \geq 1.5V_L. \tag{7.27}$$

Module voltage recovers from 2 V_{Recon} to 3 V_{Recon} so that the voltage variation ratio is 33% that is smaller than the value of 50% for a conventional series–parallel changeover circuit (Fig. 7.2.1) [6].

To utilize the energy stored in the SC as much as possible, the module should be discharged to V_L. Therefore,

$$V_L \leq 3V_{EoD}, \tag{7.28}$$

where V_{EoD} is the end of discharge voltage of SCs.

7.4.2 Experiment

An experimental SC module (Fig. 7.4.1) was tested. EDLCs with V_{cha} = 2.5 V and capacitance of 500 F were used. Power relays were employed for Q_1–Q_5 to facilitate a design of drive circuits. The EDLC module was charged using a constant-current–constant-voltage protocol and was discharged with a constant current of 1.0 A. Since V_{cha} = 2.5 V, V_U was defined to 5.0 V according to (7.24). In order to avoid oscillation, V_{Recon} was separately set to 1.635 V for discharging and 1.640 V for charging, which satisfies (7.27), as hysteresis thresholds. V_L was set to 3.2 V. Considering the slow response times of power relays, the dead

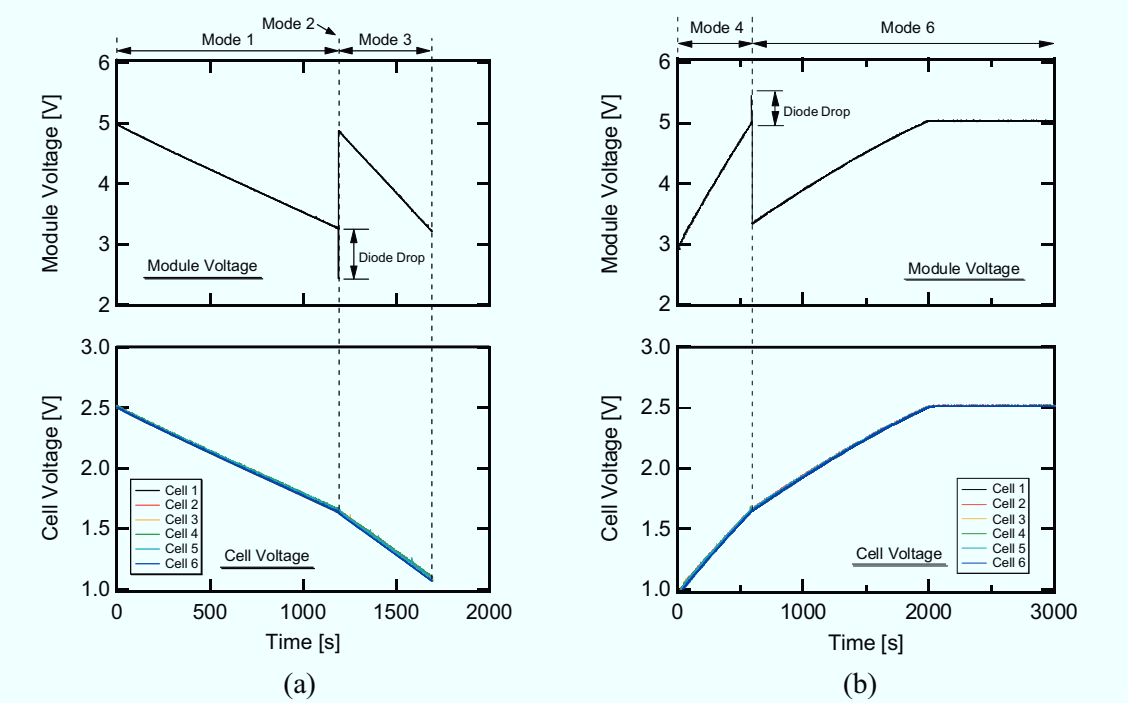


Fig. 7.4.5. Module and cell voltage curves during (a) discharging and (b) charging.

time periods of Modes 2 and 5 were set to 1.0 s. Each cell voltage was measured and averaged for V_{Recon}.

Fig. 7.4.5(a) shows experimental discharge curves for the module and cell voltages. The EDLCs were discharged to approximately 1.1 V, which corresponds to energy utilization ratio of 80.6%, at the end of discharge without voltage imbalance. At the moment of reconfiguration, during Mode 2, there was a voltage drop due to diode conduction. The drop can be negligible enough for higher voltage applications.

Fig. 7.4.5(b) shows experimental charge curves for the module and cell voltages. A diode drop was observed during Mode 5. All the EDLCs were charged from 1.1 to 2.5 V without voltage imbalance.

These experimental results demonstrated that the proposed reconfiguration technique can be used for both discharging and charging processes. The module voltage variation ratio, except for during dead time periods, was 36% (5.0–3.2 V), while that of the SCs was 56% (2.5–1.1 V). The proposed circuit achieved a much smaller voltage variation ratio than does a conventional series–parallel changeover circuit (50%) [4].

7.4.3 Combination of Proposed and Conventional Techniques

The proposed reconfiguration technique can be used with the conventional changeover circuits shown in Figs. 7.2.1 and 7.2.2. For example, an SC-based energy storage system combining the reconfigurable units shown in Fig. 7.4.1 with the changeover circuit shown in Fig. 7.2.1 is illustrated in Fig. 7.4.6. C_1 and C_2 in Fig. 7.2.1 are replaced with the unit shown in Fig. 7.4.1. The system consisting of 500 F EDLCs was discharged and charged at a constant current of 1.5 A, and the resultant discharge and charge curves are shown in Fig. 7.4.7. Table 7.2 shows

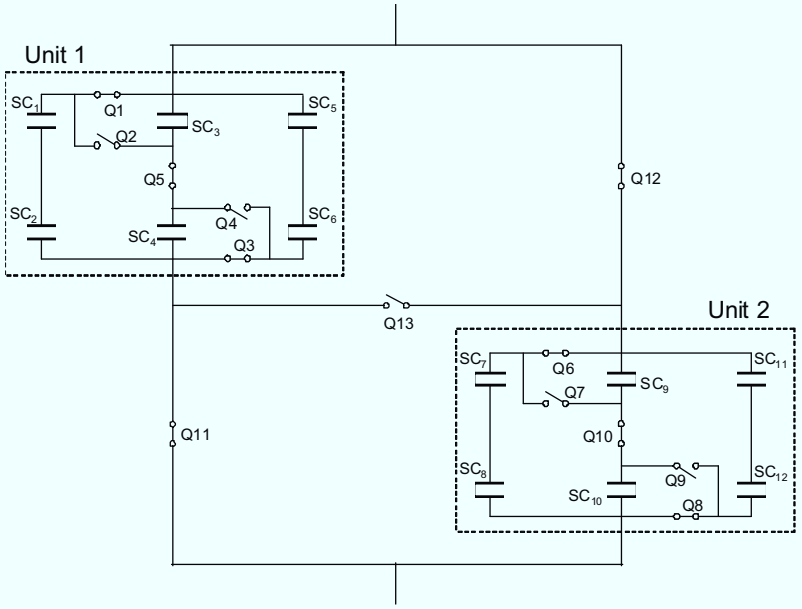


Fig. 7.4.6. Reconfigurable series-parallel SC energy storage system.

Table 7.2. Operating statuses of units and switches during discharging and charging, and system configuration in Modes A–D.

	Units 1 and 2	Q11, Q12	Q13	Configuration
Mode A	Mode 1 (4)	ON	OFF	two series six parallel
Mode B	Mode 3 (6)	ON	OFF	three series four parallel
Mode C	Mode 1 (4)	OFF	ON	four series three parallel
Mode D	Mode 3 (6)	OFF	ON	six series two parallel

the operating status of the units and switches and the system configuration during the discharging and charging experiment.

The system configuration was modified from Mode A to Mode D during discharging. When a system voltage lower than a predetermined lower voltage level (approximately 3.2 V in this case) was detected, the system configuration was modified by changing the operating statuses of the units and/or switches. As the discharging progressed, the number of series connections was increased consistently, whereas the number of parallel connections was decreased. The cell voltages decreased with discharging, but the system voltage was maintained within a desired voltage range. All the cells were uniformly and deeply discharged. The experimental results demonstrated that the system can achieve high energy utilization without causing voltage imbalance. During charging, in which the system was modified in reverse direction, all the cells were uniformly charged while the system voltage was kept within the desired range.

7.4.4 Conclusions

A series–parallel reconfiguration technique for SC energy storage systems was proposed in this section. This technique by which circuit configuration can be changed between 2-series

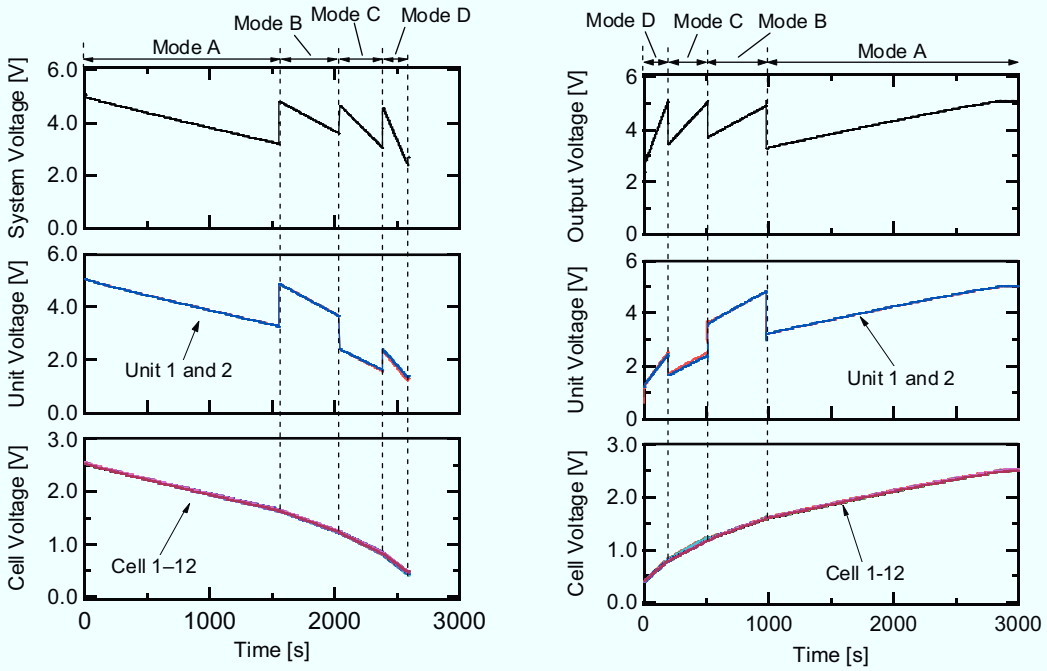


Fig. 7.4.7. System, module, and cell voltage curves during (a) discharging and (b) charging.

3-parallel and 3-series 2-parallel, realizes less variation in module voltage than does a conventional series–parallel changeover circuit.

The experimental EDLC module was cycled to verify its performance. The resulting discharge/charge curves showed almost as similar as theoretical characteristics. The experimental results demonstrated that the SCs can be discharged deeply, achieving a high energy utilization ratio (80.6% under experimental conditions). The voltage variation ratio of the proposed circuit (36%) was confirmed to be much smaller than that of a conventional series–parallel changeover circuit (50%).

7.5 Comparison

The UIC using cascaded SCCs is considered advantageous over other topologies including conventional and proposed reconfigurable UICs from the viewpoint of design flexibility because the voltage variation range of the UIC using cascaded SCCs can be arbitrary determined with the number of MLCCs stacked in series, as mathematically discussed in Section 7.3.1.4, whereas others' are determined with the number of SCs. However, the UIC using the cascaded SCCs requires numerous components, such as switches and MLCCs, compared with other UIC topologies and conventional dc-dc converters. The high component count may reduce the reliability. Multiple UICs can be used for redundancy when the reliability is a serious issue. Since the size and mass of this UIC can be small because of the lack of magnetic components, multiple use of the UICs may not have major negative impact on system mass, although cost increase due to multiple use is very likely.

On the other hand, the series-parallel reconfigurable UIC is considered less flexible in

designing the power system because at least three or two strings in parallel are necessary to configure. Although less flexible, the efficiency can be higher because of the lack of high-frequency switching operation. Considering these points, this UIC will find applications where multi-string SCs and high-efficiency power conversions are needed for large energy and power systems.

7.6 Chapter Conclusions

Since specific energies of SCs are low and SC voltage variation with cycling is large, high-efficiency power conversion electronics with wide operation voltage range are necessary in order to fully utilize stored energies of SCs. Extending operation voltage range of conventional dc-dc converters using magnetic components may cause negative influences on size, mass, and power conversion efficiencies.

In this chapter, two novel magnetic-less UICs were proposed for SC-based power systems. The UIC using cascaded SCCs with selectable intermediate taps, whose prototype demonstrated higher than 95% power conversion efficiency at 150 W, offers better design flexibility, but their high component count may pose a issue of reduced reliability. In addition, a few percent power conversion loss due to high-frequency switching operation is inevitable. Hence, it is more suitable in application having relatively low load power requirement rather than in that with high power requirement. On the other hand, the UIC based on the series-parallel reconfigurable technique requires at least three or two SC strings connected in parallel, and is considered less flexible. However, it can achieve even higher efficiency because of lack of high-frequency switching operation, and therefore, it will find applications where multiple strings are necessary for large energy and power systems.

References

[1] G. Guidi, T. M. Undeland and Y. Hori, "An Optimized Converter for Battery-Supercapacitor Interface," in *Proc. IEEE Power Electronic Specialist Conference,* , pp. 2976–2981, June 2007.

[2] B. J. Arnet and L. P. Haines, "High Power DC-to-DC Converter for Supercapacitors," in *Proc. IEEE Electric Machines and Drives Conference*, pp. 985–990, 2001.

[3] T. Mishima and E. Hiraki, "ZVS-SR Bidirectional DC-DC Converter for Supercapacitor-Applied Automotive Electric Energy Storage Systems," in *Proc.* IEEE *Vehicle Power and Propulsion,* pp. 2487–2493, 2005.

[4] S. Sugimoto, S. Ogawa, H. Katsukawa, H. Mizutani and M. Okamura, "A Study of Series-Parallel Changeover Circuit of a Capacitor Bank for an Energy Storage System Utilizing Electric Double Layer Capacitors," *EEJ,* Vol.145, No.3, pp.33–42, Nov. 2003.

[5] M. Xu, J. Sun, and F. C. Lee, "Voltage Divider and its Application in the Two-Stage Power Architecture," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, pp. 499–505, 2006.

[6] J. Sun, M. Xu, F. C. Lee and Y. Ying, "High Power Density Voltage Divider and its Application in Two-Stage Server VR," in *Proc. IEEE Power Electronics Specialist Conference*, pp. 628–635, 2007.

[7] B. Oraw and R. Ayyanar, “Load Adaptive, High Efficiency, Switched Capacitor Intermediate Bus Converter,” in Proc. IEEE Int. Telecommun. Energy Conf., INTELEC'07, pp. 1872–1877, 2007.

[8] F. Z. Peng, F. Zhang, and Z. Qian, “A Magnetic-Less DC-DC Converter for Dual-Voltage Automotive Systems,” *IEEE Transactions on Industry Applications*, Vol. 39, No. 2, pp. 511–518, 2003.

[9] C. Pascual and P. T. Krein, “Switched capacitor system for automatic series battery equalization,” in Proc. IEEE Applied Power Electron, Conf. Expo., APEC'97, pp. 848–854, 1997.

[10] A. Baughman and M. Ferdowsi, “Double-tiered switched-capacitor battery charge equalization technique,” *IEEE Transactions on Industry Applications*, Vol. 55, No. 6, pp. 2277–2285, 2008.

[11] M. Uno and K. Tanaka, “Influence of High-Frequency Charge-Discharge Cycling Induced by Cell Voltage Equalizers on Life Performance of Lithium-Ion Cells,” *IEEE Transactions on Vehicular Technology*, Vol. 60, No. 4, pp. 1505–1515, 2011.

[12] K. Sano and H. Fujita, “Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters,” *IEEE Transactions on Industry Applications*, Vol. 44, No. 6, pp. 1768–1776, 2008.

[13] M. D. Seeman and S. R. Sanders, “Analysis and Optimization of Switched-Capacitor DC-DC Converters,” *IEEE Transactions on Power Electronics*, Vol. 23, No. 2, pp. 841–851, 2008.

Chapter 8
System Consideration and Experiment

8.1 Introduction

Spacecraft power systems are designed considering load power requirement and environmental conditions, especially sunlight and eclipse periods, which determine length of charging and discharging periods, respectively. In this chapter, an SC-based LEO spacecrafts power system for a 28-V bus with 50 W load power requirement is studied. Based on the bus voltage and load power requirement, a suitable power system architecture is selected, and a power conditioning system is designed using power system components proposed in Chapters 5, 6, and 7.

8.2 Power System Architecture

The load power requirement of 50 W is small and falls into small/micro spacecraft power systems. For power systems with low load power requirement, typically lower than a few kilowatt, sun-regulated or unregulated power systems are more suitable than fully-regulated systems. With the unregulated architecture shown in Fig. 2.5.3(b), in which charging for SCs is controlled by the bus voltage regulator, the power system configuration can be simplest. However, the UIC existing between the SC and bus voltage regulator poses possible instability and decreased accuracy of charging, which originate from the interaction between the UIC and bus voltage regulator, as discussed in Chapter 2.5.1.3. On the other hand, in the sun-regulated architecture without a discharge diode, shown in Fig. 2.5.2(c), the charge regulator is directly connected to the SC, eliminating the negative interactive influences. In this chapter, the sun-regulated bus architecture without a discharge diode, shown in Fig. 2.5.2(c), was chosen for the experiment.

8.3 Cell Voltage Equalizer and Charge Regulator

In order for the power system with 50 W load power requirement to be light-mass at reasonable cost, simplifying power system configuration by reducing the number of power system components is more effective than improving individual performance of components, such as cell voltage equalizer and charge/discharge regulators. Therefore, combining components, if possible, into one unit is considered suitable than having separate components, making an equalization charger, discussed in Chapter 6, an attractive choice.

Two equalization chargers were proposed, and the comparison was already made in Section 6.6, concluding the equalization charger using multi-stacked buck-boost converter is more suitable for small charge power requirement. The single-switch equalization charger using multi-stacked SEPICs, shown in Fig. 6.4.1(a), was used for the experiment in this chapter.

8.4 Discharge Regulator

In the sun-regulated bus architecture for SC-based power systems, the UIC is used as a

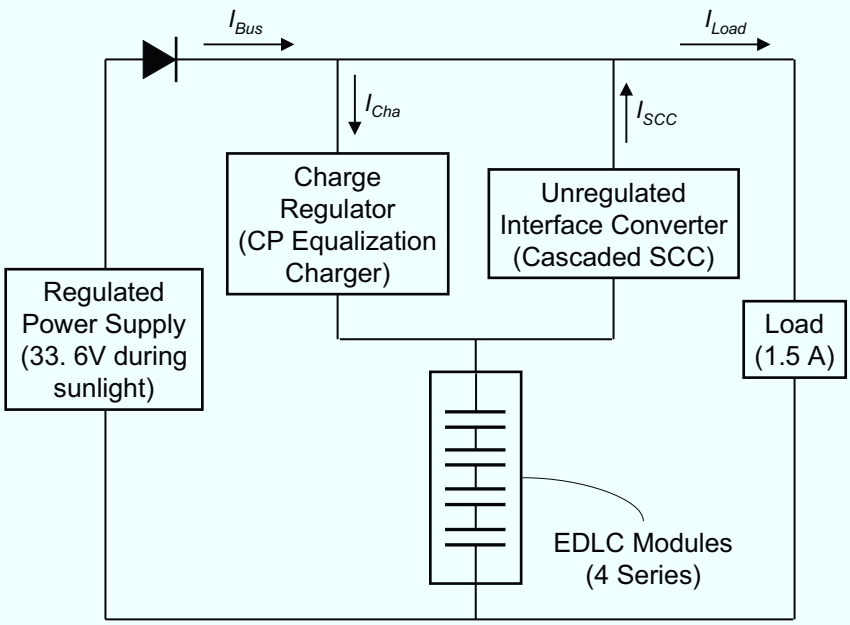


Fig. 8.5.1. System configuration for experimental SC-based sun-regulated 28-V bus system.

discharge regulator, as shown in Fig. 2.5.2(c). Two proposed magnetic-less UICs were compared in Section 7.5, in which suitable applications of the proposed UICs were discussed; the UIC using cascaded SCCs is considered to find applications having relatively low load power requirement, whereas the UIC based on the reconfigurable technique is suitable in high power applications. Since the load power requirement in this chapter is very low to be 50 W, the UIC using cascaded SCCs with selectable intermediate taps, shown in Fig. 7.3.4, was used for the system experiment.

8.5 System Experiment

8.5.1 Experimental Conditions

System configuration for the experimental sun-regulated 28-V bus system is shown in Fig. 8.5.1. Four EDLC modules with capacitance of 220 F at a rated charge voltage of 15.0 V, shown in Fig. 5.4.8, were used for the experiment instead of using individual EDLC cells for the sake of simplifying the experimental configuration, and were connected in series to form a 60-V 55-F EDLC unit. Each individual EDLC module has its own built-in shunting equalizers. Instead of the PV arrays with the bus voltage regulator, a regulated dc power supply with an output voltage of 33.6 V was used for the system experiment. The 25 W prototype of the SEPIC-based CP equalization charger tested in Chapter 6.4.3 was used for the experiment, and was operated at 70 kHz with fixed duty cycle of 0.15. The input current for the equalization charger, I_{Cha}, was constant to be approximately 0.69 A at input voltage of 33.6 V. The 150 W prototype of the UIC using cascaded SCCs, shown in Fig. 7.3.10, was used for the system experiment, and its intermediate taps were changed when the bus voltage falling below the lower voltage limit of V_L = 24.0 V during discharging was detected.

The regulated power supply was turned on and off to emulate sunlight-eclipse cycles. The load was a constant current load of 1.5 A. In order to demonstrate the system operation, the EDLC modules were cycled so that the bus voltage fully varies in the range of 24.0–33.6 V,

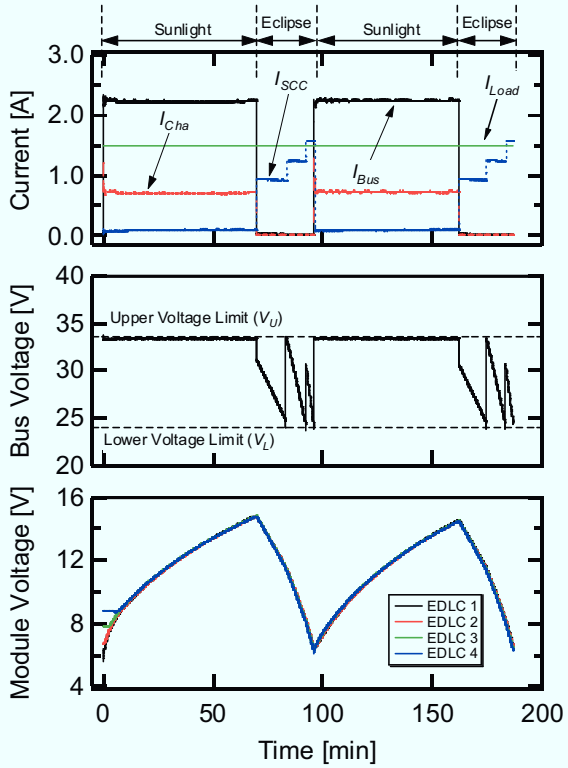


Fig. 8.5.2. Resultant sunlight-eclipse cycling profiles of the experimental SC-based sun-regulated 28-V bus system.

which is as same as the range of 8-sereies LIB cells as shown in Fig. 7.3.3, and the periods of sunlight and eclipse were not precisely controlled. For the sunlight periods, the dc power supply was turned on until the voltage of each EDLC module reaches approximately 14. 8V. On the other hand, the power supply was disabled during eclipse periods until the average EDLC voltage falls below 6.0 V. The equalization charger and UIC were disabled during eclipse and sunlight periods, respectively. The experimental sunlight-eclipse cycling was performed from an initially voltage-imbalanced condition.

8.5.2 Experimental Results

The resultant sunlight-eclipse cycling profiles are shown in Fig. 8.5.2. During sunlight periods, I_{Cha} was almost constant to be approximately 0.69 A, meaning that the equalization charger operated with the CP charging scheme, and the charge power was approximately 23.2 W. The voltage imbalance was eliminated as the EDLC voltages increased. When the average EDLC voltage reached approximately 14.8 V, the dc power supply was disabled to emulate eclipse period, and the UIC started to operate. The bus voltage decreased as the EDLCs discharged, and the intermediate taps of the UIC were shifted in turn when the bus voltage reaching 24.0 V was detected. The output current of the UIC, I_{SCC}, increased stepwise as the selected intermediate tap changed, as similar to the results shown in Fig. 7.3.12(a).

In the experimental SC-based sun-regulated 28-V bus system, the voltage imbalance of EDLC modules was eliminated during charging, and the bus voltage was maintained within 24.0–33.6 V for the entire periods, while the total voltage of EDLC modules varied between 24.0–59.2 V (6.0–14.8 V/module). The round-trip efficiency of the EDLC power system (the

bus to the EDLC and back to the bus) was approximately 79%, which was in a good agreement with the total efficiency of the equalization charger and the UIC (85% × 95% = 80.7%). The results demonstrated that the designed SC-based sun-regulated system can properly operate as a 28-V-bus spacecraft power system.

8.6 Conclusions

An SC-based power system was designed for a 28-V-bus power system with a load power requirement of 50 W in this chapter. Based on the system consideration, the sun-regulated bus architecture was selected, and the CP equalization charger using multi-stacked SEPICs and the UIC using cascaded SCCs, which were proposed in Chapter 6 and 7, respectively, were employed to build the experimental SC-based power system. Four 15-V EDLC modules were connected in series to form a 60-V EDLC unit. The experimental system test emulating sunlight-eclipse cycles was performed from the initially voltage-imbalanced condition. The voltage imbalance was eliminated during charging, and the bus voltage variation was maintained within 24.0–33.6 V, which is in a typical variation range of sun-regulated 28-V systems, while the total EDLC voltage swung between 24.0–59.2 V (6.0–14.8 V/module). The results demonstrated proper system operation of the designed SC-based sun-regulated 28-V-bus power system.

Chapter 9
Conclusions

SC technologies have a great potential of achieving longer service life over wider operation temperatures than do traditional LIBs in spacecraft power systems. The feasibility of SC technologies being an alternative energy storage source in spacecraft power system was studied, and power system components for SC-based power system were developed in this study. Expected major obstacles that originate from innate SC characteristics were posed and addressed. The raised obstacles include: (1) need of accelerated aging testing and/or life prediction model to properly design SC-based power systems, (2) possible mass increase due to low specific energies of SCs, thus needing a consideration for mass reduction at a power system level, (3) cell voltage imbalance originating from nonuniform individual cell properties of series-connected SCs, and (4) large voltage variation during cycling. Among a variety of SC technologies, two different types of SCs (EDLCs and LICs) were used to establish universal evaluation methods for feasibility study and to develop power system components universally applicable to other SC technologies.

The feasibility study was carried out based on experimental cycle life testing, establishment of ageing acceleration and life prediction model, and mass comparison between LIB- and LIC-based power systems.

In order to investigate the feasibility of aging acceleration and to establish a cycle life prediction model, the cycle life performance of EDLCs and LICs were evaluated emulating LEO cycling conditions. The resultant aging trends were linearly extrapolated with the square root of the number of cycles as the x-axis, and were mainly influenced by ambient temperature, suggesting that the aging can be accelerated by elevating the temperature. Ageing acceleration factors could be obtained from the activation energies determined by the Arrhenius equation. The cycle life prediction model was established combining the extrapolation and acceleration factor. The experimental and predicted aging trends were in good agreement, verifying that achievable cycle life of SCs at a given temperature is predictable.

The system mass comparison between LIB- and LIC-based LEO spacecraft power systems including PV arrays and power conditioning systems was made based on mathematical analysis. Although the specific energy of LIC is rather lower than that of LIB, the gap can be bridged to great extent by operating the LIC with deep DoD. In addition, the size and mass of PV arrays in the LIC-based system can be saved by introducing the CP charging scheme. The comparative analysis indicated the LIB-based systems would still be lighter for traditional cycle life requirement of 30000 cycles, whereas for even longer life requirement, LIC-based systems would be advantageous over LIB-based systems in terms of system mass and/or operation temperature range. The results imply that SCs, especially LICs, would be an alternative energy

storage source that achieves longer service life at extended operation temperature ranges than would have been achieved with LIBs at comparable power system mass.

Power system components for SCs were developed to address the issues of the cell voltage imbalance and large voltage variation during cycling.

Three novel cell voltage equalizers were proposed considering SC characteristics and general requirement in spacecrafts, such as reliability, design flexibility, and poor variety of rad-hard components. The proposed single-switch equalizers offer reduced circuit complexity, and good extendibility and design flexibility, compared with conventional equalizers. Two novel single-switch equalization chargers, which can simplify the power system configuration as a whole by integrating a charger and equalizers into one unit, were also proposed based on the single-switch cell voltage equalizers. Equalization performances of the proposed equalizers and equalization chargers were experimentally demonstrated using series-connected EDLCs.

As high-efficiency power conversion electronics operational over wide voltage range, two novel UICs, which are bidirectional dc-dc converters without voltage regulation, were proposed. Experimental charge-discharge tests were performed for EDLCs using the proposed UICs. The experimental results demonstrated that whereas EDLC voltage varied significantly, the UICs maintained the bus voltage variations within a desired range at high efficiencies.

An SC-based power system for a sun-regulated 28-V bus with 50 W load power requirement was considered and designed using the proposed power system components. The experimental power system using the singe-switch equalization charger and the UIC was built for a 60-V EDLC. The experimental test emulating sunlight-eclipse cycles was performed, and the system operation of the SC-based power system was verified.

Commercial EDLCs have been available for years, and their performance has been steadily increasing. Meanwhile, the commercialization of LICs has just began in recent years, and there would be likely to be rapid performance improvement. As SC performance increases and new SC technologies become available in the arena, the likelihood of SC technologies being considered to be alternatives to traditional secondary batteries would be further improved.

List of Papers

Peer-Reviewed Journal Papers

[1] M. Uno and K. Tanaka, "Accelerated Charge–Discharge Cycling Test and Cycle Life Prediction Model for Supercapacitors in Alternative Battery Applications," *IEEE Transactions on Industrial Electronics*, to be published.

[2] M. Uno and K. Tanaka, "Spacecraft Electrical Power System Using Lithium-Ion Capacitors," *IEEE Transactions on Aerospace and Electronic Systems*, to be published.

[3] M. Uno and K. Tanaka, "Single-Switch Cell Voltage Equalizer Using Multi-stacked Buck-Boost Converters Operating in Discontinuous Conduction Mode for Series-Connected Energy Storage Cells," *IEEE Transactions on Vehicular Technology*, Vol. 60, No. 8, pp. 3635–3645, Oct. 2011.

[4] M. Uno, K. Ogawa, Y. Takeda, Y. Sone, K. Tanaka, M. Mita and H. Saito "Development and on-orbit operation of lithium-ion pouch battery for small scientific satellite "REIMEI"," *Journal of Power Sources*, Vol. 196, No. 20, pp. 8755–8763, Oct. 2011.

[5] M. Uno and K. Tanaka, "Single-Switch Equalization Charger Using Multi-Stacked Buck-Boost Converters for Series-Connected Energy Storage Modules," *IEEJ Transactions on Industry Applications*, Vol. 131, No. 10, pp. 1203–1211, Oct. 2011. (in Japanese)

[6] M. Uno and K. Tanaka, "Discharger Using Cascaded Switched Capacitor Converters and Selectable intermediate Taps for Electric Double Layer Capacitors," *IEEJ Transactions on Industry Applications*, Vol. 131, No. 7, pp. 942–949, Jul. 2011. (in Japanese)

[7] M. Uno and K. Tanaka, "Active Device-Less Voltage Equalization Charger Using Capacitors, Diodes, and an AC Power Source," *IEEJ Transactions on Industry Applications*, Vol. 131, No. 5, pp. 739–746, May. 2011. (in Japanese)

[8] M. Uno, A. Kukita, and K. Tanaka, "Electric Double-Layer Capacitor Module with Series-Parallel reconfigurable Cell Voltage Equalizers," *IEEJ Transactions on Industry Applications*, Vol. 131, No. 5, pp. 729–738, May. 2011. (in Japanese)

[9] M. Uno and K. Tanaka, "Influence of High-Frequency Charge-Discharge Cycling Induced by Cell Voltage Equalizers on Life Performance of Lithium-Ion Cells," *IEEE Transactions on Vehicular Technology*, Vol. 60, No. 4, pp. 1505–1515, Mar. 2011.

[10] M. Uno, and K. Tanaka, "A Novel Voltage Equalization Charger using Capacitors, Diodes, and an AC Power Source for Energy Storage Cells," *IEEJ Transactions on Industry Applications*, Vol. 130, No. 10, pp. 1191–1192, Oct. 2010. (in Japanese)

[11] M. Uno, and K. Tanaka, "A Single-Switch Equalization Charger for Series-Connected Energy Storage Cells," *IEEJ Transactions on Industry Applications*, Vol. 130, No. 9, pp. 1119–1120, Sep. 2010. (in Japanese)

[12] M. Uno, and K. Tanaka, "Single-Switch Multi-Output Charger Using Voltage Multiplier for Series-Connected Lithium-Ion Batteries/Supercapacitor Equalization," *IEEE Transactions on Industrial Electronics*, submitted.

[13] M. Uno, and K. Tanaka, "Double-Switch Single-Transformer Cell Voltage Equalizer Using a Half-Bridge Inverter and Voltage Multiplier for Series-Connected Supercapacitors," *IEEE Transactions on Vehicular Technology*, submitted.

Peer-Reviewed International Conference Papers

[1] M. Uno and K. Tanaka, "Single-Switch Cell Voltage Equalizer Using Voltage Multipliers for Series-Connected Supercapacitors," *IEEE Applied Power Electronics Conference and Exposition*, Orland, USA, pp. 1266–1272, Feb. 2012.

[2] M. Uno and K. Tanaka, "Unregulated Interface Converter Based on Cascaded Switched Capacitor Converters for Supercapacitors in Alternative Battery Applications," *IEEE International Conference on Power Electronics and Drive Systems*, Singapore, pp. 579–586, Nov. 2011.

[3] M. Uno and K. Tanaka, "Single-Switch Constant-Power Equalization Charger Based on Multi-Stacked Buck-Boost Converters for Series-Connected Supercapacitors in Satellite Power Systems," *IEEE 33rd International Conference on Power Electronics and Drive Systems*, Singapore, pp. 1158–1165, Nov. 2011.

[4] M. Uno and K. Tanaka, "Accelerated Ageing Testing and Cycle Life Prediction of Supercapacitors for Alternative Battery Applications," *IEEE 33rd International Telecommunications Energy Conference*, Netherland, pp. 1–6, Oct. 2011.

[5] M. Uno and K. Tanaka, "Single-Switch Cell Voltage Equalizer Based on Multi-Stacked SEPICs for Series-Connected Energy Storage Cells," *IEEE International Telecommunications Energy Conference*, Netherland, pp. 1–7, Oct. 2011.

[6] M. Uno and K. Tanaka, "Single-Switch Equalization Charger Using Multi-Stacked Buck-Boost Converters for Series-Connected Energy Storage Cells," *IEEE 8th International Conference on Power Electronics–ECCE Asia*, Jeju, Korea, pp. 2990–2996, Jun. 2011.

[7] M. Uno and K. Tanaka, "Single-Switch Single-Inductor Equalization Charger Using a Voltage Multiplier for Series-Connected Energy Storage Modules," *IEEE 8th International Conference on Power Electronics–ECCE Asia*, Jeju, Korea, pp. 2985–22989, Jun. 2011.

[8] M. Uno and K. Tanaka, "Equalization Chargers Using Capacitor-Diode Networks for Series-Connected Energy Storage Cells," *IEEE The 9th International Power and Energy Conference*, Singapore, pp. 538–543, Oct. 2010.

[9] M. Uno, "Series–Parallel Reconfiguration Technique for Supercapacitor Energy Storage Systems," *IEEE TENCON*, Singapore, pp. 1–5, Nov. 2009.

[10] M. Uno, "Cascaded Switched Capacitor Converters with Selectable Intermediate Taps for Supercapacitor Discharger," *IEEE TENCON*, Singapore, pp. 1–5, Nov. 2009.

[11] M. Uno, "Interactive Charging Performance of a Series Connected Battery with Shunting Equalizers," *IEEE 31st International Telecommunications Energy Conference*, Incheon, Korea, pp. 1–5, Oct. 2009.

[12] M. Uno and A. Kukita, "Charge Equalizer Using a Cockcroft-Walton Voltage Multiplier for Series-Connected Supercapacitors," *IEEE 31st International Telecommunications Energy Conference*, Incheon, Korea, pp. 1–5, Oct. 2009.

Book (as a co-author)

[1] M. Uno, "Supercapacitor-Based Electrical Energy Storage System," in Chapter 2, Book Title: Energy Storage in the Emerging Era of Smart Grids, Edited by R. Carbone, INTECH Open Access Publisher, ISBN 978-953-307-269-2, pp. 21–40, Sep. 2011.

Patent

[1] M. Uno, "Series-Parallel Reconfigurable Capacitor Power Unit/System," Japan Patent 2009-265099, Nov. 20, 2009.

[2] M. Uno, "PWM-Controllable Equalization Charger for Series-Connected Energy Storage Cells," Japan Patent 2010-061137, Mar. 17, 2010.

[3] M. Uno, "Duty-Controllable Equalization Charger for Series-Connected Energy Storage Cells," Japan Patent 2010-061138, Mar. 17, 2010.

[4] M. Uno and A. Kukita, "Single-Switch Equalizer for Series-Connected Energy Storage Cells," Japan Patent 2011-046468, Mar. 3, 2011.