Development of Advanced Pixel Detectors for X-ray Astronomy with SOI Technology

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Abstract

X-ray astronomy is the one of the important research fields to understand the universe. The first X-ray detection in the universes other than the Sun was observed with the rocket by B.Rossi and R.Giacconi in 1962. X-ray astronomy has grown quickly since then.

As of 2013, three X-ray astronomical satellites, *Suzaku*, *X-ray Multi-Mirror Mission (XMM-Newton)*, and *Chandra*, are operated in the space. The standard imaging spectrometers of these modern X-ray astronomical satellites are X-ray Charge Coupled Device's (CCD). The X-ray CCD offers Fano limited X-ray spectroscopic performance with the readout noise of about 3 electrons. It allows us to do wide and fine imaging with the sensor size of 20 - 30 mm square and a pixel size of ~ 30 μm. However, it has some weakness. The most serious issue is a non-X-ray background (NXB) generated by high energy particles on orbit. Especially it has serious influence above 10 keV. The rate of the NXB is too high to study faint sources. Therefore, a low background detector is desired in the next generation. Moreover, time resolution is too poor to make fast timing study of time variable sources (e.g., millisecond pulsar).

Future X-ray astronomical satellite missions will require a new type of detectors that can distinguish X-rays and charged particle tracks, so as to reduce the background level. The new detector must have good coincidence time resolution (~ 1 μs), superior hit-position readout time (~ 10 μs) in order to reduce the NXB by cosmic rays. By introducing an anti-coincidence method between the hit signal and the external active shield detector, the background produced by the cosmic ray tracks can be greatly reduced. This is particularly important for the observation of hard X-rays with energies above 10 keV. In addition, it must have wide bandpass (from soft to hard X-rays, 0.3 – 40 keV), and comparable performance in terms of imaging spectroscopy.

In order to realize the detector described above, we have been developing a new type of active pixel sensor (APS) called XRPIX based on the semiconductor pixel detector with the

silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) technology. This new technology, i.e., SOI pixel detector (SOIPIX), has been developed by High Energy Accelerator Research Organization (KEK) in recent years. Thereby, we designed "Event-Driven SOIPIX" with a trigger information output function as "XRPIX series". And we realize the spectroscopy system which reduce background rate of the NXB by two orders of magnitude compared with the CCD. Finally, we aim to employ the XRPIX in the next generation X-ray astronomical satellite.

XRPIX series has designed six devices of XRPIX1/1b/2/2b/3/3b until now. In each chip, Event-Driven readout and spectroscopic performance are tested and improved. The XRPIX2b has a middle size of sensing area (effective area is 4.6 mm sq., pixel size is 30 μm sq., number of pixels is 20 k) and succeeded in acquisition of the spectrum by Event-Driven readout mode. We think this is a world first detector realized this function. The event rate tolerance is over 1 kHz.

In view point of the spectroscopic performance, XRPIX3 achieved best performance in the SOIPIX detectors. It includes a charge sensitive amplifier in each pixel for the first time in the XRPIX series. The gain of X-ray responsivity is 17.9 μV/e$-$. The readout noise is 33 electrons rms from the pedestal peak and the energy resolution is about 300 eV FWHM at 5.9 keV from ^{55}Fe radio isotope. Furthermore, XRPIX3 resolved $\mathrm{Mn} - \mathrm{K}_\alpha$ (5.9 keV) and $\mathrm{Mn} - \mathrm{K}_\beta$ (6.4 keV) successfully for the first time in our series. Thereby, XRPIX reached the spectroscopic performance accepted as an X-ray detector.

In this study, I have done many basic studies for the XRPIX by using device and circuit simulators. Then I have designed many prototype chips and measured performance of the chips with X-rays. In addition, I have done cooling test of the detector and analyzed the source of the leakage current etc. Through these work, I think I can demonstrate the possibility of the XRPIX for future X-ray astronomy satellite missions.

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Ayaki Takeda
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Chapter 1

Introduction

A celestial object exists in the universe countlessly and it is emitting various electromagnetic waves. However, some electromagnetic waves do not reach surface of the earth because they are scatted out or absorbed by the thick atmosphere. Therefore, it is necessary to launch observatories in orbit in order to observe photon (X-rays and γ-rays).

X-ray astronomy is the one of the important research fields to understand the universe. The first X-ray detection in the universes other than the Sun was observed with the rocket by B.Rossi and R.Giacconi in 1962. X-ray astronomy has grown quickly since then.

As of 2013, three X-ray astronomical satellites, *Suzaku*[1], *X-ray Multi-Mirror Mission (XMM-Newton)*[2], and *Chandra*[3], are operated in the space. The standard imaging spectrometers of these modern X-ray astronomical satellites are X-ray Charge Coupled Device's (CCD) [1]- [3]. The X-ray CCD offers Fano limited X-ray spectroscopic performance with the readout noise of about 3 electrons. It allows us to do wide and fine imaging with the sensor size of 20 - 30 mm square and a pixel size of ~ 30 μm. However, it has some weakness. The most serious issue is a non-X-ray background (NXB) generated by high energy particles on orbit. Figure 1.1 is the background level of various satellite missions normalized by the effective area and unit solid angle. This shows that the background is dominated by the cosmic X-ray background (CXB) level below 6 keV. On the other hand, NXB become dominating component of the background above 6 keV. Especially it has serious influence above 10 keV. The rate of the NXB is too high to study faint sources. Therefore, a low background detector is desired in the next generation. Moreover, time resolution is too poor to make fast timing study of time variable sources (e.g., millisecond pulsar).

[1]http://www.astro.isas.jaxa.jp/suzaku/index.html.en
[2]http://xmm.esac.esa.int/
[3]http://chandra.harvard.edu/

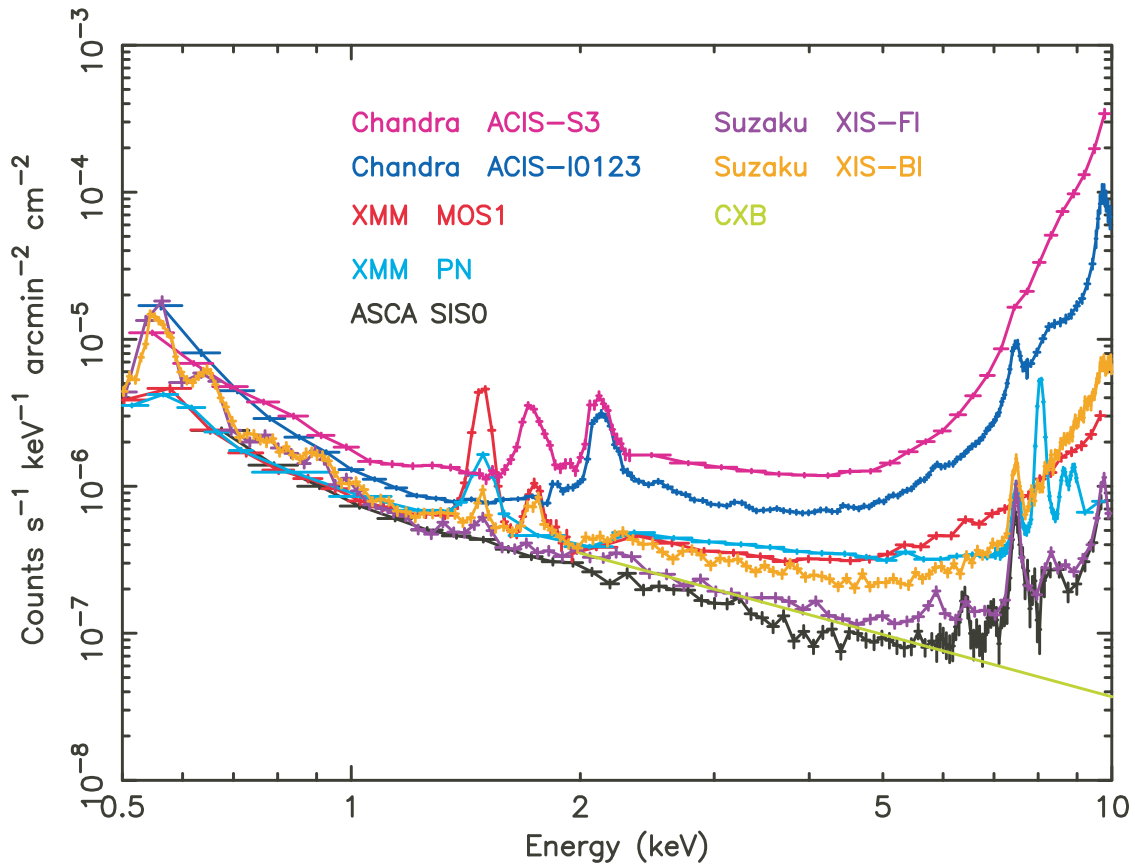

Figure 1.1: The normalized plot of the background counting rate by various satellite missions [4]. The background rate of *Suzaku*, *ASCA*, *XMM-Newton*, and *Chandra* adopted from Katayama et al. (2004) [5] are shown for comparisons.

Future X-ray astronomical satellite missions will require a new type of detectors that can distinguish X-rays and charged particle tracks, so as to reduce the background level. The new detector must have good coincidence time resolution ($\sim 1\ \mu$s), superior hit-position readout time ($\sim 10\ \mu$s) in order to reduce the NXB by cosmic rays. By introducing an anti-coincidence method between the hit signal and the external active shield detector [6] [7], the background produced by the cosmic ray tracks [8] can be greatly reduced. This is particularly important for the observation of hard X-rays with energies above 10 keV. In addition, it must have wide bandpass (from soft to hard X-rays, 0.3 – 40 keV), and comparable performance in terms of imaging spectroscopy [9] [10].

Active pixel sensors (APSs) have attracted considerable attention recently for their improved performance, which is close to that of CCDs in terms of small pixel size and low readout noise [11]- [13]. The advantage of the APS is the ability to directly access the selected pixels, which results in a faster readout. Furthermore, the APS can generate a hit timing signal instantaneously; therefore, it can achieve much better timing resolution than

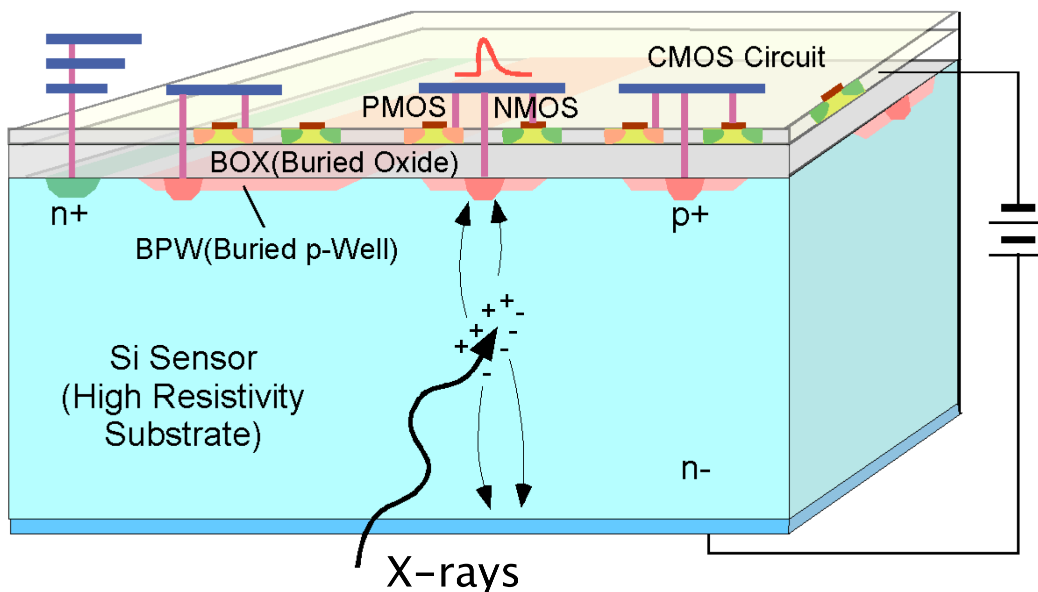

Figure 1.2: Cross sectional view of the SOI pixel detector.

CCDs. Hybrid pixel sensor like Medpix [14] is one of the candidates to realize above requirements. However, the spectroscopic performance of the sensor is limited by its counting type structure, and the yield is not so good due to the large number of bump bondings.

In order to realize the detector described above, we have been developing a new type of APS called XRPIX based on the semiconductor pixel detector with the silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) technology. This new technology, i.e., SOI pixel detector (SOIPIX), has been developed by High Energy Accelerator Research Organization (KEK) in recent years. The SOI wafer is a bonding of two silicon wafers and a thin oxide film in between. The pixel detector consists of low resistivity silicon of a circuit and high resistivity silicon of a sensor. The SOIPIX utilize a thick handle wafer of SOI structure as a radiation sensor to detect charged particles and X-rays (Figure 1.2). Therefore, it is realized the ideal monolithic active pixel sensors. Thereby, we designed "Event-Driven SOIPIX" with a trigger information output function as "XRPIX series". And we realize the spectroscopy system which reduce background rate of the NXB by two orders of magnitude compared with the CCD. Finally, we aim to employ the XRPIX in the next generation X-ray astronomical satellite.

This thesis describe about basic development of the new detector for future X-ray astronomy. Furthermore, development of SOIPIX which is the new detector technology

is also included. We designed this detector and show performance by evaluation of the prototype. The remaining part of the thesis proceeds as followings. In Chapter 2, we review the technology related to SOIPIX. Then, we describe our new semiconductor pixel detector with SOI technology, “SOIPIX” in Chapter 3. Moreover, we introduce my design, “XRPIX” which is event-driven type SOIPIX for future X-ray astronomical satellite mission in Chapter 4. In Chapter 5, we show the evaluation results of XRPIX. Finally, the discussion and the conclusion of this thesis are given in Chapter 6 and Chapter 7, respectively.

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Chapter 2

Review of Pixel Detector Technology

In order to understand a radiation semiconductor detector, it is necessary to get to know about a semiconductor and interaction with a radiation. Obviously, it corresponds also to the SOIPIX detectors. This chapter describes these contents briefly. Moreover, existing pixel detectors other than the SOIPIX detectors are also introduced.

2.1 Semiconductor Physics

2.1.1 p-n Junction

The reversely biased p-n junction is the basic building block of silicon sensors. It builds up an electric field that collects the signal charge and suppresses the leakage current, an important noise source. A pixel sensor is a reversely biased p-n diode with a highly segmented cathode or anode.

2.1.2 Depletion Region

A depletion region is made by p-n junction. In this region, the electric field which goes to p-type from n-type has occurred. The electron-hole pairs generated in this region moves by an electric field. And the electron-hole pairs generated outside this region disappears by re-combination. Therefore, this region is important in order to detect charged particles and photons. The depletion region spreads by applying the reverse bias voltage of p-n junction.

Depletion Depth

The depth of a depletion region is calculable. The depth x_p and x_n of depletion region in a p-type and n-type semiconductor, respectively,

$$x_p = \sqrt{\frac{2\epsilon(V + V_{bi})}{qN_A(1 + N_A/N_D)}},\ x_n = \sqrt{\frac{2\epsilon(V + V_{bi})}{qN_D(1 + N_D/N_A)}} \tag{2.1}$$

ϵ is a permittivity of semiconductor. In case of silicon, ϵ is 1.0×10^{-12}. V is a reverse bias voltage. V_{bi} is a built-in potential of p-n junction. q is a elementary charge ($= 1.602 \times 10^{-19}$). N_D is a donor concentration and N_A is an acceptor concentration. Then, the depletion depth, W_{dep} is shown by

$$W_{dep} = x_p + x_n = \sqrt{\frac{2\epsilon(V + V_{bi})}{q}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)} \tag{2.2}$$

The case of the p-n junction of a general semiconductor detector is considered. That is, a large difference is to donor concentration and acceptor concentration ($N_D \ll N_A$). Thus, W_{dep} is

$$x_p = \sqrt{\frac{2\epsilon(V + V_{bi})}{qN_A^2}} \ll x_n = \sqrt{\frac{2\epsilon(V + V_{bi})}{qN_D^2}} \simeq W_{dep} \tag{2.3}$$

In this case, the depletion region spreads in n-type semiconductor. Furthermore, by using Formular (2.3) and resistivity of n-type semiconductor, $\rho = 1/q\mu N_D$, W_{dep} is

$$W_{dep} = \sqrt{2\epsilon\mu\rho(V + V_{bi})} \tag{2.4}$$

W_{dep} is proportional to the square root of resistivity of silicon wafer and reverse bias voltage from this formula.

Depletion Capacitance

A depletion region is served as a capacitor. The capacitance of this region, C_{dep} is calculable. The junction depletion region capacitance per unit area is defined as

$$C_{dep} = \frac{dQ}{dV} = \frac{dQ}{\frac{dQ}{\epsilon}W_{dep}} = \frac{\epsilon}{W_{dep}} \tag{2.5}$$

, where dQ is the incremental change in depletion region charge per unit are for an incremental change in the applied voltage dV. By using Formula (2.4), Formula (2.5) is

$$C_{dep} = \sqrt{\frac{\epsilon}{2\mu\rho(V + V_{bi})}} \tag{2.6}$$

Furthermore, when it changes about V,

$$V = \frac{\epsilon}{2\mu\rho} \cdot \frac{1}{C_{dep}^2} - V_{bi} \tag{2.7}$$

From this, V is proportional to $1/C_{dep}^2$. This relation is used by CV measurements (Section 5.3).

2.2 Radiation

2.2.1 Photon Interactions

Photoelectric Absorption

The photo electric effect is the absorption of a photon by an atomic electron which is hence moved into the conduction band. It is the dominant process at low photon energies, in silicon below about 100 keV as shown in Figure. Its cross section is very strongly dependent on the nuclear charge Z of the absorbing material: with n varying between 4 and 5 depending on the photon energy. For this reason high-Z materials like cadmium telluride are preferred for X-ray detection. Silicon is used for photon detection up to energies of about 100 keV [1].

Compton Scattering

At higher energies the photoelectric cross section drops down several orders of magnitude and scattering processes become more important. The cross section of Compton scattering is only linearly dependent on Z.

Pair Production

At energies exceeding twice the electron mass pair production also contributes to the cross section and becomes the only important process at energies exceeding 10 MeV.

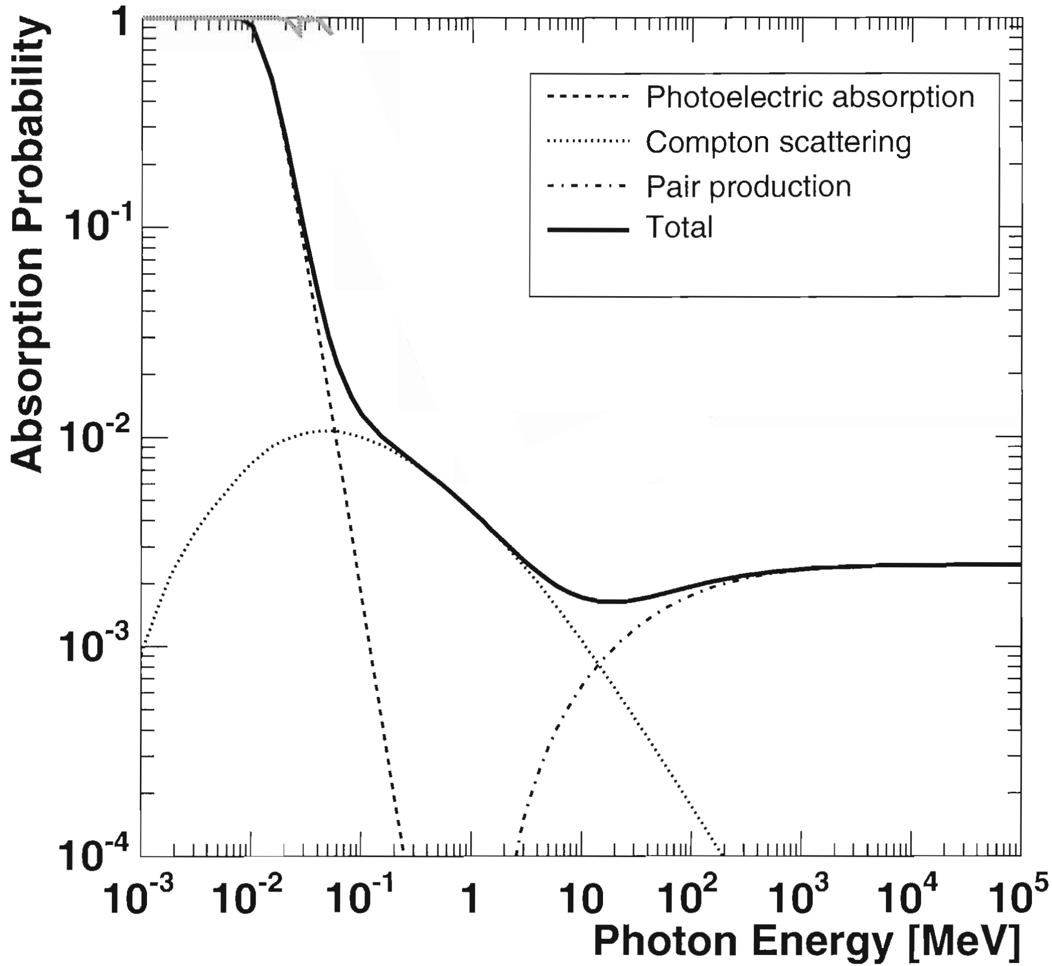

Figure 2.1: Probability of photon absorption for 300 μm silicon as function of the photon energy. Contributions from different process are indicated [1].

2.2.2 Charged Particle Interactions

Ionization Loss

Charged particles deposit a part of their energy through many scattering processes with electrons of the absorbing material along the particle track. This process is dominant for particles heavier than electrons and described by the *Bethe-Bloch formula* :

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left(\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 + \cdots \right), \tag{2.8}$$

$\frac{dE}{dx}$ is energy loss of the particle usually given in $\frac{eV}{g/cm^2}$. K is $4\pi N_{Ave} r_e^2 m_e c^2$ $(= 0.307\ MeV\ cm^2)$. z is charge of the traversing particle in units of the electron charge. Z is atomic number of absorption medium (14 for silicon). A is atomic mass of absorption medium (28 for silicon). $m_e c^2$ is rest energy of the electron (0.511 MeV). β is velocity of the traversing particle in units of the speed of light. γ is Lorentz factor $1/\sqrt{1-\beta^2}$. I is mean excitation energy (137

eV for silicon) [1].

2.2.3 Fano Factor

The average number of electron-hole pairs, N, generated for a constant amount of absorbed energy, e.g., caused by a radio isotope of X-rays, can be calculated by dividing the absorbed energy E by the average energy necessary to produce one electron-hole pair, w:

$$N = \frac{E}{w} \tag{2.9}$$

The energy w required to create an electron-hole pair is about 3.65 eV in silicon. This value, which is more than three times larger than the band gap of 1.12 eV, is a material property and does hardly depend on the type and energy of the radiation if the latter is much larger than the band gap. The difference generates phonons, which in the end will dissipate as thermal energy.

The fraction of deposited energy that is used for electron-hole separation and phonon generation is subject to fluctuations which N to vary by

$$\left\langle \Delta N^2 \right\rangle = FN = F\frac{E}{w} \tag{2.10}$$

with F begin the *Fano factor*. If the fraction of the absorbed energy used for the electron-hole pair generation would be fixed, their number N would also be fixed and the value of F would be zero. The Fano factor F, however, is, according to theoretical works, in the order of ∼0.1 for most semiconductors and determines the best possible energy resolution of semiconductor sensors in spectroscopic applications.

The energy resolution of a detector is decided by the statistical fluctuation of an electron obtained and equivalent noise charge (ENC) of readout circuit. ΔE_{FWHM} is shown by

$$\Delta E_{FWHM} = 2.35w\sqrt{E_\gamma(F + f)/w + \sigma^2} \tag{2.11}$$

E_γ is a photon energy. F is a *Fano factor*. f is a statistics factor showing the amplification effect. Since amplification is not performed in the case of silicon, f is 0. σ is an ENC of readout circuit. A value in case σ of Formula (2.11) is zero is a spectroscopic performance limit, i.e., Fano limit of a detector [1].

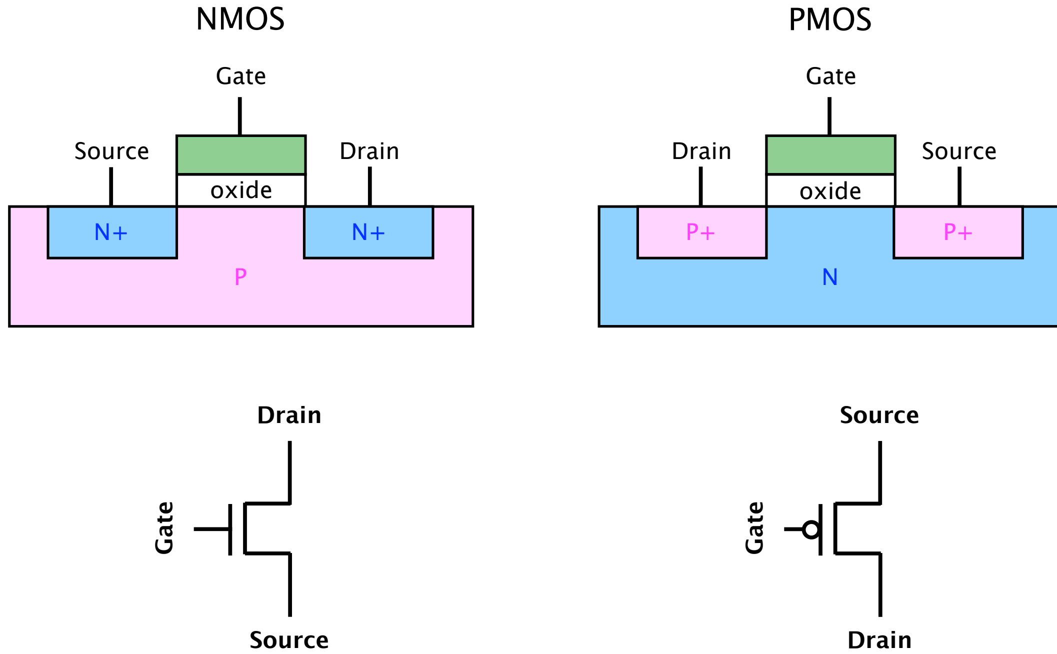

Figure 2.2: Cross sectional view and symbol of NMOS and PMOS (e.g., CMOS).

2.3 Analog CMOS Circuit

2.3.1 CMOS

The circuit by CMOS is used for a large-scale integration (LSI) circuit. It consists of NMOS and PMOS which are the contrastive pairs of metal oxide semiconductor field effect transistors (MOSFETs). Figure 2.2 shows the cross sectional view and symbol of NMOS and PMOS transistors. "N" and "P" shows n-type and p-type semiconductors respectively. The analog and the digital circuit consist of combination for these. The symbol of Figure 2.2 is used with the circuit schematic of this thesis.

2.3.2 Clock Feedthrough

In analog CMOS circuit, a MOS switch couples the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance. The effect introduces an error in the sampled output voltage. Assuming the overlap capacitance is constant, we express the error as

$$\Delta \mathrm{V} = \mathrm{V}_{\mathrm{CK}} \frac{\mathrm{WC}_{\mathrm{ov}}}{\mathrm{WC}_{\mathrm{ov}} + \mathrm{C}_{\mathrm{H}}} \tag{2.12}$$

where C is the overlap capacitance per unit width. The error V is independent of the input level, manifesting itself as a constant offset in the input / output characteristic. As with charge injection, clock feedthrough leads to a trade-off between speed and precision as well.

2.3.3 kT/C Noise

The kT/C noise is a reset noise. A similar effect occurs in sampling circuits. The on-resistance of the switch introduces thermal noise at the output and, when the switch turns off, this noise is stored on the capacitor along with the instantaneous value of the input voltage. It can be proved that the rms voltage of the sampled noise in this case is still approximately equal to kT/C.

2.4 Other Pixel Detector Technology

The technology of some pixel detectors has been developed until now. Some typical silicon semiconductor detectors are introduced in this section. It is common that these collect the electric charges (electron-hole pairs) generated by the interaction with silicon. These differences are the methods of processing as a subsequent signal. In the following sections, they are also described.

2.4.1 CCD

One of the pixel detectors used for a long time has the charge coupled device (CCD). This is detectable in a wide-band from visible light to X-rays. As the Chapter 1 described, it is a standard detector also in X-ray astronomy. It was invented in 1969 at Bell Labs by Willard Boyle and George E. Smith. The principle of operation is transmitting an electric charge, and reads it as a signal. Figure 2.3 shows this principle model. The pixel size is several μm to about tens of μm. It has high spectroscopic performance. However, manufacture is difficult because of a complicated structure. Moreover, it is very expensive. Therefore, it is being transposed to a CMOS image sensor in recent years.

2.4.2 Medipix

The VLSI front-end prototype chip (Medipix) has been developed at the European Organization for Nuclear Research (CERN) [3]. Development of this detector was started from the

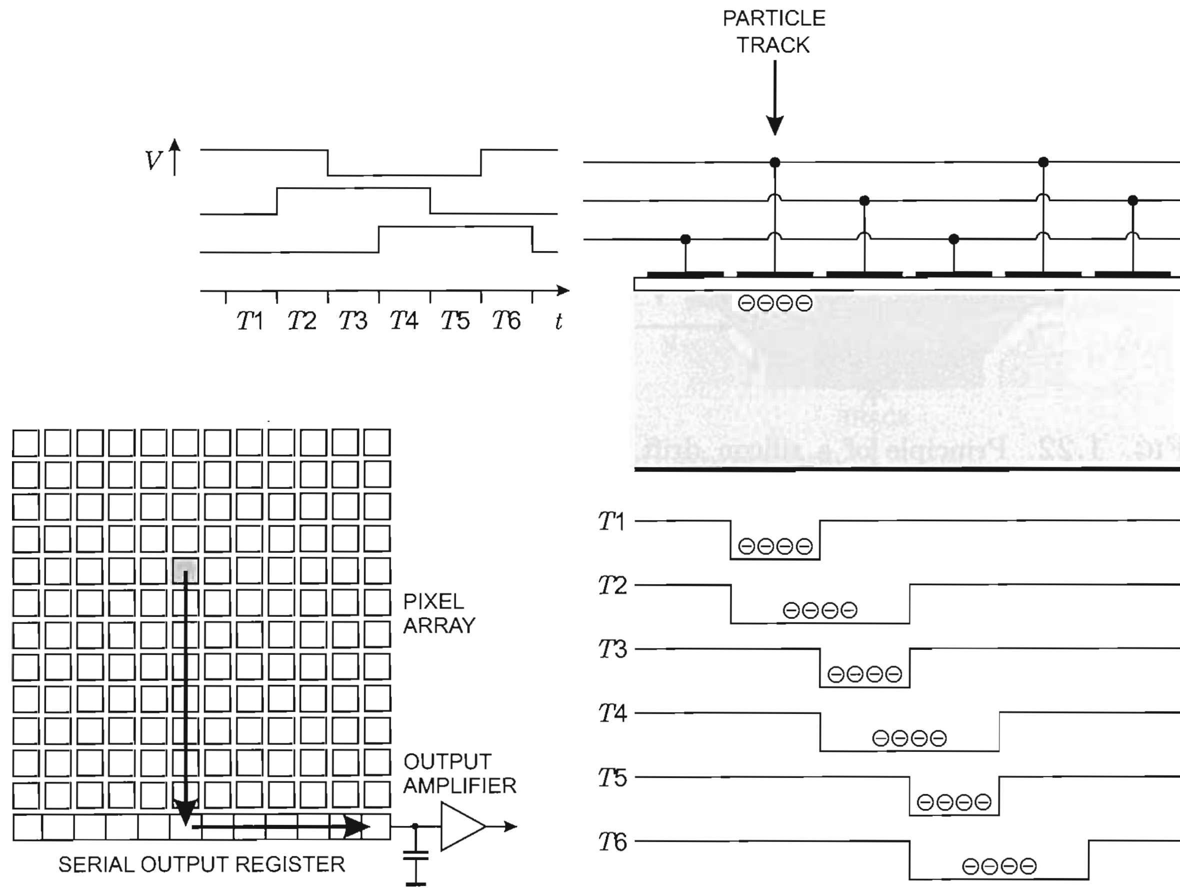

Figure 2.3: Principle model of CCD [2]. Upper right: schematic cross-sectional view of a CCD. Voltages are applied to the electrodes according to the timing diagram at the upper left. The potential sequence shifts the charge from the track to the right Three electrodes comprise one pixel, but all charge from the track subtended by the pixel is drawn to the pixel's left-most electrode. Six clock periods shift the charge to the neighboring pixel. The pixels are read out sequentially (bottom left). Charge is transferred down the transferred to the readout line by the output amplifier.

latter half of the '90s. It is used as a radiation pixel detector of a high energy experiment and X-ray imaging. Figure 2.4 is a schematic view of Medipix. It is the structure of making a sensor and readout circuit independently and connecting them by a metal bump (i.e., Hybrid type detector). The pixel size is 55 μm square [5]. Operation of a detector is a counting type. The module by a USB interface also exists in this detector.

2.4.3 DEPFET

The DEPleted-Field Effect Transistor (DEPFET) principle has been proposed in 1985 at Max-Planck-Institut (MPI), Germany by Kemmer and Lutz [6]. It is used as a radiation pixel detector of a high energy experiment (e.g., Belle II and ILC experiment [7]) and a future X-ray astronomical satellite mission (e.g., *Athena+* [8]). It is a monolithic active

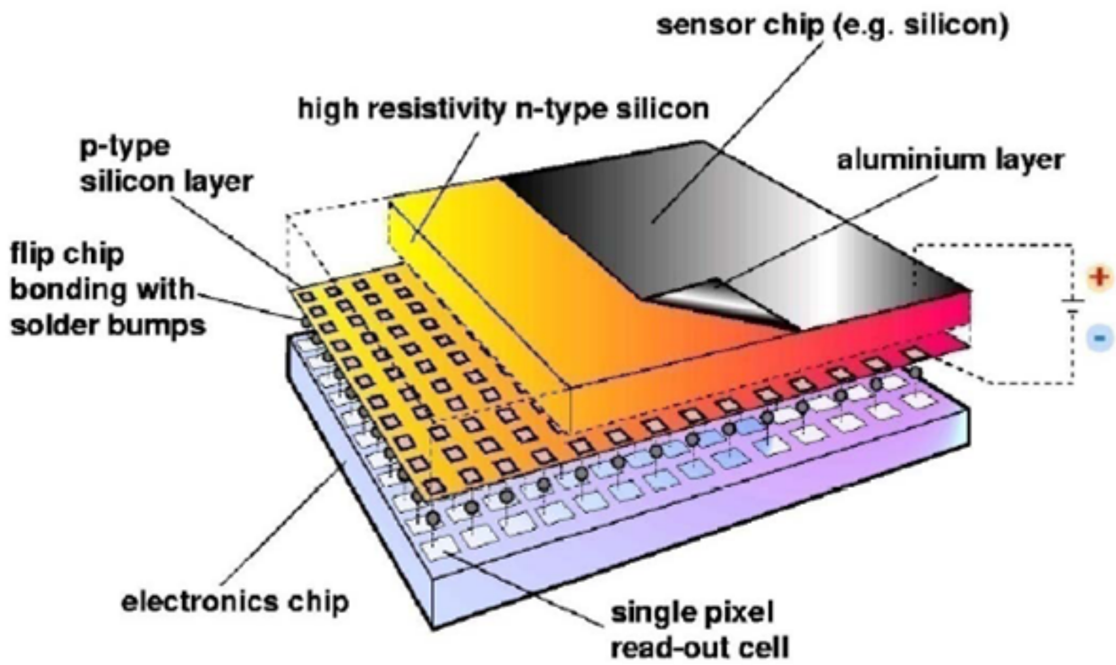

Figure 2.4: Schematic view of Medipix [4].

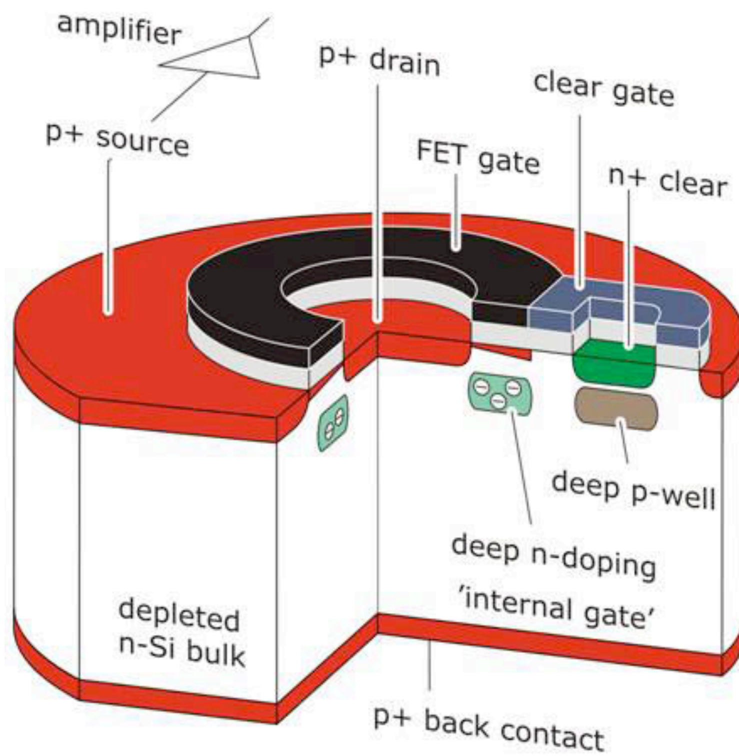

Figure 2.5: Cross sectional view of DEPFET [8].

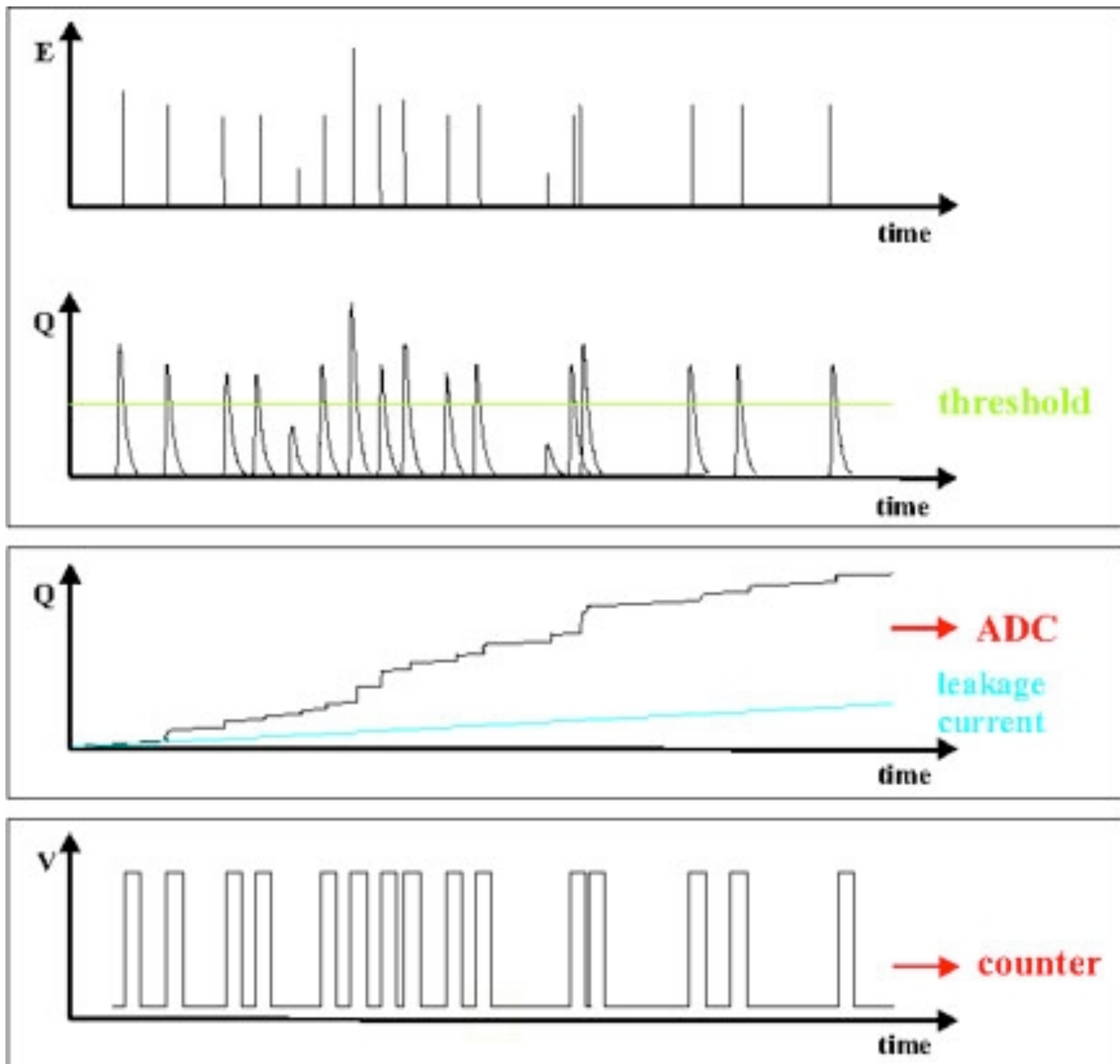

Figure 2.6: Principle of single-photon counting detectors vs. integrating detectors.

pixel detectors. Figure 2.5 shows the structure of DEPFET. The pixel size is about 25 μm. The characteristics of this detector is operation by "internal gate" and "clear gate". This detector collects the generated electric charges to a internal gate, and reads the signal according to the number of electric charges. The electric charge held at the internal gate is drawn out from a clear gate.

2.4.4 PILATUS

At the Swiss Light Source (SLS)[1] at the Paul Scherrer Institut (PSI) in Switzerland, a single photon counting pixel detector called PIxeL ApparaTUs for the SLS (PILATUS) has been developed for X-ray applications since 1997 [9]- [11]. Figure 2.6 shows the principle of single

[1] http://www.psi.ch/sls/

photon counting. This is also the detector proved about the usefulness of photon counting in X-ray imaging. The PILATUS is established as a product and is sold from DECTRIS Ltd.[2] which is founded by 2006. This has wide-spread in the market as application of X-ray imaging.

2.4.5 MIMOSA

In the early 1990s a monolithic active pixel sensors (MAPS) was proposed. This detector, called Minimum Ionising particle MOS Active pixel (MIMOSA) [12], is developed as virtex detector of a high energy experiment (e.g., ILC experiment). It is used of the epitaxial layer of standerd CMOS processes as detecting sensitive volume.

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Chapter 3

SOI Pixel Detector

The SOI pixel detector (SOIPIX) is the key technology of this thesis. This development was started originally for the particle tracker in the high-energy physics experiments. However, it is soon revealed that the detector also has great potential as X-ray detectors. In this chapter, we describe this new detector development and technology.

3.1 Development of SOI Pixel Detector

In the high-energy physics experiment, semiconductor pixel detectors are widely used and located near the interaction point of colliding beams in order to know the track of particles with high accuracy. At present, the pixel detectors used in the experiment are consist of the sensor and circuit substrates, and those are connected by metal bumps (i.e., Hybrid type detector). This is that it is difficult to build both radiation sensor and circuit in a single substrate. Radiation sensors need thick depletion region, so high-voltage and high-resistive wafer are required. On the other hand, CMOS LSI circuits work only in low-voltage environment and low-resistive wafer is used to avoid latch-up effect etc.

However, the hybrid structure has many drawbacks. For example, it has limitation of spatial resolution by the size of the bump bondings, high multiple scattering probability due to its excessive material, and low signal speed by large parasitic capacitance. In addition, the cost of the bump technology is high due to its low yield. On the other hand, the monolithic type detector solves those disadvantages of the hybrid type. It is a detector with the structure which a sensor and readout circuit unified. However, since high resistivity silicon cannot be used for a circuit, it is difficult to obtain a thick depletion layer. In order

to conquer all of these problems, a new detector is desired for future experiments.

In Detector Technology Project (DTP) of KEK a new project to develop a semiconductor pixel detector using the SOI technology was started. It is called SOIPIX, and has been developing from 2005 [1]. The SOIPIX utilize a thick handle wafer of SOI structure as a radiation sensor to detect charged particles and X-rays. The SOI wafer is a bonding of two silicon wafers and a thin oxide film in between. Thus optimum resistivity can be selected for sensing part and circuit part respectively. By making contacts between top and bottom silicon through an oxide film, it becomes the detector which unify a sensor and readout circuitry. This is the reason that the SOIPIX is called "ideal" monolithic pixel sensor.

The SOIPIX has many advantages. For example, the mechanical bump bonding does not exist. Therefore, this is high density, low parasitic capacitance, and high sensitivity. Moreover, sensor thickness can be adjusted with polish of a sensor wafer from the thin depletion layer of a high energy experiment ($\sim 50\ \mu$m) to the thick depletion layer of X-ray application ($\sim 500\ \mu$m). This can have a complex circuit in each pixel because this is composed of standard CMOS circuit. Additionally, the price cutting can be expected because of based on industrial standard technology. Thus, SOIPIX can be applied to the high energy experiments, astrophysics, medical imaging and so on [2].

3.2 SOI Technology

SOI technology is growing greatly as a CMOS LSI process of the industry in recent years. This is because it has many advantages as compared with the bulk CMOS usually used. For example, high speed operation (i), low consumed power (ii), high integration (iii), latch-up immunity (iv), operate in wide temperature (4 – 570 K) range (v), single event effect (SEE) tolerance (vi), and so on. Figure 3.1 is the difference in a transistor model of bulk and SOI. The big feature of SOI structure is that each transistor is separated by the insulating layer of SiO_2, i.e., buried oxide (BOX). Thereby, the parasitic capacitance between elements decreases greatly ((i), (ii), (iii)) and SOI is suitable also for an integrated circuit like CPU which needs high-speed operation. Furthermore, the leakage current between elements and through a substrate is lost ((ii), (iii)). Moreover, the temperature dependency of SOI of the threshold voltage of a transistor is low (v). The ionization damage by radiation affects operation of a transistor. Since bulk layer of SOI CMOS is small as compared with bulk CMOS, there is little generation of the electric charge which causes SEE (Figure 3.2, (vi)).

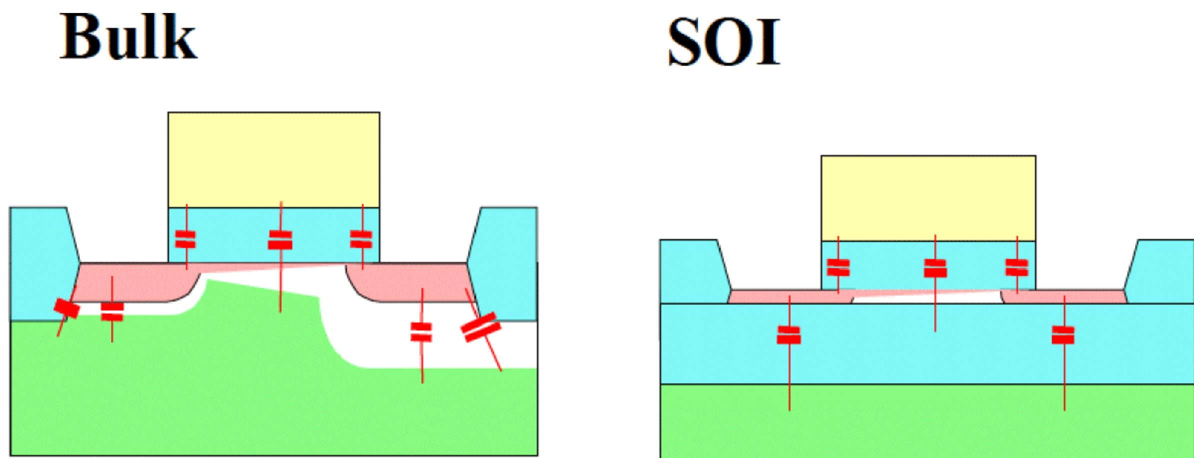

Figure 3.1: The difference in a transistor model of bulk and SOI. The left side is a bulk (normal) process. The right side is a SOI process. The SOI transistor of parasitic capacitance is smaller than bulk.

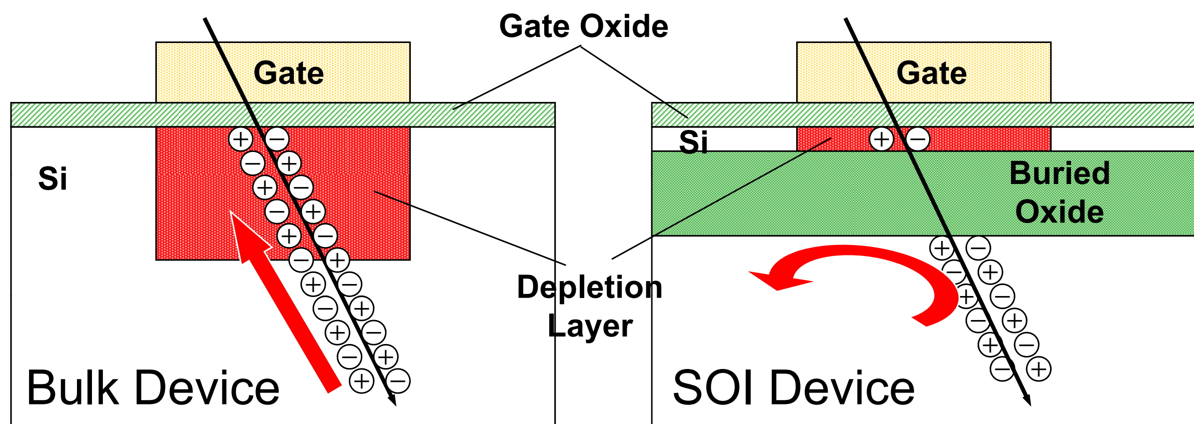

Figure 3.2: Radiation tolerance of single event effect (SEE).

Thus, existence of BOX layer gives the big benefit for a transistor.

3.3 Process of SOI Wafer

In this section, we introduce the Czochralski and Floating Zone method which is a typical generation method of a silicon single crystal, the Smart Cut^{TM} process which is a typical generation method of a SOI wafer, and the high resistivity SOI wafer which becomes important with SOIPIX.

3.3.1 Czochralski Method

The method of introducing first is Czochralski (Cz). Single crystalline substrates are typically differentiated by the process by which they are made. The Cz wafers are the most

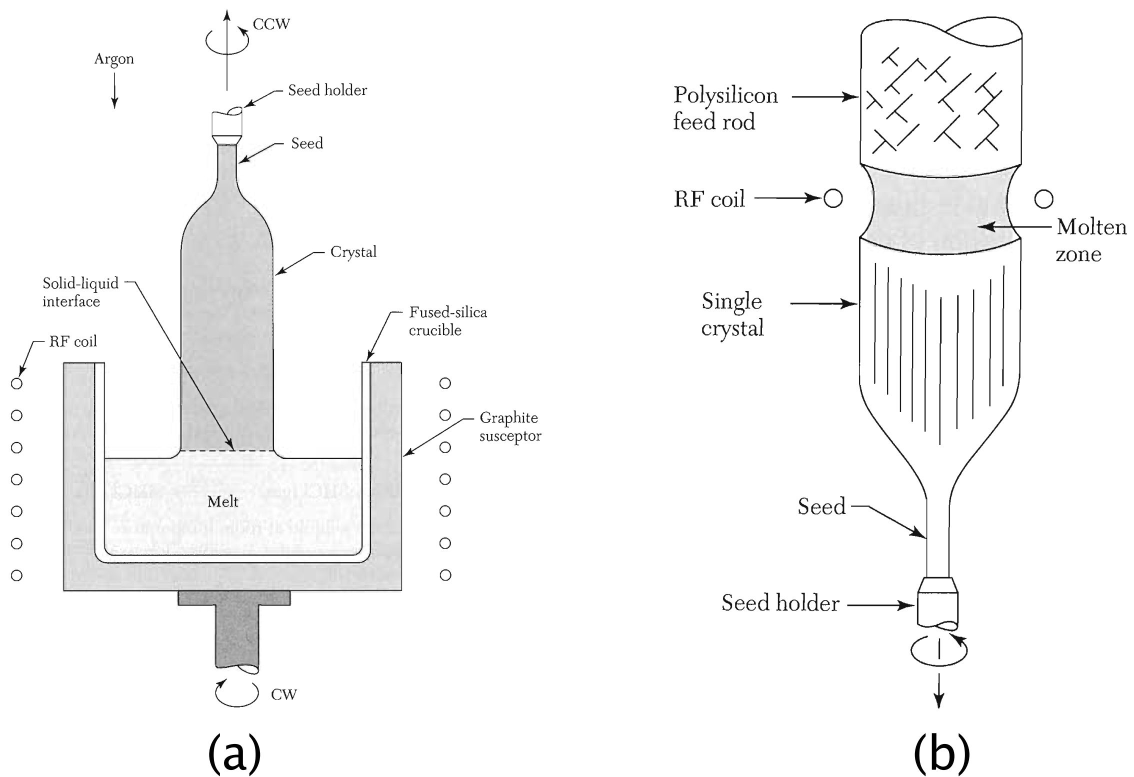

Figure 3.3: Schematic view of (a) Czochralski method and (b) Floating Zone method [3].

commonly used type of silicon wafer, and are used by both the solar and integrated circuit industry. Of course, we also use well. The process of making a large single crystalline silicon ingot by the Czochralski process is shown below. The use of quartz crucibles in the manufacture of Cz substrates causes the incorporation of ppm (10^{18} cm^{-3}) oxygen into the silicon ingot. The oxygen itself is relatively benign but creates complexes with boron doping that degrades the carrier lifetime. N-type ingots fabricated with phosphorous dopants have similar oxygen concentrations but do not show the degradation effect nor do wafers with lower resistivity or gallium dopants.

3.3.2 Floating Zone Method

The method of obtaining a crystal with high purity, i.e., high resistivity is the Floating Zone (FZ) method rather than obtained by the usual Cz method. By high-frequency heating, a new single crystal is grown up by melting few cm of width. Cz wafers contain a large amount of oxygen in the silicon wafer. On the other hand, in order not to use crucibles, this process method tends to maintain purity. Therefore, we need the wafer by FZ method, in order to obtain a thick depletion layer.

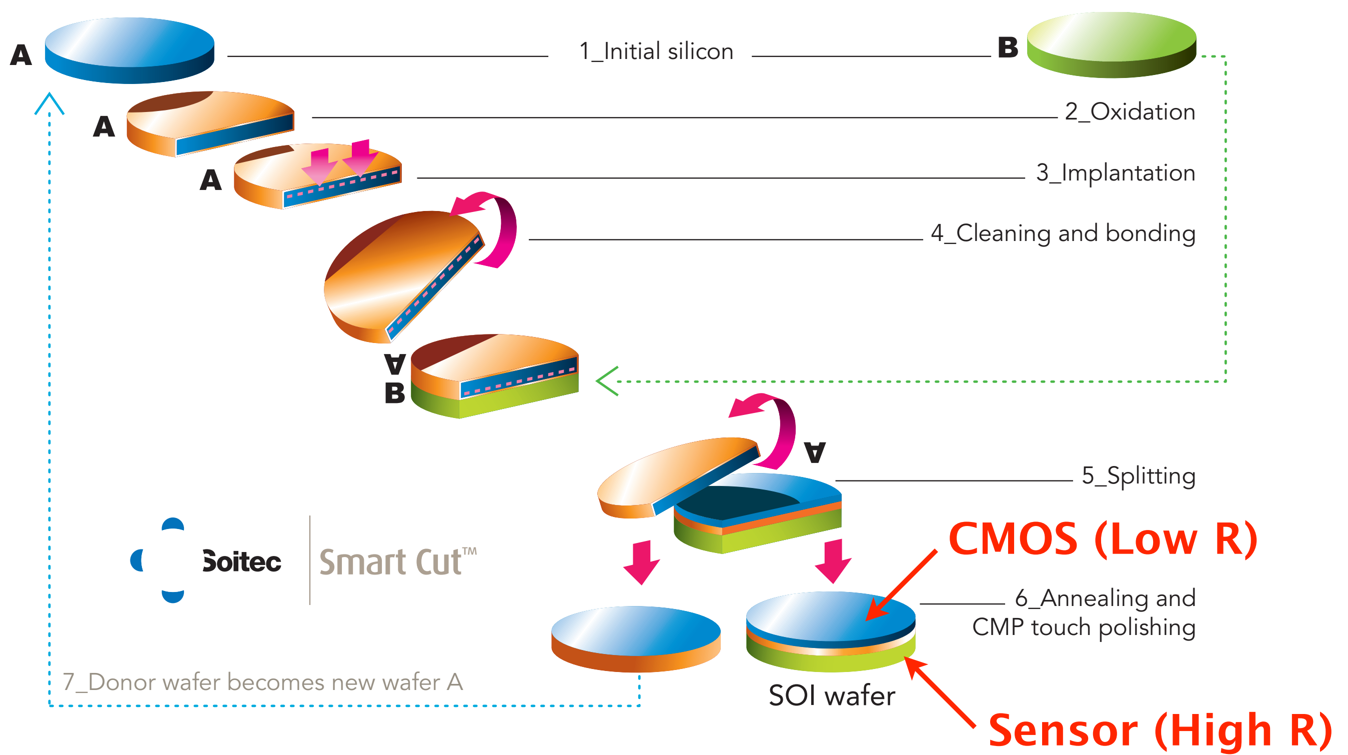

Figure 3.4: The process of Smart Cut^{TM} technology by SOITEC [6]. SOIPIX uses the special SOI wafer which has the process of the handle wafer with the high resistivity silicon wafer.

3.3.3 Smart Cut^{TM} Process

Although there are some methods of creating a SOI wafer, Smart Cut^{TM} by SOITEC is mainly used now. This process was developed by M.Bruel of CEA-LETI in 1991. Figure 3.4 shows this process technology. First, two initial silicon wafers (A and B) are prepared for Smart Cut^{TM} process. In the case of SOIPIX, they are different resistivity wafer in which the circuit (wafer A) is low and the sensor (wafer B) is high (1). Next, the wafer A is oxidized to create insulating layer (2). Then, a hydrogen ion is implanted into the wafer A to induce formation of an in-depth weakened layer. By adjusting the implant energy of ion, the thickness of a SOI layer can be changed (3). After implantation, both wafers A and B are cleaned to eliminate any particle and surface contaminants and to make both surfaces hydrophilic. Thereby, they are united as one silicon wafer (4). This wafer splits in the place which poured in hydrogen ions by heating to 400 – 600 °C (5). By annealing and chemical mechanical polishing (CMP), SOI wafer is completed (6). Furthermore, seed wafer becomes new wafer A (7). The process of the SOI wafer for SOPIX is specially made from utilizing the handle wafer in which resistivity differs.

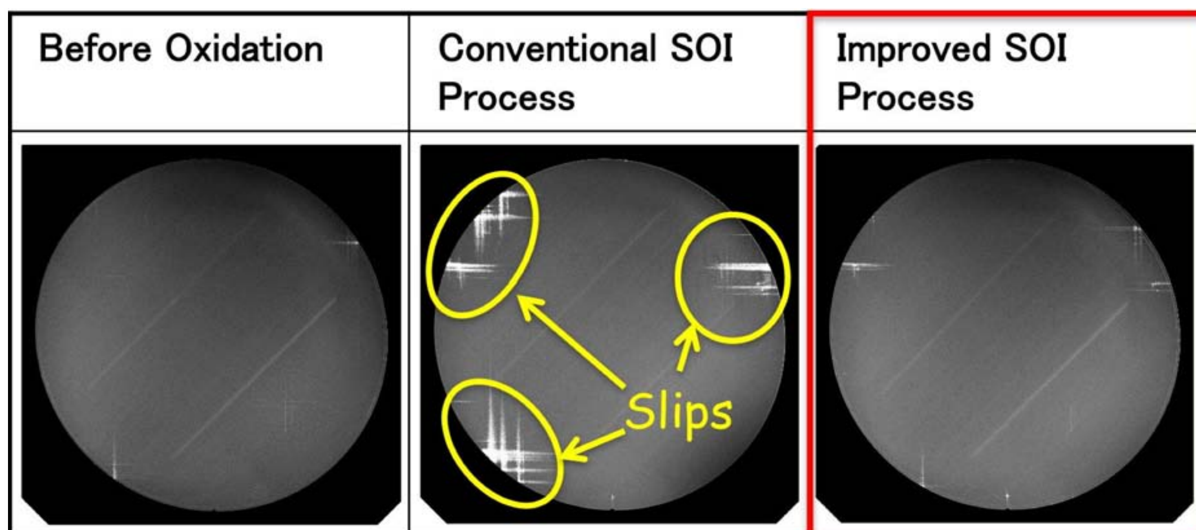

Figure 3.5: X-ray inspections of FZ-SOI wafers and slips.

3.3.4 High Resistivity SOI Wafer for SOIPIX

In order to realize a pixel detector with SOI wafer, it is necessary to make a handle wafer with high resistivity. Thereby, a depletion layer can be grown up on more low back bias voltage of sensor. From the early stages of development, the high resistivity wafer offered by the standard process of SOITEC is mainly used. This handle wafer is made in Cz method, which is n-type and has about 700 $\Omega \cdot$ cm resistivity. However, it is desirable to obtain much higher resistivity to create thicker depletion region with lower voltage. Then, we requested SOITEC and had the special SOI wafer by bonding with FZ wafer. As a result of the challenge, it was not easy to make FZ-SOI wafer of 8 inch.

Figure 3.5 shows X-ray inspections of FZ-SOI wafers. In the original process, the FZ-SOI wafer has some lattice defect (i.e., slips) which CMOS high temperature process causes into a wafer (Figure 3.5 center). After careful tuning of the high temperature process, the FZ-SOI wafer without the major slips was realized (Figure 3.5 right). The resistivity of handle wafer has about 7 k$\Omega \cdot$ cm. Furthermore, n-type and p-type have completed FZ-SOI wafer. The resistivity of handle wafer has about 40 k$\Omega \cdot$ cm. Therefore, three kinds of wafers (Cz n-type, FZ n-type, and FZ p-type) are available for SOIPIX. The results of this thesis mainly treats SOIPIX by Cz-SOI wafer (Cz-SOIPIX). Incidentally, handle wafers other than silicon (e.g., cadmium telluride (CdTe) or germanium (Ge)) do not exist for the reason of a process line.

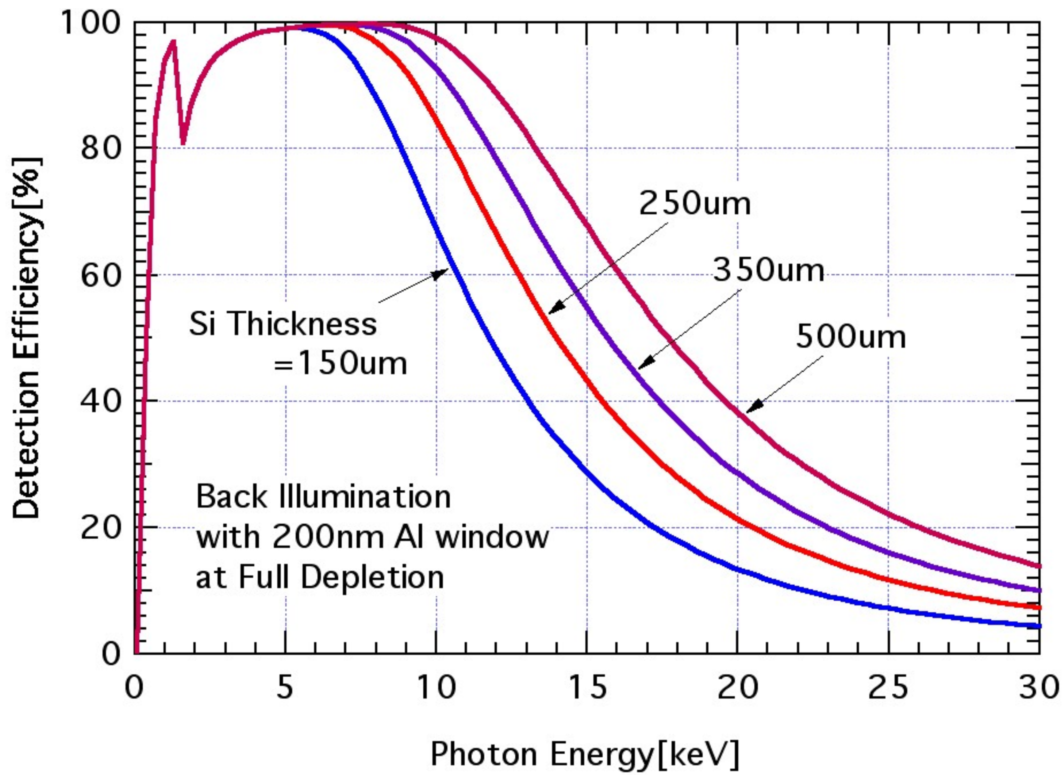

Figure 3.6: Detection efficiency of X-ray energy by sensor thickness.

3.4 SOI Pixel Process

The SOIPIX is realized based on the existing SOI technology currently used in industry. Therefore, the new process to make a pixel detector needed to be developed. This process called "SOI pixel process", and joint development with LAPIS Semiconductor Co., Ltd.[1] which is a leading company about SOI process in Japan. The company name of LAPIS Semiconductor Co., Ltd. changed from OKI Semiconductor Co., Ltd. in September, 2011. Our SOI pixel process is developed based on their 0.2 μm CMOS fully-depleted (FD-) SOI process. Thanks to the process line of a company, the quality of the process which realizes SOIPIX has been achieved. In this section, we introduce SOI pixel process currently used by SOIPIX.

3.4.1 Structure of SOIPIX

The component of SOIPIX is three layers, a circuit, BOX, and a sensor, and they are dependent on the structure of SOI wafer. The SOI wafer currently used for the process is a wafer of SOITEC and Shin-Etsu Chemical Co., Ltd.[2] The thickness of a circuit layer is

[1]http://www.lapis-semi.com/en/
[2]http://www.shinetsu.co.jp/en/

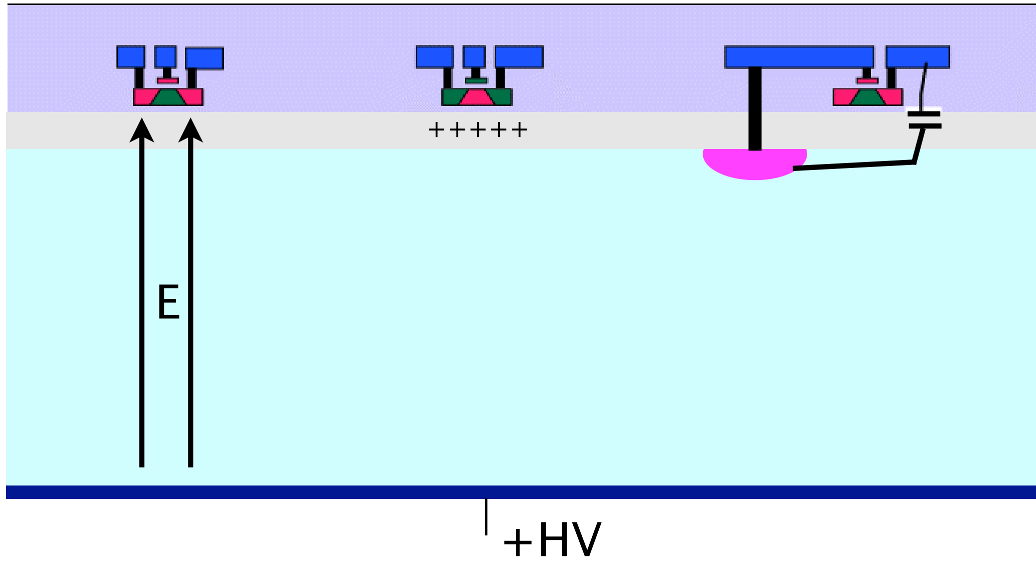

Figure 3.7: SOIPIX issues.

40 nm and BOX layer is 200 nm. The sensor layer is limited by the thickness of the handle wafer, and is 725 μm at the maximum. Although thickness is controllable by mechanical grinding a handle wafer, it can be made thin to 50 μm until now. Usually, the thickness of the sensor layer of Cz-SOIPIX is 260 μm and FZ-SOIPIX is 500 μm, respectively. On the back side of a sensor layer, chemical etching, impurities implant, laser annealing, and vapor-deposition of aluminum (200 nm) as an electrode are processed. The thickness of a sensor layer influences detection efficiency. It is important for especially X-ray application to have a thick depletion region. The detection efficiency of SOIPIX is calculable as normal silicon. Figure 3.6 shows detection efficiency of X-ray energy by sensor thickness. In order to detect the X-rays of higher energy, the sensor layer needs to obtain a thicker depletion region. This is realizable by two or more stacks of SOIPIX.

SOIPIX has some issues from the structure. They are three phenomena, back gate effect (BGE), hole trapping, and cross talk. The BGE is a difficult problem which must be solved to build SOIPIX. When high voltage is applied to the sensor, the threshold voltage of a transistor shifts under the influence of the electric field, and it become ON, i.e., stops working as a circuit. This is because the layer of a sensor and a circuit is in a very near place ($\sim$ 200 nm). In order to shield the electric field from sensor voltage to a transistor, a new structure of Buried Well (BW) and its process method were developed (see Section 3.4.2). This technology was the very big technical innovation for SOIPIX.

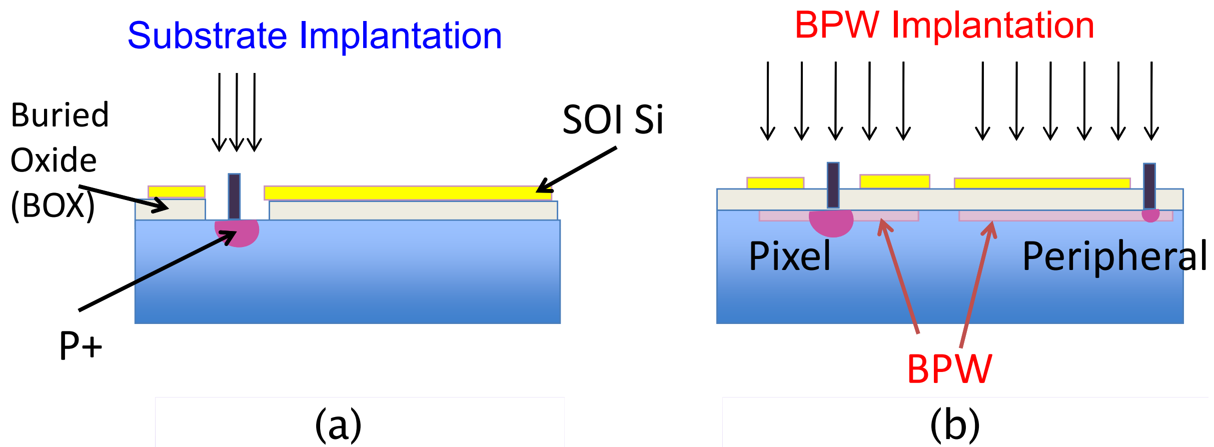

Figure 3.8: (a) Normal implantation method to create p-n junction in the substrate and (b) buried p-well implantation method. By fixing the BPW potential under peripheral circuit, the back gate effect is completely suppressed. In the pixel area, BPW may be used extend sensor area.

As the Section 3.2 described, the tolerance SEE is high, however, the problem to a hole trapping is not avoided. This phenomenon is a damage by accumulation of the radiation called Total Ionizing Dose (TID). A hole trap occurs by ionization in BOX. A circuit stops working normally by the shift of the threshold voltage of a transistor, and formation of a back channel in response to the influence of the electric charge. In the electrode of p-n junction and circuit, capacitive coupling is built by BOX. This affects a circuit, when the electric charges generated in the sensor layer are collected (i.e., cross talk). Although hole trapping and cross talk are not fatal, operation of a detector is affected not a little. These phenomena are improved by Double SOI (D-SOI) technology under present development (see Section 3.6.2).

3.4.2 Buried P-Well

As the Section 3.4.1 described, it is important to suppress BGE in order to realize SOIPIX. This was a big problem in early stages of development. The structure devised in order to solve this problem is Buried P-Well (BPW). This is the structure which made thin p layer in the sensor layer under BOX layer. By fixing the potential of this p layer, the shield of the electric field from voltage applied to a sensor layer is built. Figure 3.8 shows process method of BPW implantation. First, a hole is created by etching of BOX layer and a normal implantation is introduced into the by accelerating the impurity ions to high-energy level in order to form p-n junction in the substrate (Figure 3.8 (a)). Next, the BOX layer is formed by introducing p layer without removing a top silicon layer (Figure 3.8 (b)). Usually,

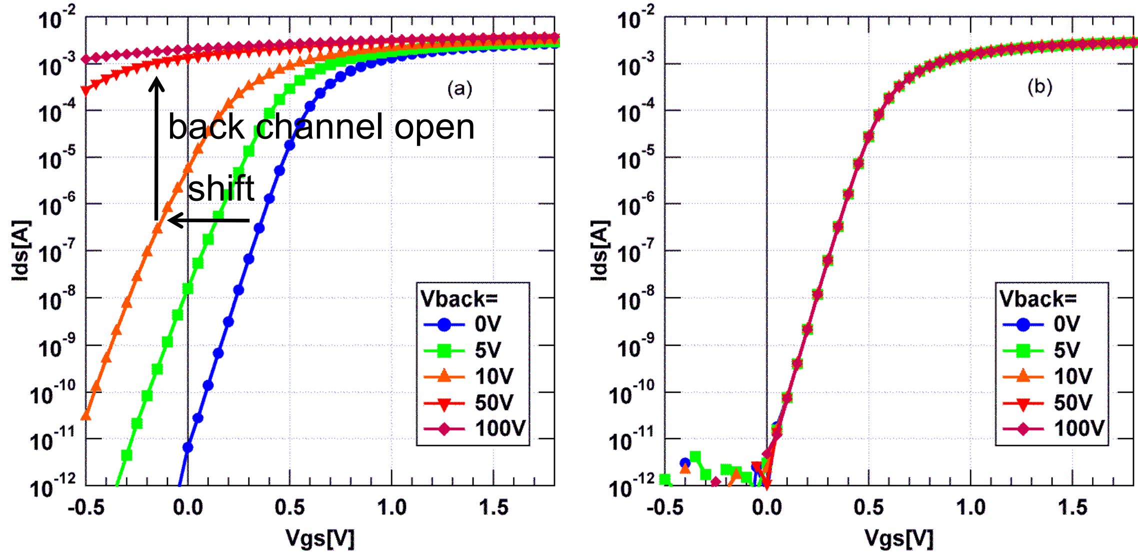

Figure 3.9: NMOS transistor Ids-Vgs curve and back side voltage. (a) Without BPW layer, (b) with BPW layer connected to ground. By introducing the BPW layer, the back gate effect is fully suppressed.

peripheral circuitry is fixed BPW layer to a grand level. Thereby, the back gate effect is completely suppressed. In the pixel area, the potential of BPW is a reset voltage level of a sensor. Therefore, the potential is completely unfixable. However, although there is potential change at the time of charge collection, it works as a shield of an electric field. In the pixel area, BPW may be used extend sensor area.

Figure 3.9 shows the plot of NMOS transistor Ids-Vgs curve and back side voltage. When there is no BPW layer, the output of NMOS transistor changes with the influences of the voltage applied to the sensor (Figure 3.9 (a)). In case of fixing BOX layer to a grand level, the output does not change (Figure 3.9 (b)). This plot shows that BGE is completely suppressed by introduction of the BPW layer.

3.4.3 Circuit Layer

The circuit layer of SOIPIX is fundamentally the same as the usual SOI process. A difference is existence of contact to the electrode of a sensor layer. Therefore, the layout of a detector can be designed like the usual SOI CMOS only by including this contact. Figure 3.10 shows the 0.2 μm FD-SOI pixel process for SOIPIX. The Core and I/O valtage are 1.8 and 3.3 V, respectively. This process has 5 metal layers for trace and 1 active layer (CMOS transistor). Moreover, metal-insulator-metal (MIM) capacitance (1.5 fF/μm^2) can consist of 3-4 metal layers. Furthermore, there is normal and low threshold transistors are available

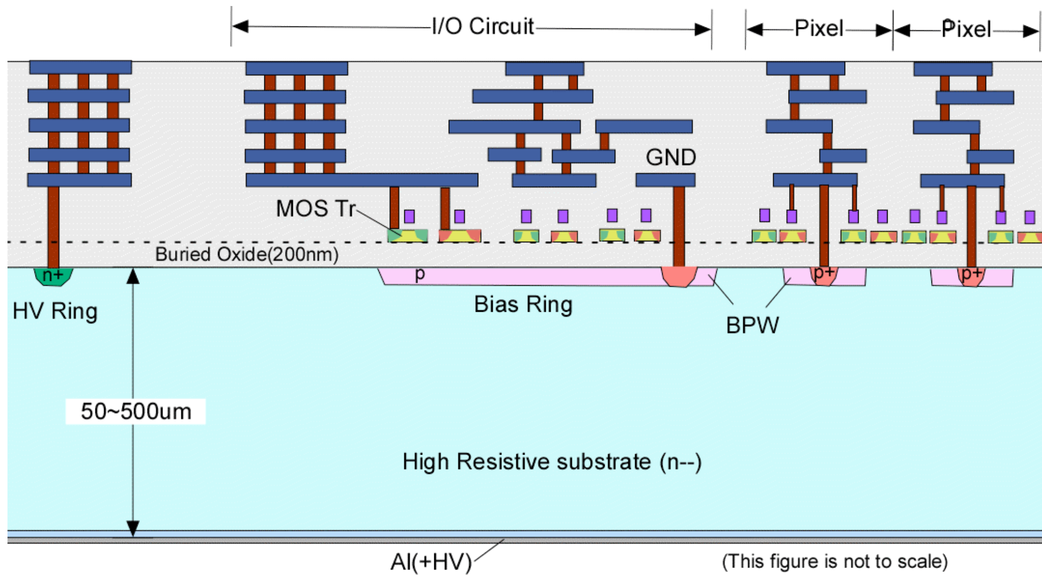

Figure 3.10: Cross sectional view of the SOI pixel process model.

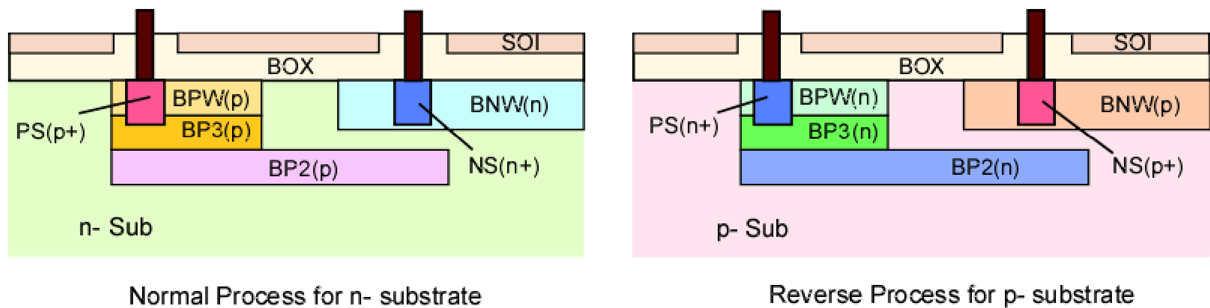

Figure 3.11: Structure of the sensor layer for n-substrate and p-substrate. Capital letters are layer name and inside of brackets shows actual doping.

for both core and IO transistors. The transistor model of structure are available three type, Body-floating, Source-tie and Body-tie.

3.4.4 Sensor Layer

In the sensor layer, the electrode is formed by p-n junction at the BOX interface, and it is made to connect with a circuit layer through via. In the present process, this electrode is called PS and NS. After introduction of BPW/BNW layers (Section 3.4.2) successfully, several additional structures implanted into a deeper sensor layer were proposed and introduced. Figure 3.11 shows present possible layers under the BOX layer. BP3 is same mask layer used in the BPW, and is used when deeper implant is required. BP2 is deepest buried layer to create nested structure with the BNW.

3.5 Multi Project Wafer Run

The cost of semiconductor process is not cheap. Major part of the cost is mask set. To reduce development cost and have multiple chances for developments, we decided to operate this SOI pixel process as Multi Project Wafer (MPW) runs. In past a few years, we have been doing the MPW runs twice per year except year 2011 when large earthquake was occurred and Lapis semiconductor fab was damaged.

In addition to many Japanese institutes, we have been collaborating with US / Europe / Asian researchers through this MPW runs. In 2011, we changed the mask size from 20.6 mm × 20.6 mm to 24.6 mm × 30.8 mm, so that we can accept more designs and build larger detector.

3.6 Development of Advanced SOIPIX Technology

In order to realize a more high specification detector, we are developing the new technology of advanced SOIPIX. In this section, we describe some technology currently developed.

3.6.1 Stitching

Large area detectors are often required in some experiments, but the mask size is limited to 20.4 mm × 30.8 mm in size now. Therefore, we have developed stitching technique to make large format detector by using only one mask set. Figure 3.12 shows the stitching method and photographs of the processed wafer.

The development is mainly driven by Riken group for the SOPHIAS detector. Since this was our first trial, we took buffer region size of 10 μm and connect only minimum number of layers (PS, NS and metal 1). However, Lapis is confident to make buffer region shorter and connects all metals.

3.6.2 Double SOI Wafer

As the Section 3.4.1 described, two problems, radiation tolerance of the detector and crosstalk between sensor-node and SOI CMOS circuit, still remain in SOIPIX. The cross talk generates the unintended signal and the circuit causes unstable operation or mistaken operation. Although the influence of SEE is small, it has influence of TID for SOIPIX. Now,

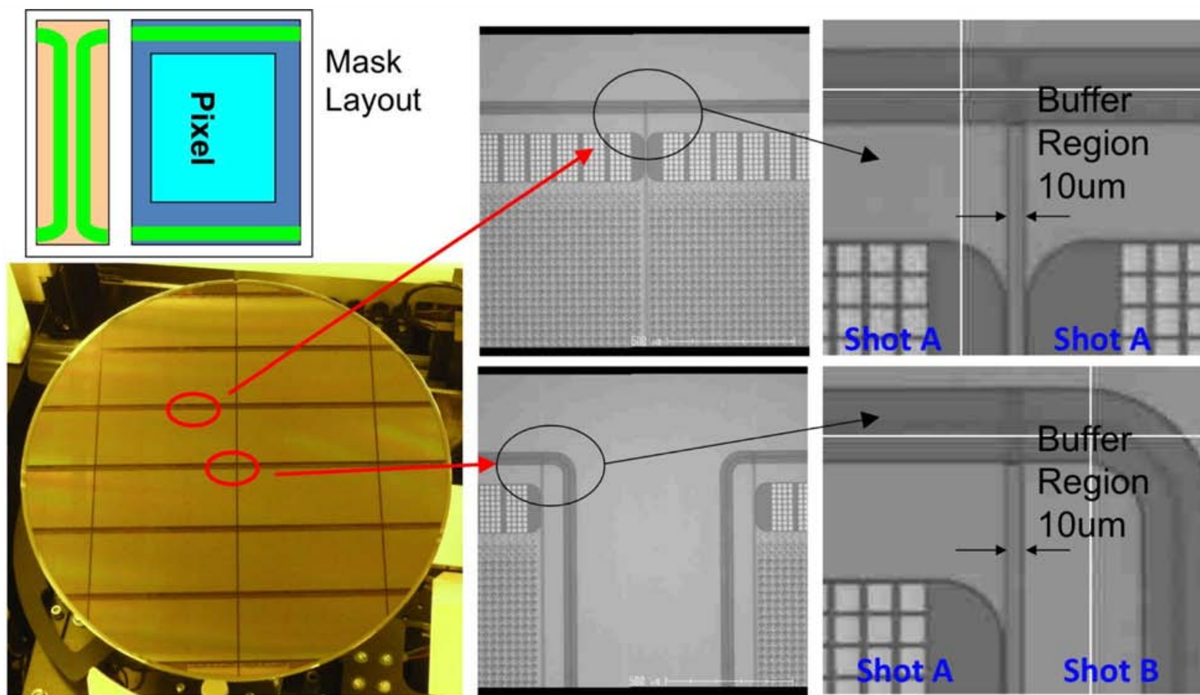

Figure 3.12: Stitching exposure for the SOPHIAS detector. Both edge structure and pixel structure and pixel structure were drawn in a mask. Part of the mask is blocked during exposure. In this detector (SOPHIAS), pixel layout was repeated 3 times and edge structures are exposed at both ends.

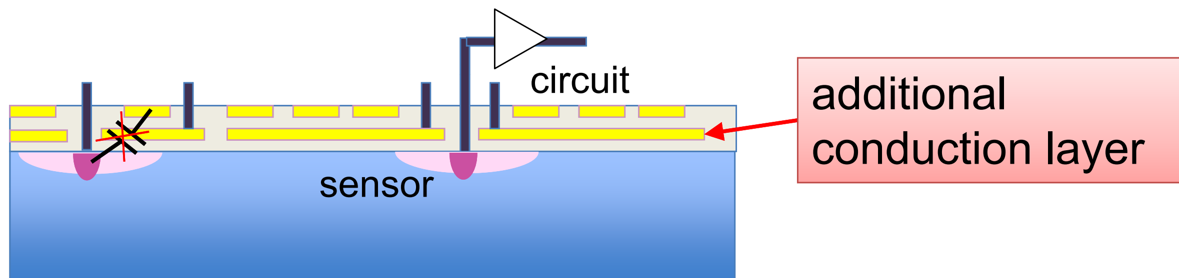

Figure 3.13: Schematic view of Double SOI wafer.

radiation tolerance is about 2 kGy. However, many applications require more than 10 kGy (1 Mrad) tolerance. In space, radiation tolerance is unnecessary compared with the high energy physics experiment. Though, it is important to suppress the cross talk.

In order to solve these problems, introduction of the another conduction (middle silicon) layer between sensor and circuit was considered. Figure 3.13 shows schematic view of this concept. This new SOI wafer is called Double SOI (D-SOI) wafer. Thereby, a cross talk can be suppressed by fixing the potential of middle silicon. Furthermore, by applying the potential of minus to middle silicon, the shift of the threshold voltage by a hole trap can be setoff. Therefore, performance of SOIPIX as a detector improves greatly by introducing

middle silicon.

The first D-SOI wafers were produced by SOITEC with n-substrate. Moreover, second D-SOI wafers have been produced by Shin-Etsu Chemical Co., Ltd., Japan, with p-type substrate. The SOIPIX with D-SOI wafer is already realized and the device is under evaluation now. By introducing D-SOI wafer, BGE can be suppressed without using BPW layer. This becomes reduction of sensor capacitance, i.e., the improvement in a gain.

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Chapter 4

Design for X-ray Astronomy

For future X-ray astronomical satellite mission, we have been developing a new detector based on SOIPIX technology. It realizes a new operation called Event-Driven readout mode by intra-pixel trigger signal. In this chapter, we introduce the design and specification of this detector.

4.1 Concept

The new detector for X-ray astronomy must have high coincidence time resolution ($\sim 1\ \mu$s), superior hit-position and signal readout time ($\sim 10\ \mu$s) in order to reduce a NXB by cosmic rays, and wide bandpass (from soft to hard X-rays, 0.3 – 40 keV) in terms of imaging spectroscopy (Chapter 1). In order to realize this performance, we have been developing a new APS based on SOIPIX, called XRPIX. It has a comparator circuit in each pixel. Therefore, it can generate a trigger signal of timing and a hit-position when X-rays and charged particles signal crosses the threshold voltage of the pixel. This can realize new operation called "Event-Driven readout mode" which judges whether it is a "real X-ray signal" for every detection events.

Figure 4.1 shows the concept of the XRPIX imaging spectroscopy system with an active shield which consists of scintillation counters. Most importantly, the anti-coincidence system with an active shield (rejection with timing) and the X-ray hit-pattern selection (rejection of events spread over pixels caused by charged particles), both of which can be realized with the APS, is expected to reduce the space NXB in the hard X-ray band. Furthermore, high-speed readout is also realized because only the pixel which detected X-rays direct access

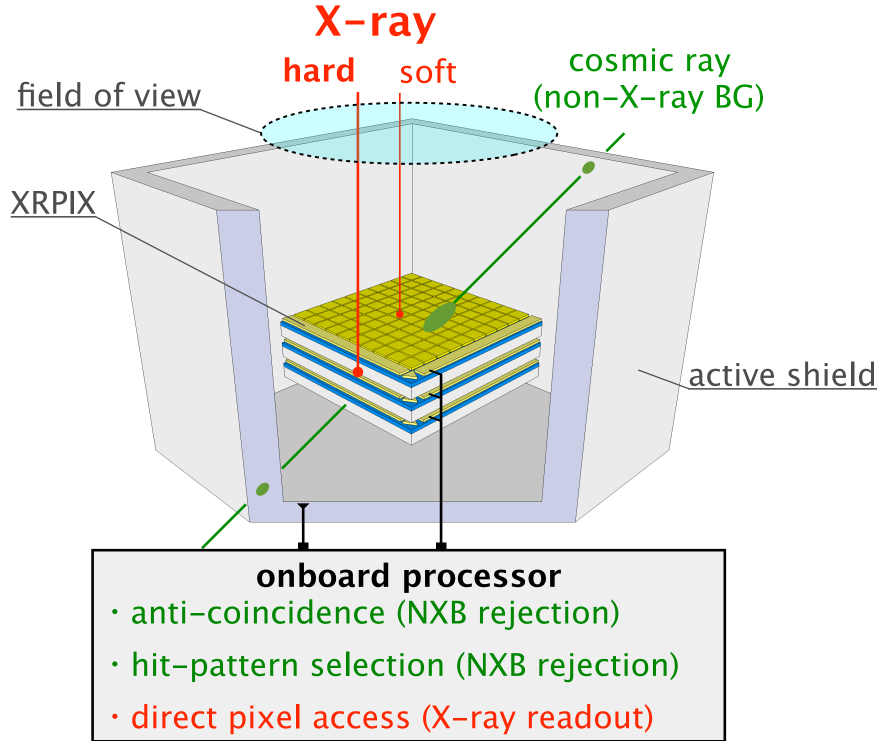

Figure 4.1: Concept of an active shield system with XRPIX to reduce the NXB by cosmic rays. The active shield can be a scintillation counter (e.g., a BGO) read out by avalanche photodiodes (APDs).

and reads a signal by the hit position information obtained from XRPIX.

The anti-coincidence system is important for reject NXB. The X-ray signals which are a candidate for observation condense by the mirror and come from the upper part of XRPIX. On the other hand, XRPIX have to remove NXB which comes from various directions. First, NXB from the upper part is discriminable with the trigger timing signal from several stack XRPIXs. The other NXB is discriminable with the trigger timing signal from an active shield and XRPIXs. There are two cases in this NXB with what is the charged particle itself, and is the X-ray of fake signals generated by the interaction of charged particle with the lens barrel. Thus, the NXB is identified by the coincidence of the trigger timing signal from XRPIXs and an active shield; i.e., X-ray signals are discriminable by anti-coincidence with NXB. Additionally, the detection efficiency over high energy X-rays also improves by two or more stacks of XRPIX.

Furthermore, NXB is also excluded by a hit-pattern selection. X-rays generate electron-hole pairs to a narrow region by an interaction. As a result, a hit pattern becomes only one or two pixels. On the other hand, charged particle events spread over in the wide area

pixels. Therefore, it can be judged with a hit-pattern whether it is NXB. If the hit-pattern selection is simple, it can be processed in the digital circuit of XRPIX, and it can also perform advanced processing by reading to external FPGA. By XRPIX, the highly efficient detector which have high spectroscopic performance and fast signal readout is realized in the future.

4.2 XRPIX Series

As the Section 4.1 described, XRPIX is Event-Driven SOIPIX which can readout analog signal only from hit pixel. There are no other detectors which can perform such operation in the world. In this section, we describe the history of XRPIX series.

4.2.1 XRPIX Project

XRPIX project started in 2009 with the Kyoto University. The basic structure of XRPIX is the same as that of the integration-type SOIPIX. Furthermore, it has trigger generation function. XRPIX series has designed six devices of XRPIX1/1b/2/2b/3/3b until now (Figure 4.2). All the devices have been designed by changing a pixel circuit, structure, a chip size, and so on. XRPIX1 to XRPIX2b were designed as a prototype for realizing event-driven readout mode, and XRPIX3/3b was designed for improvement spectroscopic performance. They were fabricated using the 0.2 μm FD-SOI CMOS pixel process by LAPIS Semiconductor Co., Ltd. We designed all the devices except XRPIX1. Moreover, we also developed FPGA for XRPIX control, and DAQ software. In the following sections, we describe the specification of each device.

4.2.2 XRPIX1

XRPIX1 is a first prototype of XRPIX series. It was designed by A-R Tec. Corporation[1] in order to verify the response of X-rays and operation of a comparator circuit. And it was fabricated in 2010, 3rd MPW run of 0.2 μm SOI pixel process (FY09-1). It is 2.4 mm $\times$ 2.4 mm in size and consists of 32 $\times$ 32 pixels. The pixel size is 30.6 μm $\times$ 30.6 μm, so the effective sensing area is approximately 1.0 mm $\times$ 1.0 mm. For the sake of comparison and evaluation, it consists of four different types of test element group (TEG) pixels. Each TEG

[1] http://www.a-r-tec.jp/

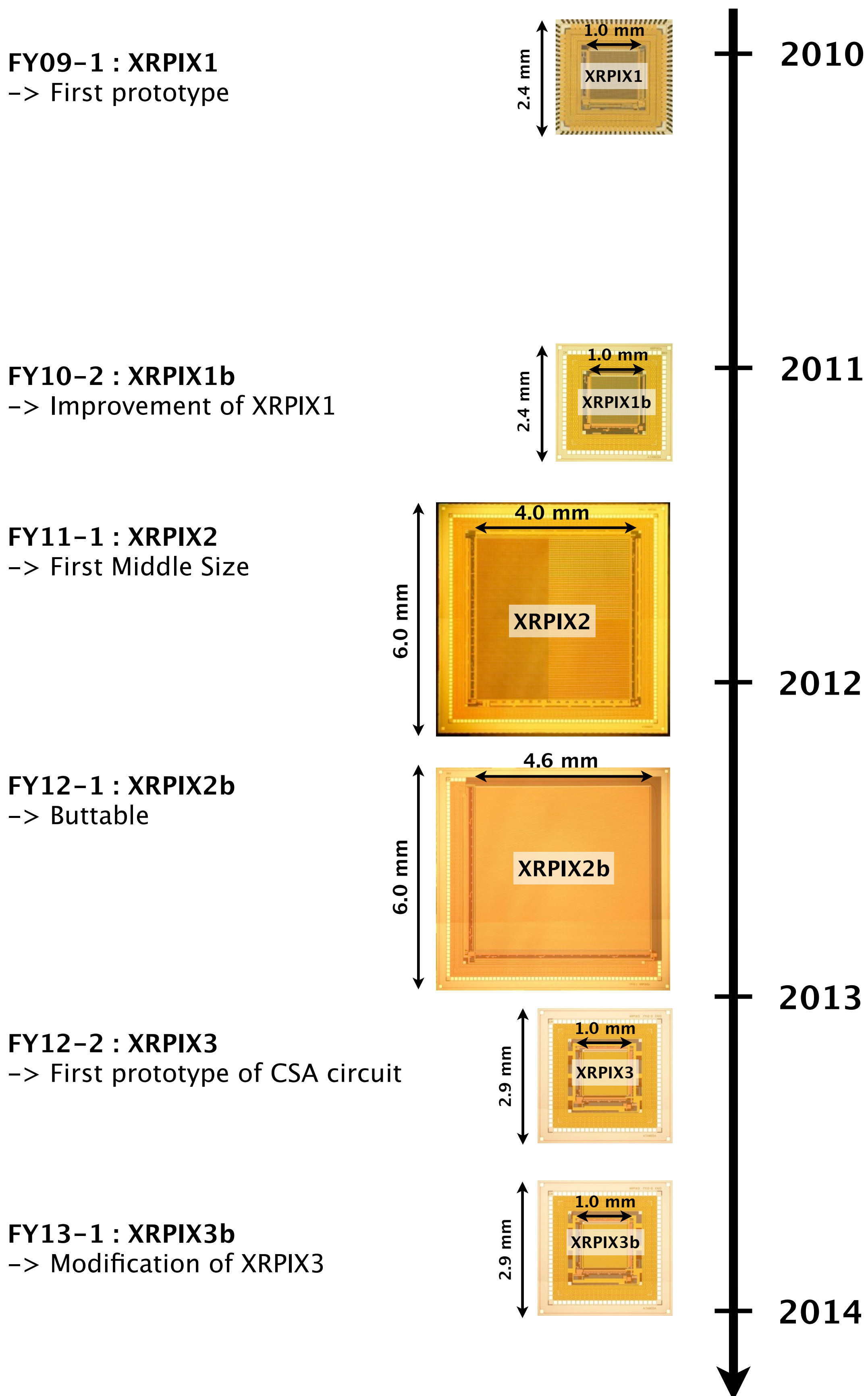

Figure 4.2: XRPIX series history.

have the same basic circuit, but uses different types of transistors (body-floating, body-tie, source-tie) and capacitors (MIM, DMOS). As a result of evaluation [1], subsequent versions decided to use body-tie transistor and MIM capacitance which showed best performance within the 4 TEGs. Although the response of X-rays has been verified, the gain was low and the spectroscopic performance was not high. The following version was designed in order to improve these. The comparator circuit works good by XRPIX1.

4.2.3 XRPIX1b

XRPIX1b is a second prototype of XRPIX series. It was designed in order to improve spectroscopic performance and obtain X-ray spectra by Event-Driven readout mode. And it was fabricated in 2011, 6th MPW run of 0.2 μm SOI pixel process (FY10-2). XRPIX series has been designed by myself from this version. The basic specification is the same as XRPIX1, i.e., it is 2.4 mm $\times$ 2.4 mm in size and consists of 32 $\times$ 32 pixels. The pixel size is 30.6 μm $\times$ 30.6 μm, so the effective sensing area is approximately 1.0 mm $\times$ 1.0 mm. It has 4 TEGs by the difference in the size of BPW area and MIM capacitance. As results of evaluation, the gain and the spectroscopic performance of XRPIX1b improved compared with XRPIX1. Moreover, it was also successful to obtain a spectra by Event-Driven readout mode. There are most results in XRPIX series at present, and the paper has been published [2] [3].

4.2.4 XRPIX2

XRPIX2 is a third prototype of XRPIX series. It was designed for dependency on pixel size or structure. Furthermore, it is a first middle size chip. This is a new step of XRPIX series. It was fabricated in 2012, 7th MPW run of 0.2 μm SOI pixel process (FY11-1). It is 6.0 mm $\times$ 6.0 mm in size. The feature of XRPIX2 is having two kinds of pixel sizes. One is the “Small Pixel (SP)” (left side) and pixel size is 30 μm $\times$ 30 μm. It consists of 144 $\times$ 64 pixels, so the effective sensing area is approximately 4.3 mm $\times$ 1.9 mm. The design of the pixel which showed the best performance in XRPIX1b as a reference was adopted for pixel circuit and structure. Another is the “Large Pixel (LP)” (right side) and pixel size is 60 μm $\times$ 60 μm. This was designed in order to evaluate expansion of the 1 pixel area by circuit size increasing in the future. It consists of 72 $\times$ 36 pixels, so the effective sensing area is approximately 4.3 mm $\times$ 2.1 mm. Therefore, the total effective sensing area

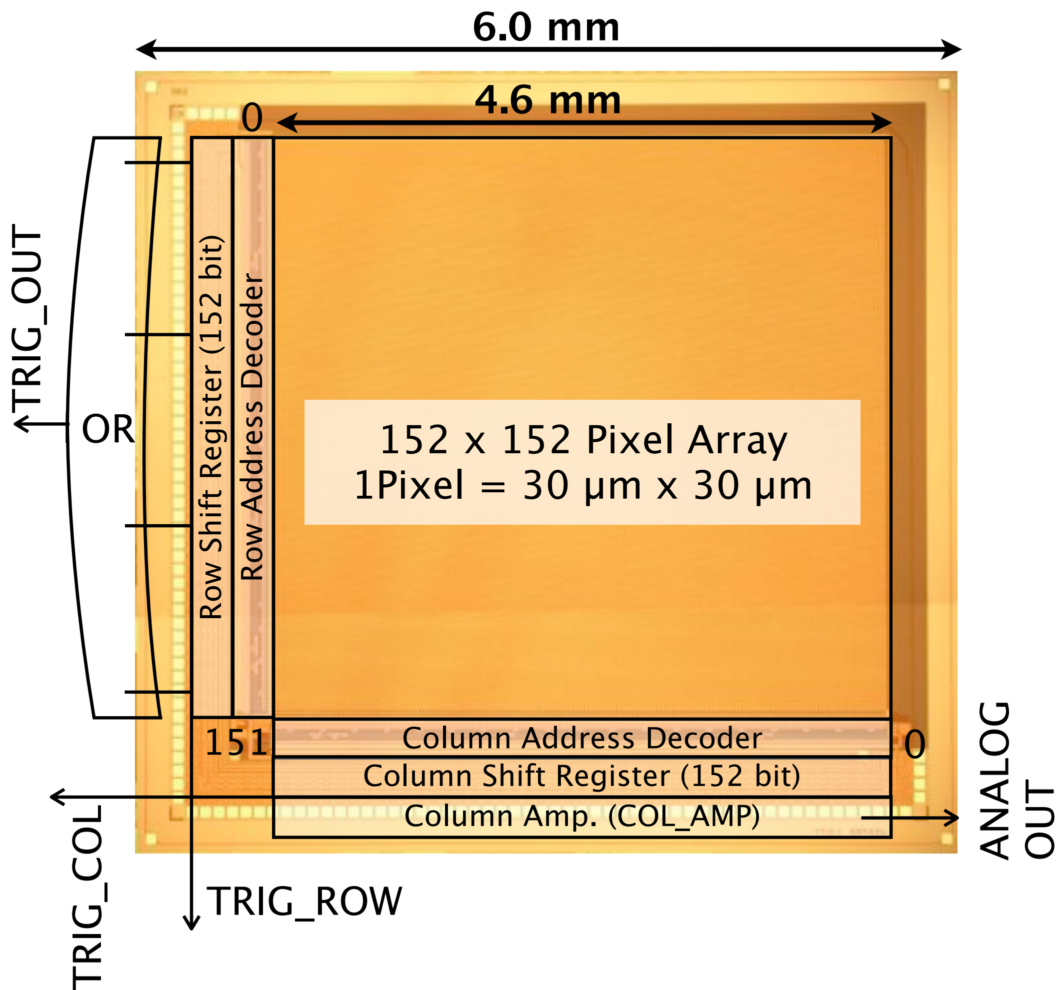

Figure 4.3: XRPIX2b chip photograph and block diagram.

is approximately 4.3 mm × 4.0 mm. Moreover, LP consists of three pixel types, "Large Pixel 1 (LP1)", "Large Pixel 2 (LP2)", and "Large Pixel 3 (LP3)". This is for studying about charge collection efficiency. The LP1 is the same as the layout of SP, and enlarges it, i.e., it is single-via. The LP2 is the pixel structure which formed 3 × 3 multi-via with LP1. Finally, LP3 is the pixel design which adjusted other parameters. The result of XRPIX2 is published [4].

4.2.5 XRPIX2b

XRPIX2b is a fourth prototype of XRPIX series. It was designed for the conclusion to XRPIX2, i.e., it constitutes a middle size chip only from a pixel which showed the best performance. Furthermore, it is also a prototype chip of the "buttable" which puts four devices and makes tiling structure. It was fabricated in 2012, 8th MPW run of 0.2 μm SOI

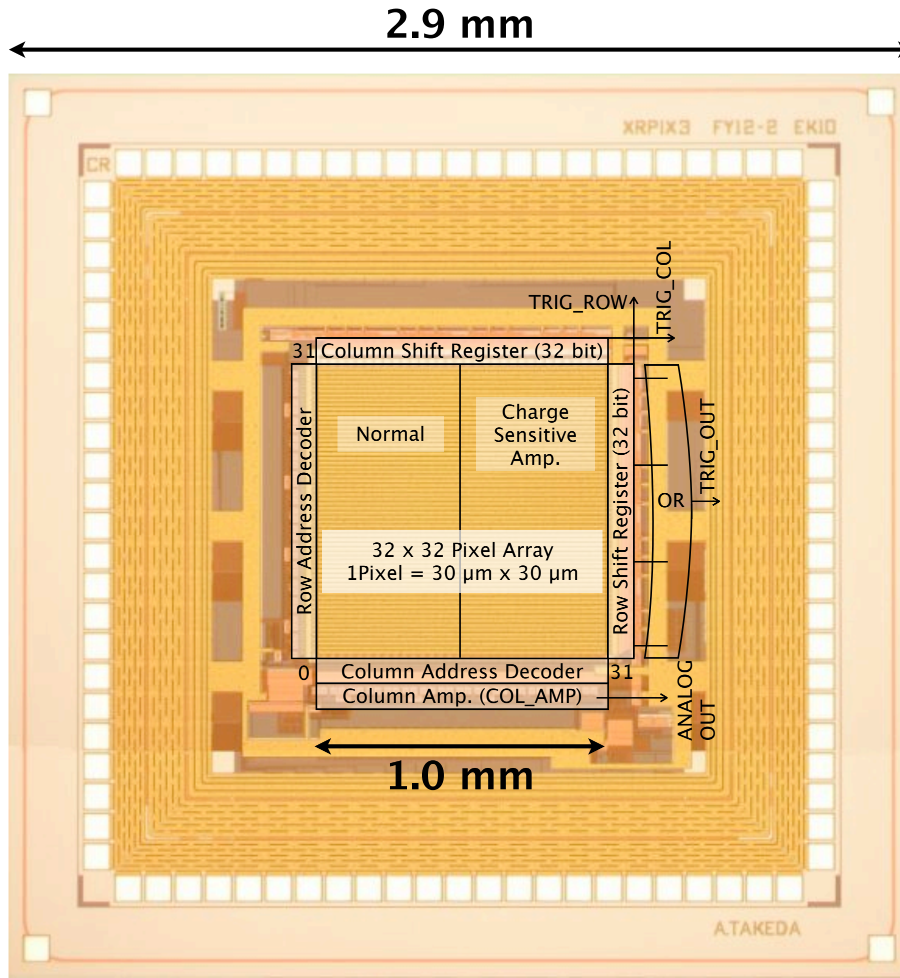

Figure 4.4: XRPIX3 chip photograph and block diagram. The left side is a circuit of "Normal" pixel which was used until now as a reference. On the other hand, the right side is a circuit of the "CSA" pixel tried newly this time.

pixel process (FY12-1). It is 6.0 mm × 6.0 mm in size and consists of 152 × 152 pixels. However, it makes 8 pixels the dummy pixel from the edge with peripheral circuitry. Thus, it consists of 144 × 144 pixels, and the effective sensing area is approximately 4.3 mm × 4.3 mm. Figure 4.3 is a photograph of XRPIX2b and block diagram. By XRPIX2b, Event-Driven of middle size chip was realized and the first stage of XRPIX series was completed. This thesis shows focusing on the results of XRPIX2b.

4.2.6 XRPIX3

XRPIX3 is a fifth prototype of XRPIX series. It was designed in order to improve spectroscopic performance as a next step. It was fabricated in 2013, 9th MPW run of 0.2 μm SOI pixel process (FY12-2). It is 2.9 mm × 2.9 mm in size and consists of 32 × 32 pixels. The

pixel size is 30 μm $\times$ 30 μm, so the effective sensing area is approximately 1.0 mm $\times$ 1.0 mm. It has 2 TEGs by the difference in a circuit. One is the "Normal Pixel" of the same circuit as former as a reference. Another is the "CSA Pixel" of the pixel which has charge sensitive amplifier (CSA) in each pixel in order to increase the gain and improve energy resolution. The sensor format and block diagram are shown in Figure 4.4. The pixel circuit with CSA works good and improved energy resolution successfully. This thesis also shows results of XRPIX3.

4.2.7 XRPIX3b

XRPIX3b is a sixth prototype of XRPIX series. And it was fabricated in 2013, 10th MPW run of 0.2 μm SOI pixel process (FY13-1). XRPIX3 succeeded in obtaining a new result. However, it had restriction of the condition (e.g., Back bias voltage applied only 5 V) by layout mistake. Thus, XRPIX3b was re-designed as a modification version of XRPIX3. It is under evaluation.

4.2.8 Specification Summary of XRPIX Series

Thus, XRPIX series has optimized a pixel circuit and a pixel structure in order to improve performance. The Table 4.1 summarizes the history of the specification by the present.

Table 4.1: Specification Summary of XRPIX Series

	XRPIX1 (FY09-1)	XRPIX1b (FY10-2)	XRPIX2 (FY11-1)		XRPIX2b (FY12-1)	XRPIX3 (FY12-2)	XRPIX3b (FY13-1)
Chip Size (mm × mm)	2.4 × 2.4	2.4 × 2.4	6.0 × 6.0		6.0 × 6.0	2.9 × 2.9	2.9 × 2.9
Effective Area (mm × mm)	1.0 × 1.0	1.0 × 1.0	4.3 × 4.0		4.3 × 4.3	1.0 × 1.0	1.0 × 1.0
Pixel Size (μm × μm)	30.6 × 30.6	30.6 × 30.6	30 × 30	60 × 60	30 × 30	30 × 30	30 × 30
BPW Size (μm × μm)	20.9 × 20.9	20.9 × 20.9 14.0 × 14.0	14.0 × 14.0	14.0 × 14.0 9.0 × 9.0 (+ 4.0 × 4.0, 8 sets)	12.0 × 12.0	14.0 × 14.0	14.0 × 14.0
Number of Pixel	32 × 32	32 × 32	144 × 64	72 × 36	144 × 144	32 × 32	32 × 32
Number of TEG	4	4	1 (SP)	3 (LP1 ∼ LP3)	1	2	2

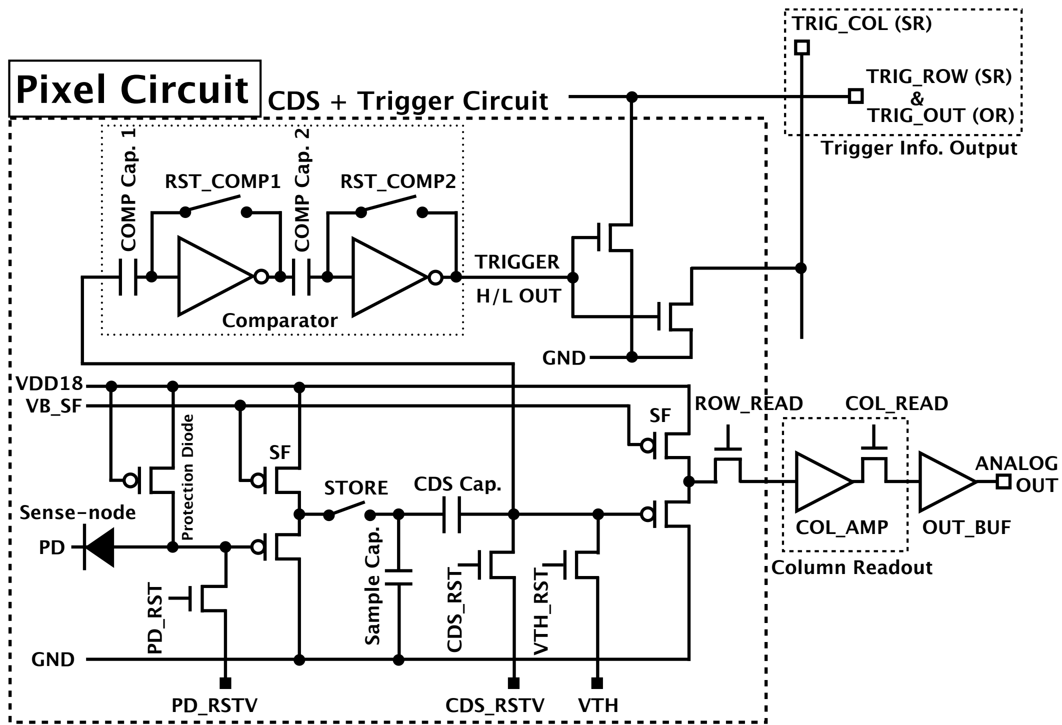

Figure 4.5: Pixel circuit of the XRPIX2b. The comparator for trigger detection is an inverter-chopper type.

4.3 Design of XRPIX

4.3.1 Pixel Circuit

The pixel circuitry and layout of XRPIX2b are shown in Figure 4.5 and Figure 4.7, respectively. The pixel circuitry can be divided into two main parts: the signal processing part, containing the correlated double sampling (CDS) circuit, and the trigger part. The CDS circuit suppresses the kTC reset noise in the sense-node and subtracts the offset levels.

The trigger circuit generates a trigger signal when an X-ray signal crosses the threshold voltage (VTH) of the pixel. This function is realized by two inverter-chopper type comparators. The reason for using two inverter stages is for raising detection sensitivity. This comparator contains a cascade of inverter stages which is essentially a bistable multivibrator [5].

XRPIX3 has CSA circuit in each pixel. Figure 4.6 is the CSA Pixel circuit of XRPIX3. The Normal Pixel circuit is the same as XRPIX2b (i.e., Figure 4.5). The Normal and the CSA pixels have different circuit configuration of preceding stage. The Normal circuit consists of source follower (SF) by common-drain of a PMOS transistor. The CSA circuit

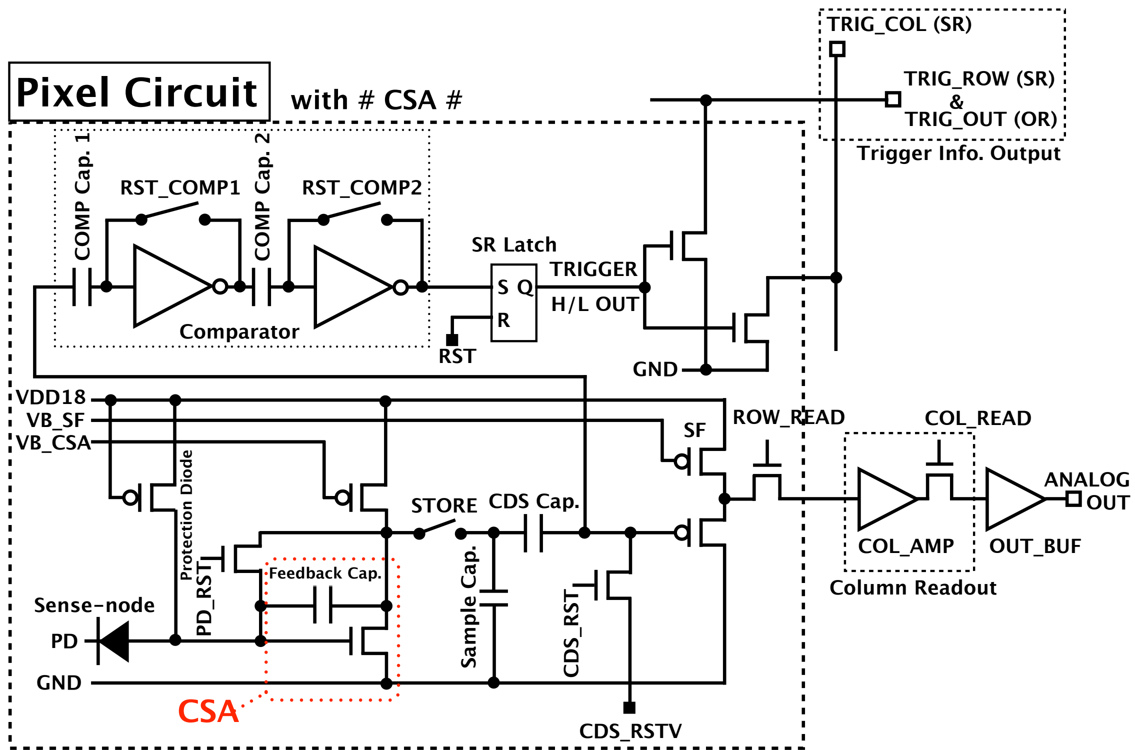

Figure 4.6: Pixel circuit of the XRPIX3/3b. CSA circuit was added newly. Furthermore, simple Set-Reset Latch was also added to the output latter part of the comparator circuit.

consists of pre-amplifier by common-source of a NMOS transistor and a feedback capacitance (1 fF). The gain of output signal is designed about 10 times (50 μV/e−) as compared with the previous detector. The CSA circuit improves the S/N ratio to the circuit noise in the following stages. Furthermore, XRPIX3 also has Set-Reset (SR) latch in order to stabilize the logic output of a comparator.

4.3.2 Peripheral Circuit

The peripheral circuit other than a pixel is important in order to control XRPIX. For example, the input/output (IO) buffer circuit for connecting the inside and outside of a chip, the address decoder for selecting the pixel, the output buffer amplifier circuit of a column or analog signal, the bias generation circuit to each circuit, the shift register for storing the information on a hit-pattern or a bad pixel mask, and so on. Furthermore, XRPIX3 has an encoder which converts from hit-pattern into address. This circuit has the function to judge the easy pattern whether two or more bits have a hit.

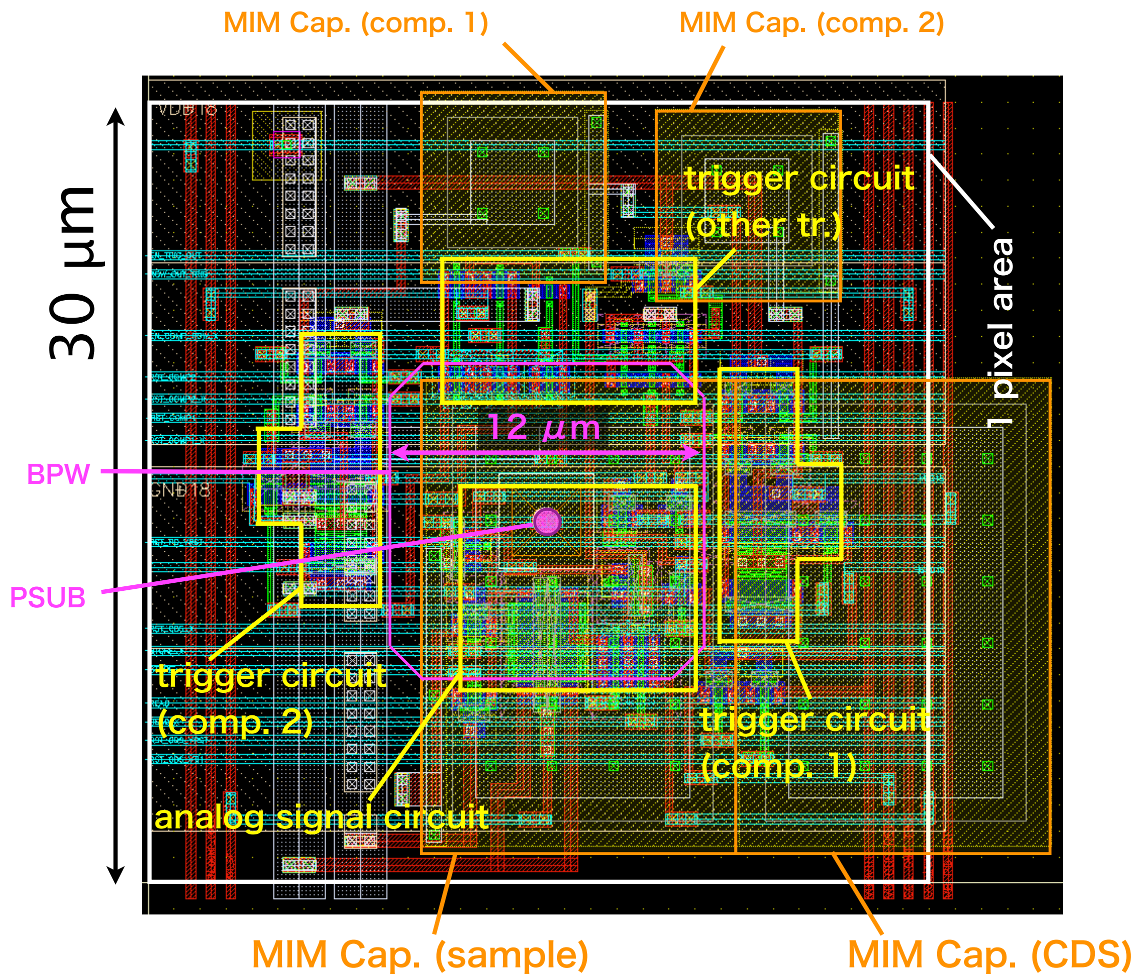

Figure 4.7: Pixel layout of the XRPIX2b.

4.4 Operation Architecture

4.4.1 Pixel Circuit

The trigger operation consists of a resetting phase and a waiting phase. The timing diagram of the trigger circuit is shown in Figure 4.8. In the resetting phase, the threshold voltage is connected to the input of the trigger circuit by asserting a VTH_RST signal and stored in the capacitors (COMP Cap.1 and COMP Cap.2) by turning on and off the reset switches (RST_COMP1 and RST_COMP2) in series. Then, the VTH level is set at the input-node of the comparator. After releasing the reset signal of the sense-node (PD_RST), the input-node level of the comparator moves down to the level corresponding to the CDS_RST to allow some room for the noise not to trigger the comparator. And then, the waiting phase begins, during which the trigger output signal is asserted when the voltage at the sense-node exceeds the threshold voltage by X-ray signal.

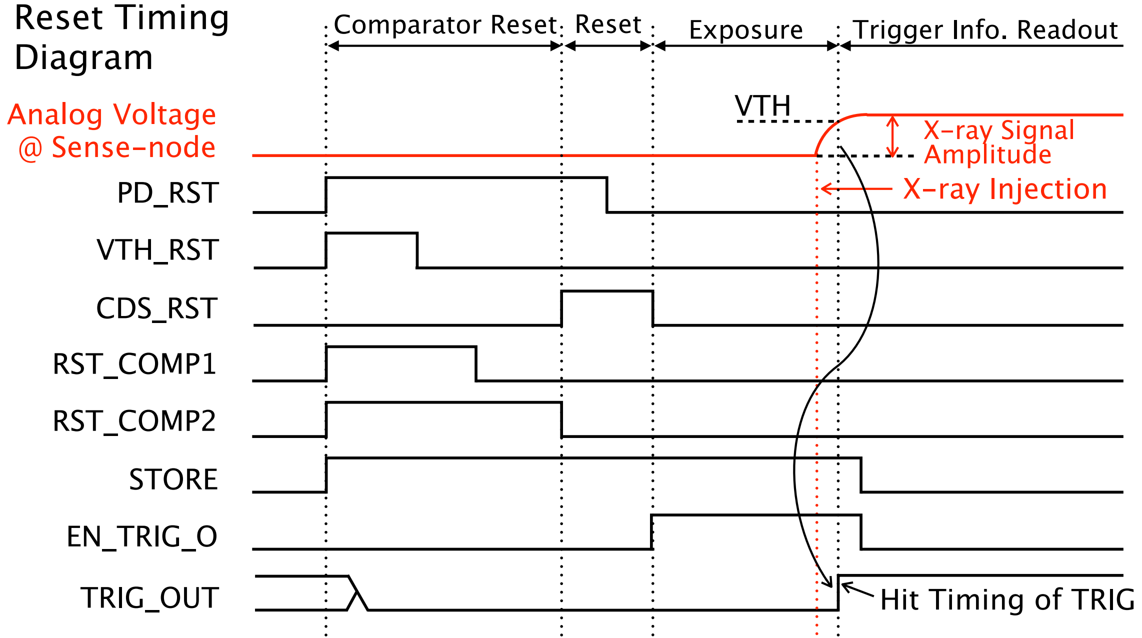

Figure 4.8: Pixel operation timing diagram.

The trigger output signal from a pixel is wired-OR'ed in the row and column directions and stored in shift registers at the edges of the sensor array. The 152 wired-OR'ed row signals are then OR'ed again, and the final trigger signal is fed to the output by the sensor. After receiving the trigger output signal with an external circuit, the store switch (STORE) is turned off. The X and Y addresses of the hit pixel are available from the row and column shift registers.

4.4.2 Trigger Circuit

We have designed an intelligent readout mode driven by the pixel trigger. Figure 4.9 and Figure 4.10 show the flow chart and the overall timing diagram of the signals controlled by the USER FPGA, respectively.

As shown in Figure 4.9, when an X-ray signal is detected by a pixel (i.e., a hit pixel, (i)), the comparator output of the hit pixel (ii) and TRIG_OUT of the 152 wired-OR'ed in row (iii) become high. Thus, USER FPGA is notified of the arrival of an X-ray and reads the hit pattern information from the row and column shift registers (iv). Thereafter, the USER FPGA accesses the hit pixel directly (v) and reads out the analog voltages (signal and pedestal levels) using the ADC (vi). Finally, the obtained digital data is transmitted to the DAQ-PC (vii); this is called the "Trigger Assert" state. The system is reset periodically

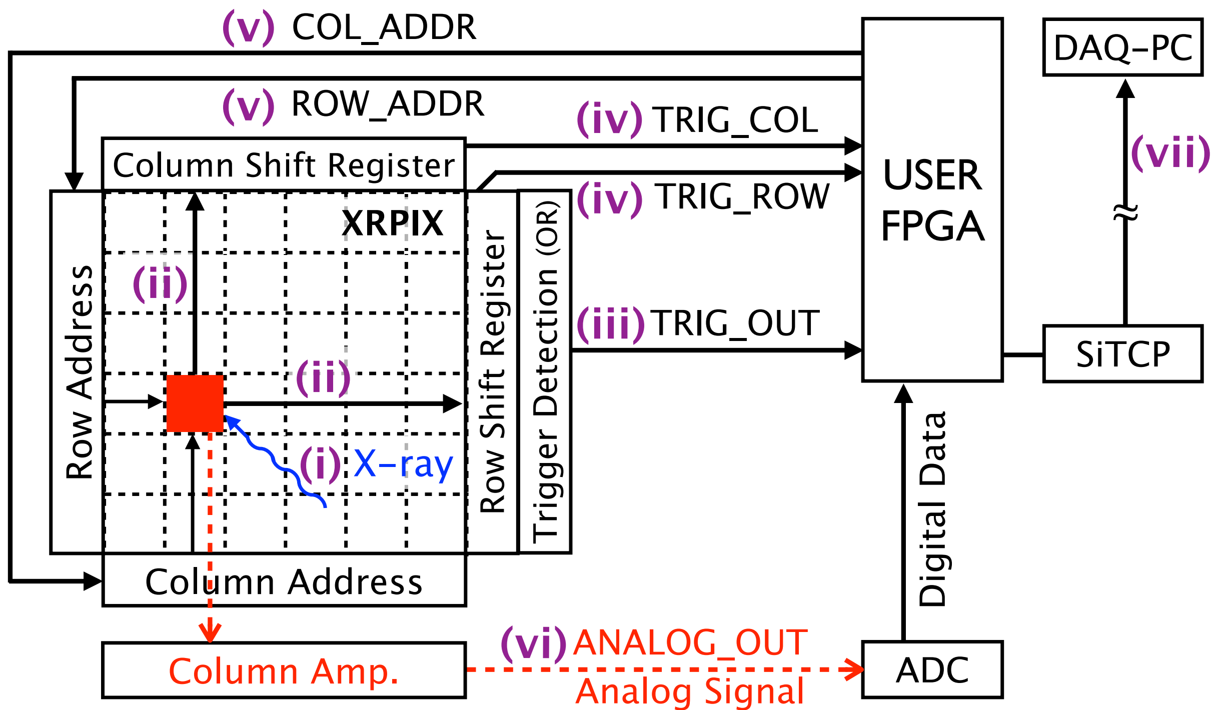

Figure 4.9: Flow of the event-driven readout. The solid / dashed arrows show digital / analog signals, respectively.

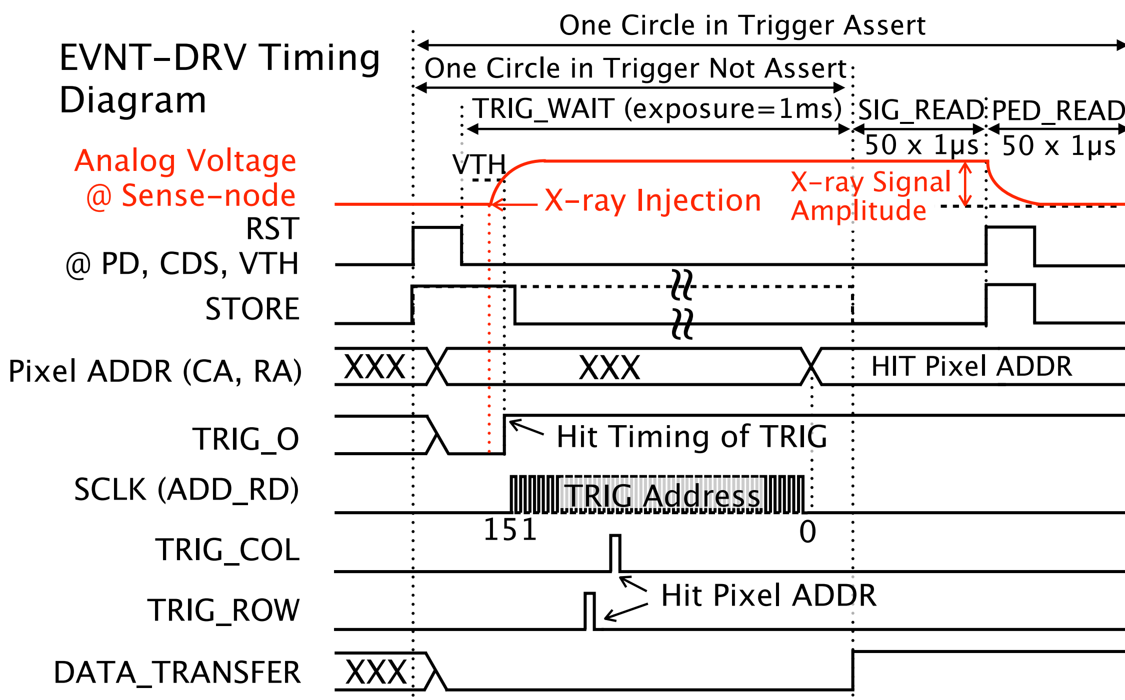

Figure 4.10: Timing diagram of XRPIX2b in event-driven readout mode. The solid line shows the case of trigger assertion, and the dashed line shows the case of no trigger assertion.

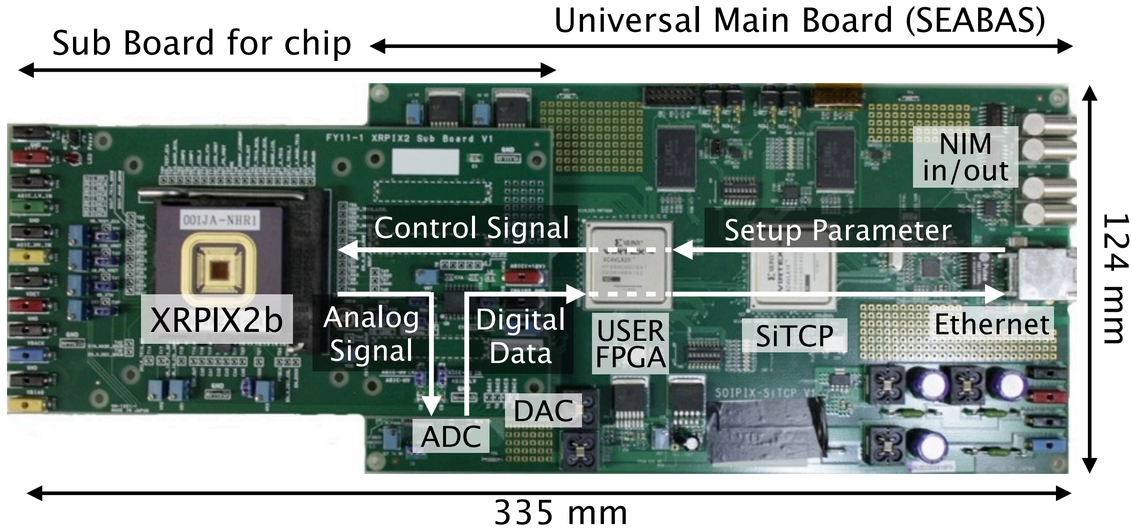

Figure 4.11: General data acquisition system for SOI detectors, "SEABAS".

if no X-ray is detected (i.e., the "Trigger Not Assert" state).

Currently, one set of the event data contains a header (2 bytes), an event number (4 bytes), a hit timing (6 bytes), row and column addresses of the hit pixel (2 bytes), pulse height words of the signal (50 samples, 100 bytes), and pedestal levels (50 samples, 100 bytes). The total data size is 214 bytes, and the readout time is about 100 μs. The data is transferred as an 8-bit (byte) unit via 100 Base-T Ethernet.

The X-ray signal amplitude is calculated from the difference between the averages of the signal and the pedestal levels (c.f., Figure 4.10). This over sampling process works as a low-pass filter, reducing white noise and quantization noise.

4.4.3 Bad Pixel Mask and Control Register Writing

XRPIX disable the output information of a comparator by bad pixel writing. The writing line of bad pixel mask has two, RA and CA. Furthermore, there is also a register writing region for detector control in each line. They consist of the shift register and information is written in by giving a clock from the external.

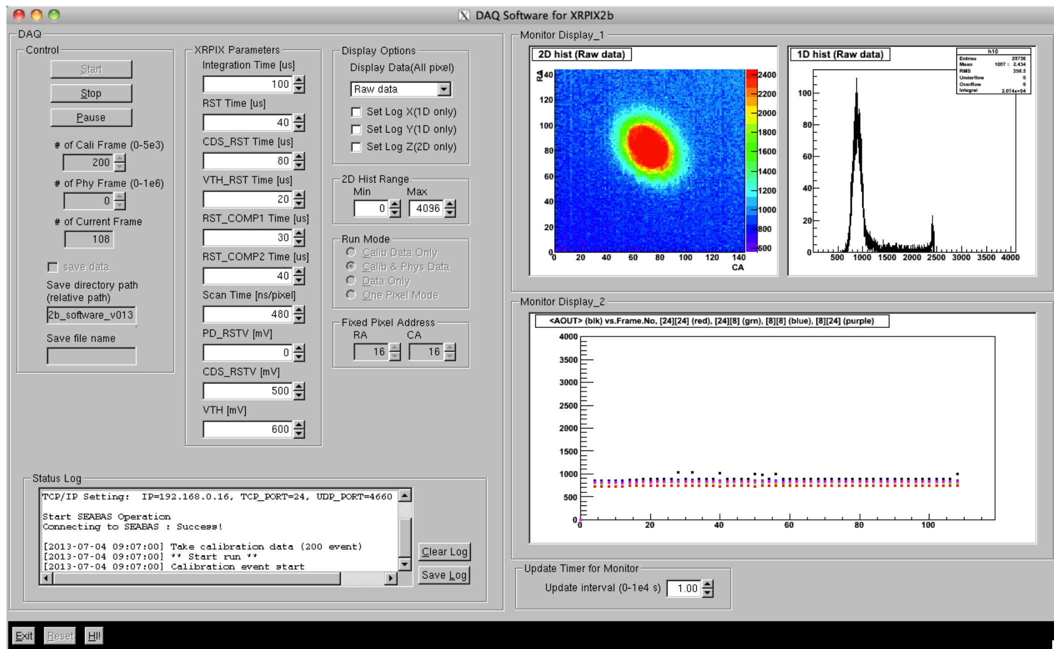

Figure 4.12: Data acquisition software for XRPIX2b. It is based on ROOT GUI. The 2D image is the picture which irradiated with the laser pointer of visible light.

4.5 Data Acquisition System

4.5.1 Hardware

We have developed a compact evaluation system, as shown in Figure 4.11. The system consists of the chip-loaded sub-board and the main board (SEABAS: Soi EvAluation BoArd with Sitcp). The SEABAS contains two FPGAs (Xilinx Virtex-4). One is used for chip control and data taking (called USER FPGA), and the other is used for data transmission via 100 Base-T Ethernet (called SiTCP [6] FPGA). The external clock frequency sent to the USER and the SiTCP FPGAs is 25 MHz; this frequency can be multiplied within the internal PLL circuit. The SEABAS also provides an ADC (1 V / 12 bits) for pulse height digitization, a 4-channel DAC (12 bits / 1.8 V) for producing reference voltages (e.g., PD_RSTV, CDS_RSTV, and VTH in Figure 4.5), 2 inputs and 2 outputs of the NIM signal for communication with external modules, and a power system (±5 V inputs).

4.5.2 Software

DAQ software is graphical user interface (GUI) based on ROOT[2] framework. It also consists of the network programming by C/C++. Each parameter and DAQ mode can be set up from a screen. Those information is transmitted to SEABAS from PC via User Datagram Protocol (UDP). And it writes in the register space secured in FPGA. Furthermore, the acquired data can be displayed on a histogram. Acquisition data is transmitted to PC from SEABAS via Transmission Control Protocol (TCP). The saved data is ROOT form and is analyzed off-line later. The software is built by a network programming. Any language may be used and it is satisfactory also at Character User Interface (CUI).

[2]http://root.cern.ch/

References

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Chapter 5

Evaluation of XRPIX

The XRPIX series has been designed as Chapter 4 described. In this chapter, we show the evaluation result of XRPIX. Evaluation of Event-Driven readout mode is described focusing on XRPIX2b. Furthermore, spectroscopic performance also describes the result of XRPIX3 with a CSA pixel circuit.

5.1 Experiment Setup

The examination of XRPIX2b was done on two locations, KEK and Kyoto University. Here, each experiment setup is described briefly.

5.1.1 Setup of KEK

Figure 5.1 shows the experimental setup of KEK. Thermostatic chamber is “espec SU-661” and it can cool it to -60 °C. Capacity is 400 mm × 400 mm × 400 mm. “KEITHLEY 2410” of sauce meter is used for apply the back bias voltage of a sensor. The regulated DC power supply of “TEXIO PW26-1AT” is used for apply the voltage of SEABAS.

5.1.2 Setup of Kyoto University

Figure 5.2 shows the experimental setup of Kyoto University. Thermostatic chamber is used in a vacuum. A vacuum chamber is a custom-made item. It can cool it to -50 °C. “KEITHLEY 2410” of sauce meter is used for apply the back bias voltage of a sensor. The regulated DC power supply of “KENWOOD PWR36-1” is used for apply the voltage of SEABAS.

Figure 5.1: Experimental setup of KEK.

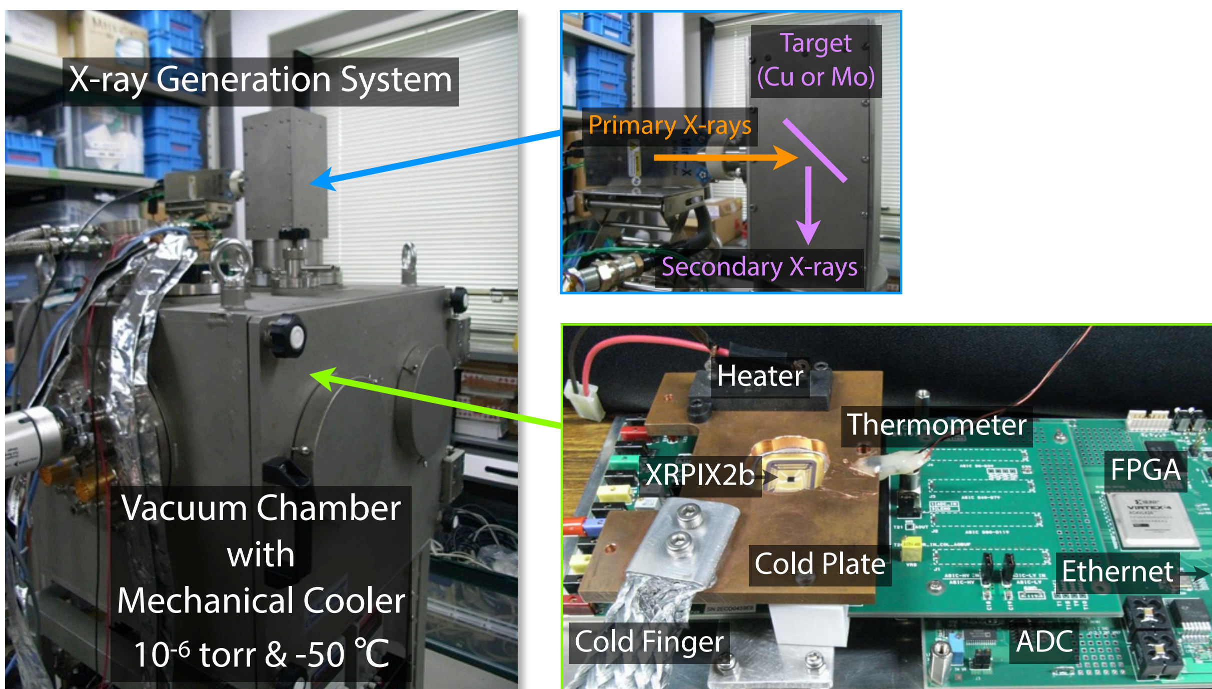


Figure 5.2: Experimental setup of Kyoto University.

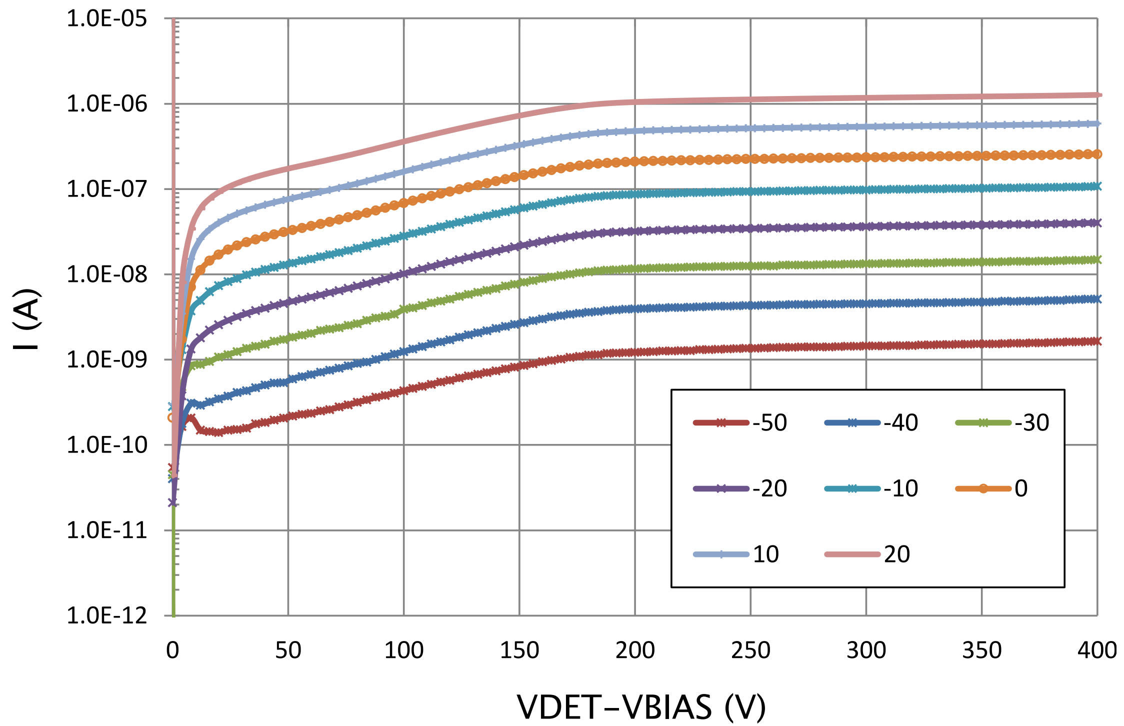


Figure 5.3: I-V measurement of XRPIX2b.

5.2 Diode Characteristic

5.2.1 IV Measurements

In order to evaluate spectroscopic performance, it is important to obtain the information on leakage current. Therefore, the relation of back bias voltage and sensor current of XRPIX2b was measured. The back bias voltage was applied in source meter of KEITHLEY 2636 between n+ (VDET) and p+ (VBIAS) bias rings. Figure 5.3 shows the measurement result of a current value when changing back bias voltage and temperature. The breakdown voltage of a diode disappear less than 400 V. This plot has the inflection point in 180 V. Although it may be because the depletion region arrived at the back side of sensor (i.e. full depleted), it cannot judge only by this result. This conclusion requires another measurement (see Section 5.3). As shown by Figure A.1, there is a chip from which behavior differs on the back bias voltage beyond 200 V. There is an increase in current by more than 250 V. Thus, the variation in the performance by a wafer may be large. The reason is unknown although this has the possibility of the difference in a wafer or in a process of mounting.

Figure 5.4 shows the temperature dependency of the dark current of the pixel part by XRPIX1b. This is a value which is consulted by CZ type SOIPIX.

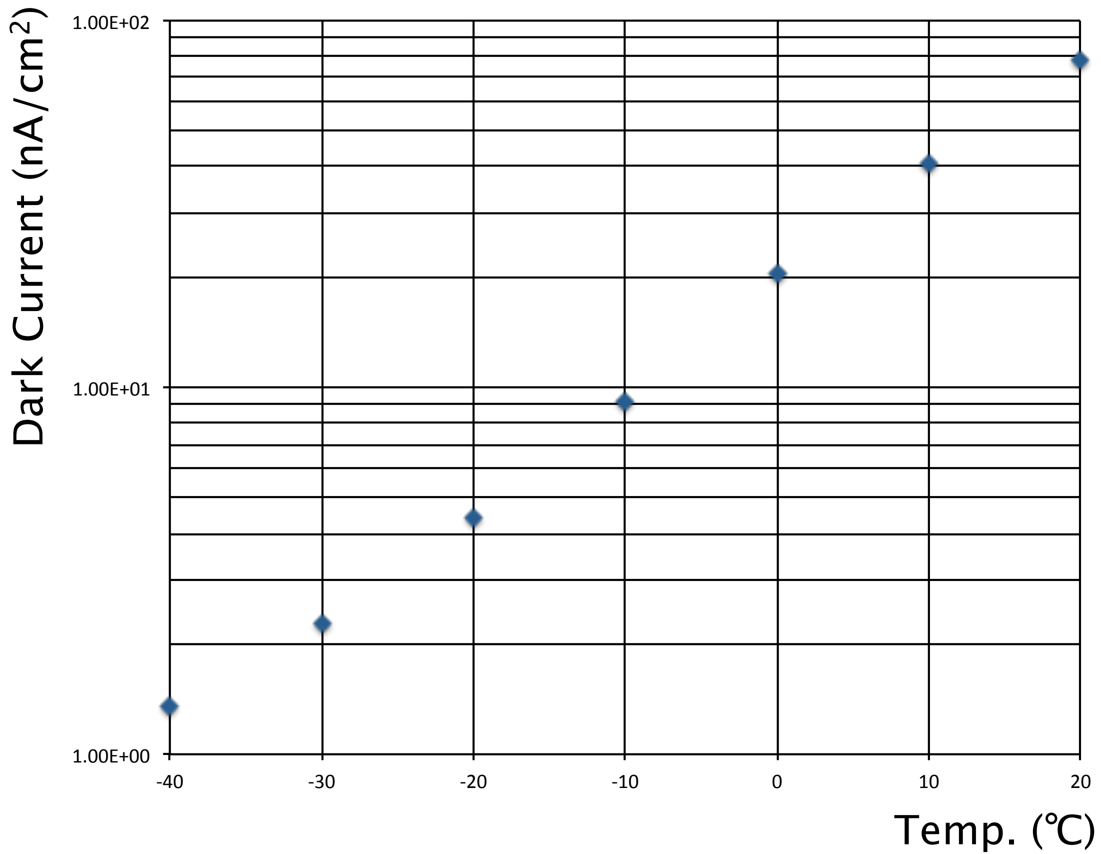


Figure 5.4: Temperature dependency of the dark current of the pixel part by XRPIX1b.

5.2.2 Arrhenius Plot

In Section 5.2.1, I-V measurements was obtained. Furthermore, if the origin of this leakage current is known, the method of reducing it may be found. This is required in order to reduce a noise. Arrhenius plot is known as a method of investigating the origin of leakage current. It is often used to analyze the effect of temperature on the rates of chemical reactions. In the case of a semiconductor, the current I in the temperature T can be experientially written by the following Arrhenius' equations.

$$I = Ae^{-\frac{Ea}{kT}} \tag{5.1}$$

$$ln(I) = ln(A) - Ea\frac{1}{kT} \tag{5.2}$$

Ea is activation energy and k is Boltzmann constant. If the main element of leakage current is diffusion current, Ea is 1.12 eV (i.e. energy gap of Si), and if it is generation current, it is 0.56 eV. Figure 5.5 shows the arrhenius plot using the result of the Section 5.2.1. Its horizontal axis is for the $1/kT$, and the vertical for the current. As shown in the Formula 5.1,

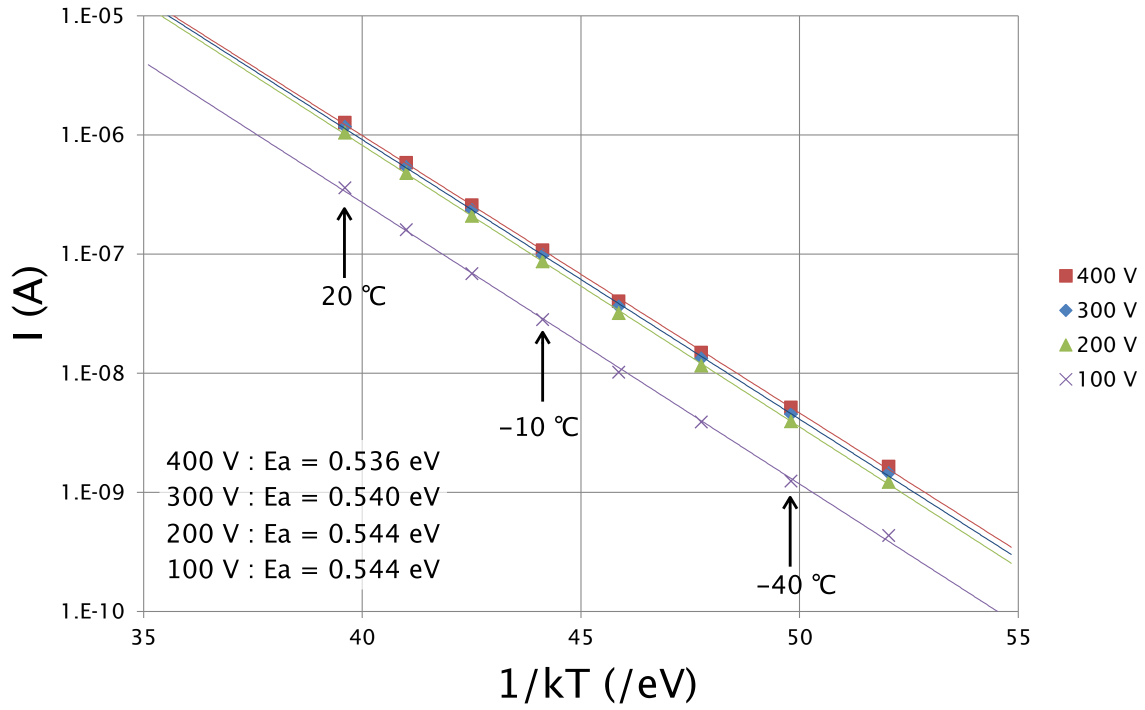


Figure 5.5: Arrhenius plot of XRPIX2b.

the index which fitted the plot by exponential corresponds to activation energy. From a fitted result, when back bias voltage is less than 250 V, activation energy is about 0.56 eV. Thus, it is thought that the leakage current of XRPIX2b has dominant generation current.

5.3 CV Measurements

As the Section 2.1.2 described, a depletion region grows with the voltage applied to a sensor layer. It continues spreading until it arrives at the back side of sensor layer, i.e., the capacitance by depletion region increases until it reaches fully-depleted voltage. Therefore, this voltage can be obtained by C-V measurement described with the Section 2.1.2. Since back bias voltage and $1/C^2$ are proportionality relation as the Formula (2.7) showed, a plot becomes linearly. And the voltage at which an increase stops is fully-depleted voltage. Figure 5.6 is the C-V measurement result of XRPIX2b. Its horizontal axis is for the back bias voltage, and the vertical for the $1/C^2$. The fully-depleted voltage obtained from this plot is about 180 V. The inflection point of 180 V shown in the Figure 5.3 was fully-depleted voltage.

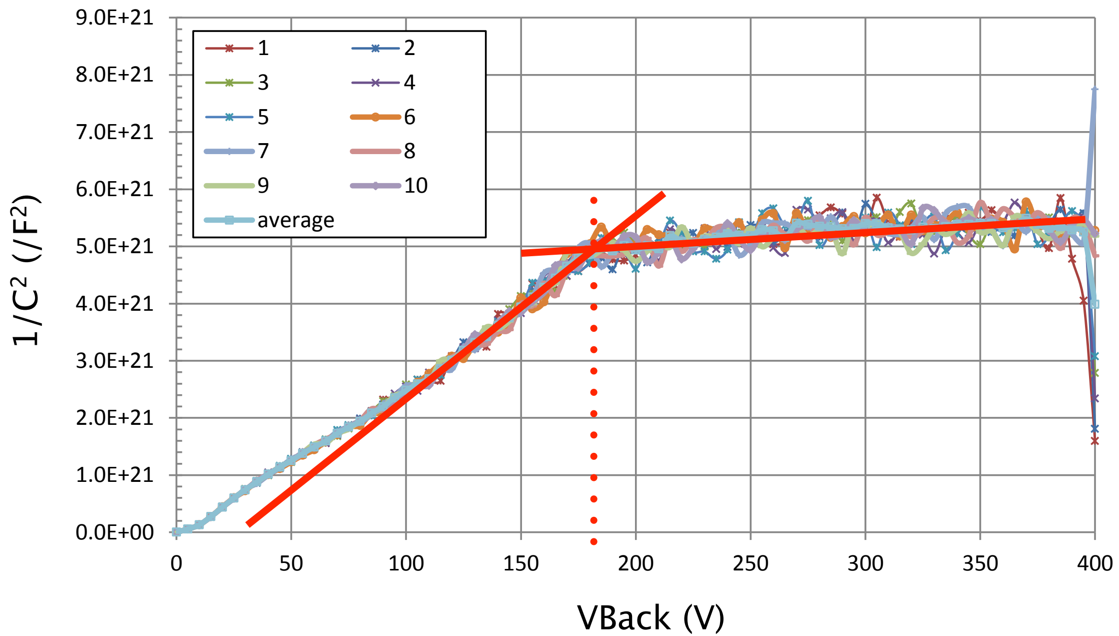


Figure 5.6: The CV measurement of XRPIX2b. The fully-depleted voltage obtained from this plot is about 180 V.

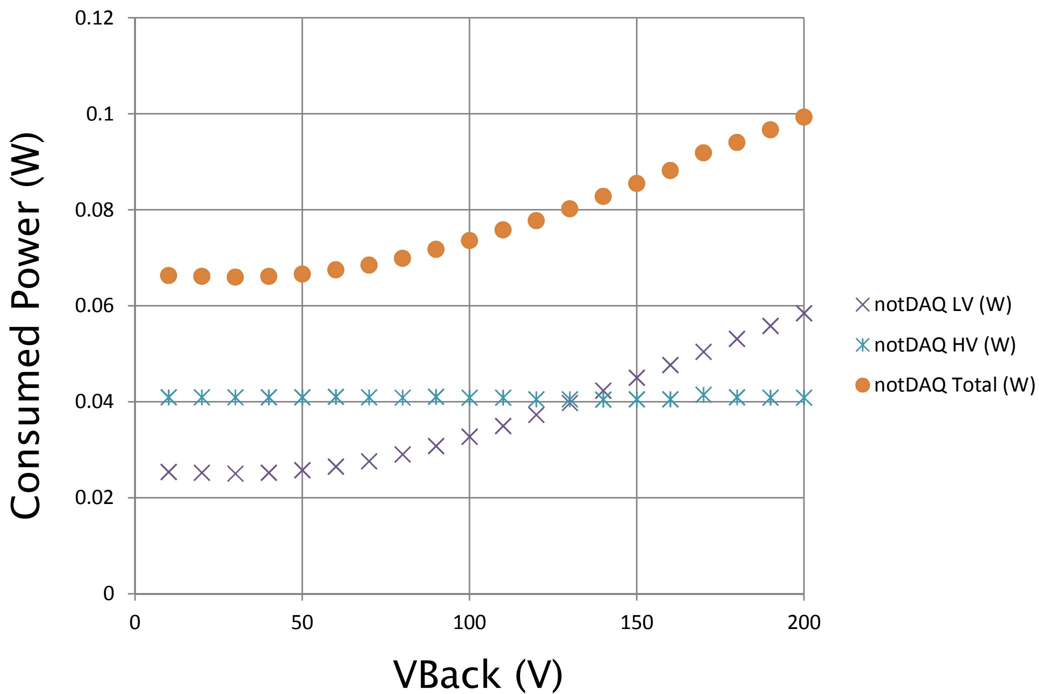


Figure 5.7: Consumed power measurement of XRPIX2.

5.4 Consumed Power

Measurement of consumed power is important for the detector operated under cooling. XRPIX2b consists of three kinds of power supply lines, 1.8 V, 3.3 V, and a sense-node apply voltage. Since sense-node apply voltage is less than 200 nW ($\leq$ 1 nA @ 200 V /

-50 °C) also in it, there is little influence. Therefore, the consumed power of 1.8 V and 3.3 V were measured. The consumed power was measured in the state of stopping DAQ, i.e., reset state. This is for a source follower circuit by common-drain of a PMOS transistor consuming current most in a reset state. However, it became clear that XRPIX2b could not measure consumed power correctly by the mistake of a layout design from the result of measurement. Thus, XRPIX2 which is the same chip size (6 mm sq.) was measured instead of it. The measurement result about XRPIX2b was shown in the Section A.2.

Figure 5.7 shows the plot of the measurement result of consumed power. The 3.3 V supply line (HV) is not dependent on back bias voltage and is constant at 40 mW. This shows that there is no influence of back gate effect. However, the 1.8 V supply line (LV) has the increase in consumed power on the back bias voltage beyond 100 V. This is dependent on a pixel design and considered to have back gate effect. XRPIX2/2b designed BPW region as small as possible, unless trouble appears in operation. This condition was obtained by the simulation of Technology CAD (TCAD). If a transistor is arranged within 6 μm from the end of BPW region when back bias voltage is 100 V, there will be no big problem in operation. Obviously, this has restrictions and is not the best method. However, in order to improve spectroscopic performance, the gain needed to be increased and it was unavoidable. This problem is avoided by preventing the back gate effect using D-SOI wafer in the future. As a result, the consumed power of XRPIX2 is 100 mW at 200 V. This is very small compared with a readout board (i.e., SEABAS).

5.5 Circuit Gain

The obtained signal voltage is outputted through readout circuit. Thus, it is necessary to get to know a circuit gain in order to estimate output signal voltage from the X-rays energy. The analog signal circuit of XRPIX2b consists of source follower, column output buffer, and analog output buffer. In an ideal, these output gain is 1. However, actual operation becomes lower than 1. Therefore, the circuit gain needs to measure. Furthermore, an output signal can be corrected by measuring the variation in the circuit gain for every pixel.

The gain was obtained from the relation between the input voltage to a pixel circuit, and output voltage. Constant voltage was inputted from CDS_RSTV and output voltage from this pixel circuit was measured (Figure 5.8). Figure 5.9 shows example of circuit gain measurement at 20 °C. It has offset because of fixed voltage is added in source follower

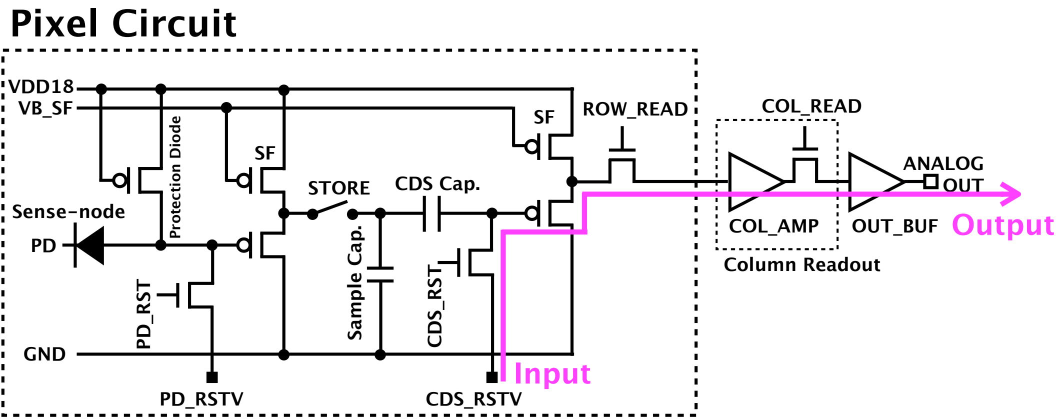


Figure 5.8: The measurement course of circuit gain. The comparator circuit is omitting. Constant voltage was inputted from CDS_RSTV and output voltage was measured.

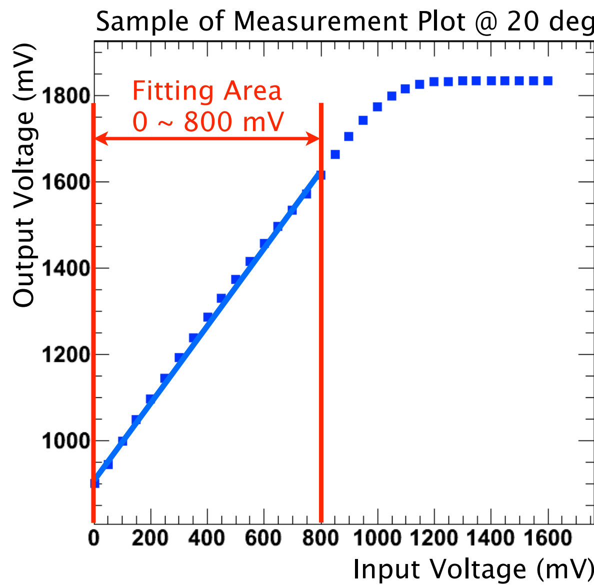


Figure 5.9: Example of circuit gain measurement at 20 °C.

circuit. The circuit gain was obtained by the slope of the linear fitting from 0 to 800 mV. Figure 5.10 shows the measurement result of the circuit gain of all the pixels. The Mean of a circuit gain is 0.95 (σ = 0.5 %) from the result of 1D histogram.

5.6 XRPIX2b Operation

5.6.1 Observing of Analog Waveform

When operating a detector, an important thing is observing analog signal waveform at first. In particular, the parameter of a control signal can be determined by obtaining DC characteristic. This is because it is necessary to check the influence by expansion of a chip

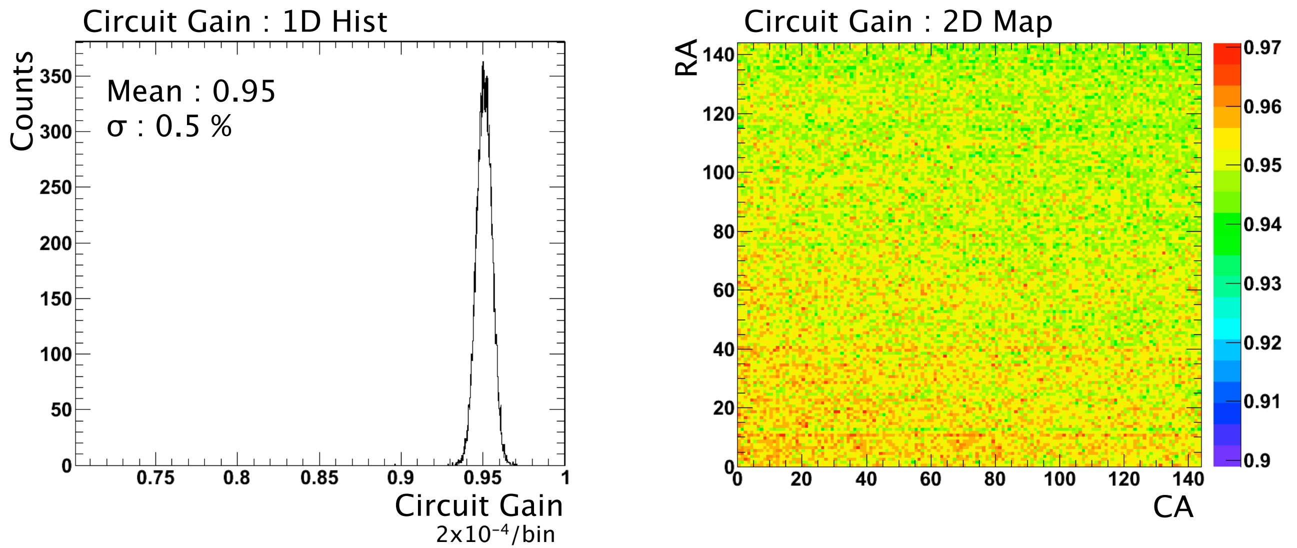


Figure 5.10: Results of circuit gain measurements (all pixels). The left figure is 1D histogram of all the pixel gains. The right figure is 2D map of it.

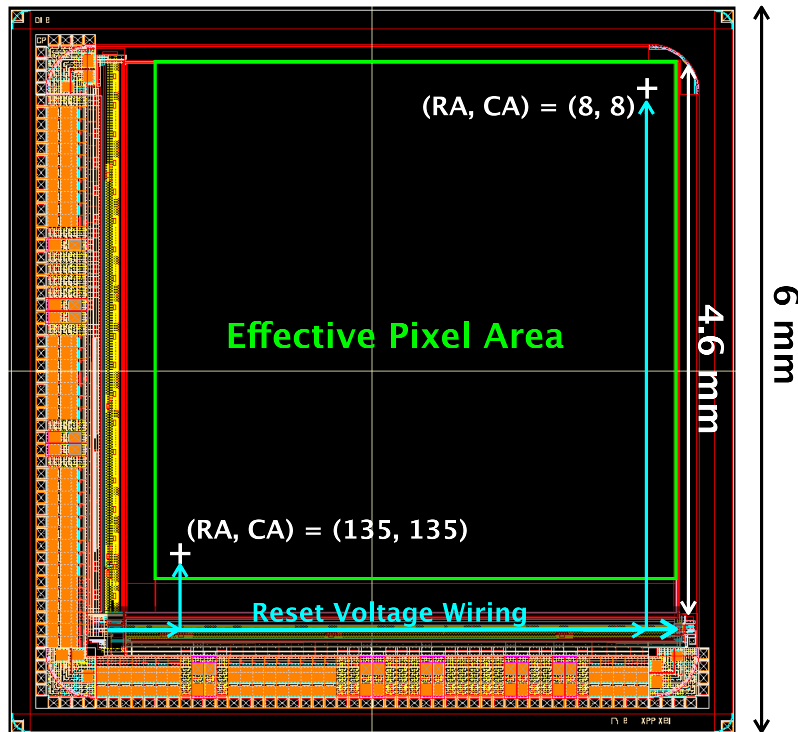
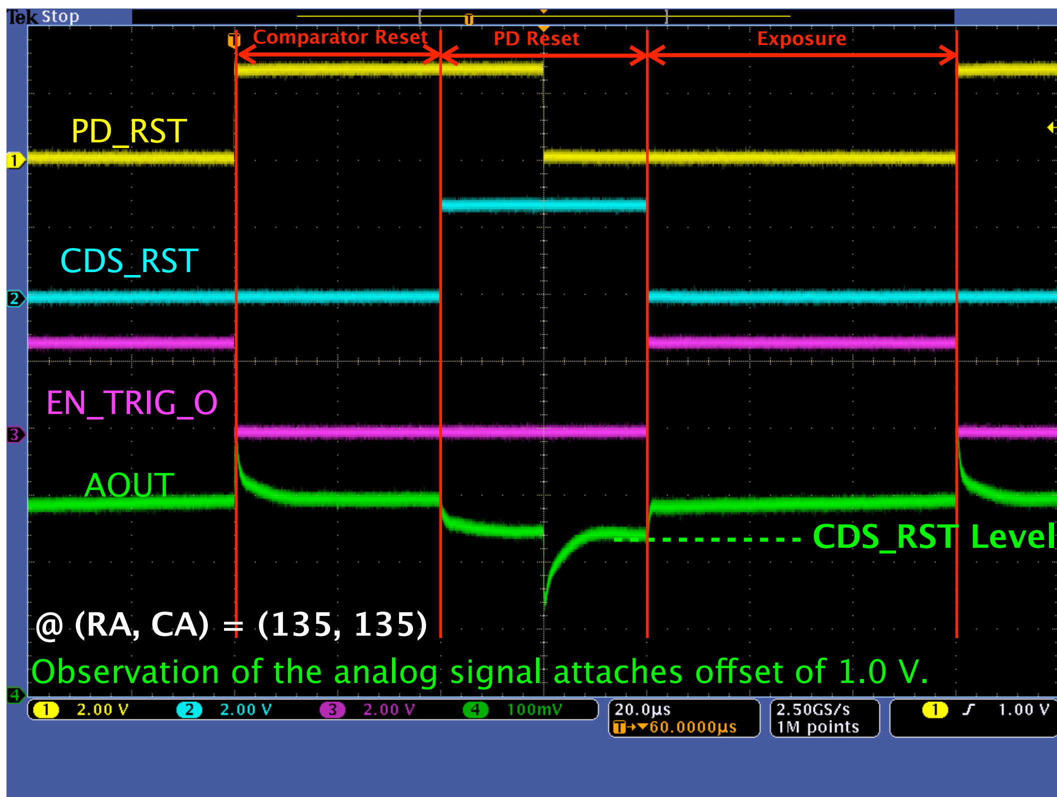


Figure 5.11: The position on the observed chip of two points ((RA, CA) = (8, 8), (135, 135)). The reset voltage is inputted from left(-bottom) side. Therefore, right(-bottom) interconnection resistance becomes large. Furthermore, since reset voltage is wired for each column, top side interconnection resistance is large.

area (i.e., interconnection resistance and parasitic capacitance).

In order to check the difference by a pixel position, two extreme points are compared. This time, two points, (RA, CA) = (8, 8) and (RA, CA) = (135, 135), were selected (Figure 5.11). That is, interconnection resistance of (8, 8) is large and (135, 135) is small.



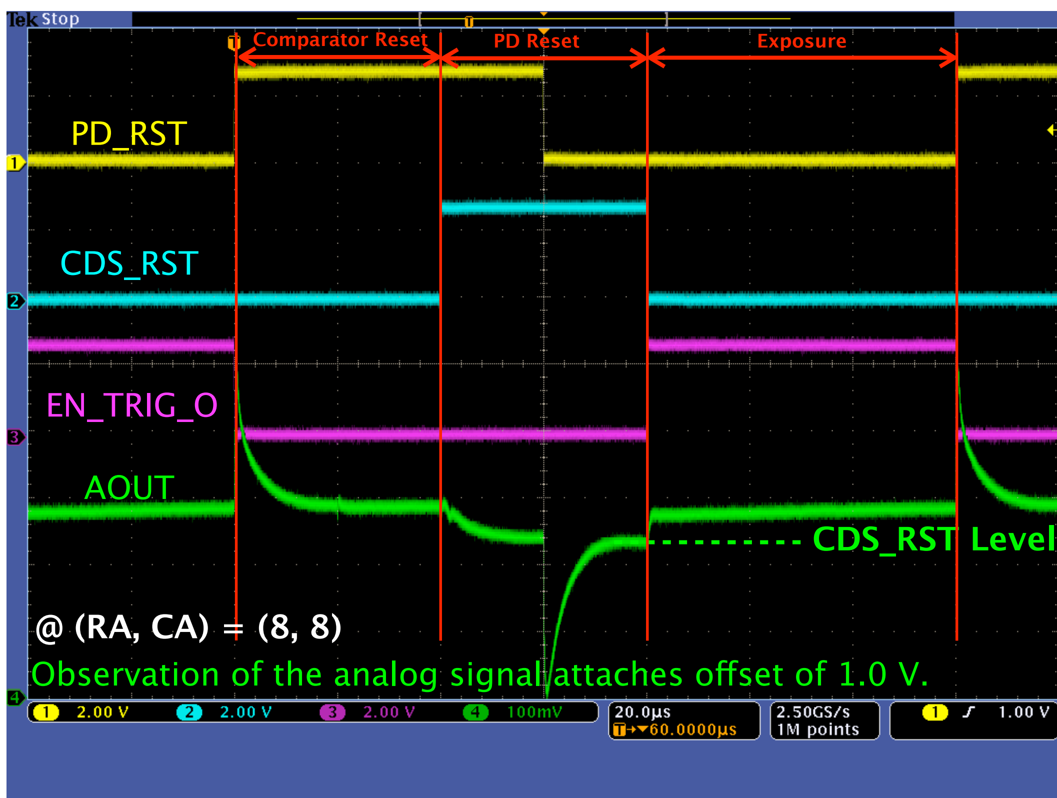


Figure 5.12: Obtain waveform of pixel operation with the oscilloscope.

Figure 5.12 is a typical waveform of two points of the pixel operation obtained with the oscilloscope. The control signal shows PD_RST, CDS_RST, and EN_TRIG_O as a representative. This timing diagram was shown by Figure 4.8 of the Chapter 4.

The waveform shows that PD_RST signal has affected the analog signal (AOUT) greatly. This shows that it has parasitic capacitance by these signals (i.e., crosstalk). Moreover, the influence of a crosstalk has (8, 8) larger than (135, 135). This shows the influence of interconnection resistance of the reset voltage. Therefore, in XRPIX2b, time is required about 10 μs for an analog signal to be stabilized by change of a control signal. This is because the chip area became large (A small chip like XRPIX1b is short time in about 1 μs). The strengthening of a reset voltage line (i.e., reduction of interconnection resistance) is required for the next design.

This waveform shows that the EN_TRIG_O signal has also affected the analog signal. The most important thing in this observation is that the level of an analog signal changes (jumps) after "PD Reset" state. The level of an analog signal does not return because the potential of the analog signal is not being fixed. This becomes high about 30 mV from the original voltage set up by CDS_RSTV. Therefore, when setting up VTH by Event-Driven readout mode, it is necessary to include this increment.

Thus, PD_RST signal and EN_TRIG_O have a crosstalk in an analog signal. These are based on the design of a pixel layout and the cause part became clear. We give these details in Section 6.1.1.

5.6.2 Output of Trigger Information

The greatest advantage of XRPIX is a function which outputs trigger information. Thus, it is necessary to check whether trigger signal of timing and a pixel position can be outputted correctly.

Figure 5.13 is a waveform of the outputs trigger information with the oscilloscope by XRPIX2b. The control signal shows TRIG_OUT of hit timing, and SCLK of a serial clock required for projection hit pattern readout. And the serial output signal from RA and CA shift resistors are obtained. This timing diagram was shown by Figure 4.10 of the Chapter 4.

When pulse laser is incident into the pixel of RA 77 and CA 113, the address information can be readout correctly. When TRIG_OUT changes from Low to High, a hit pattern can be outputted in inputting a serial clock. This function works good.

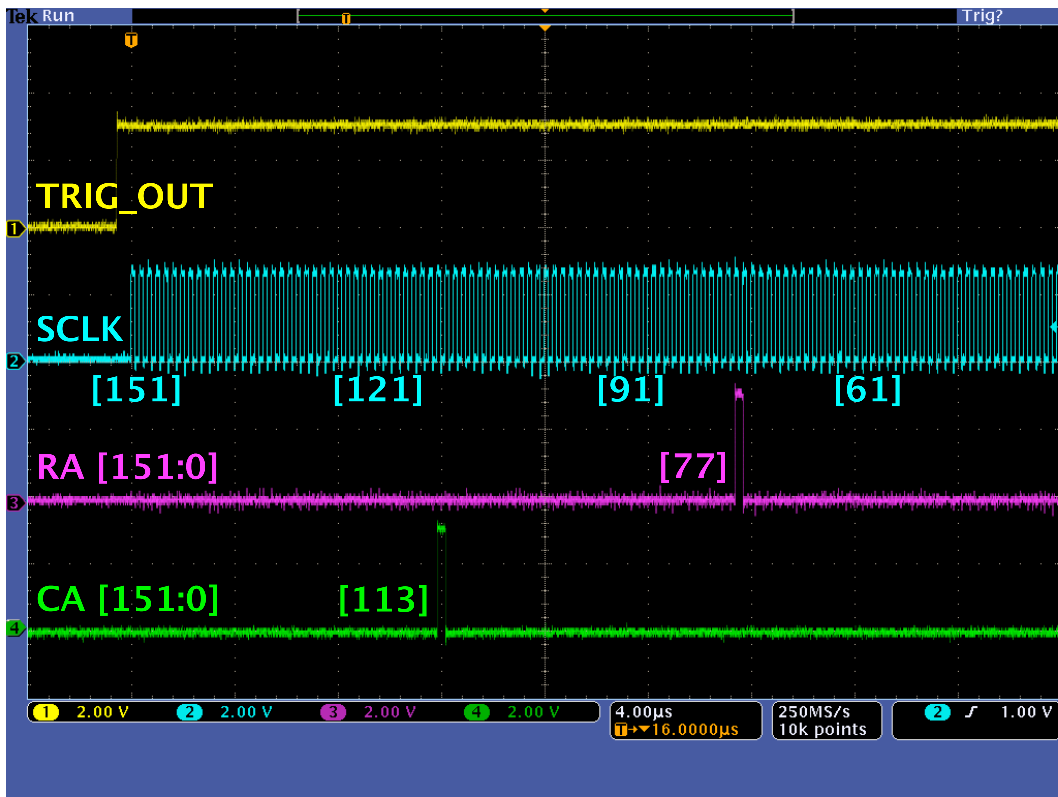
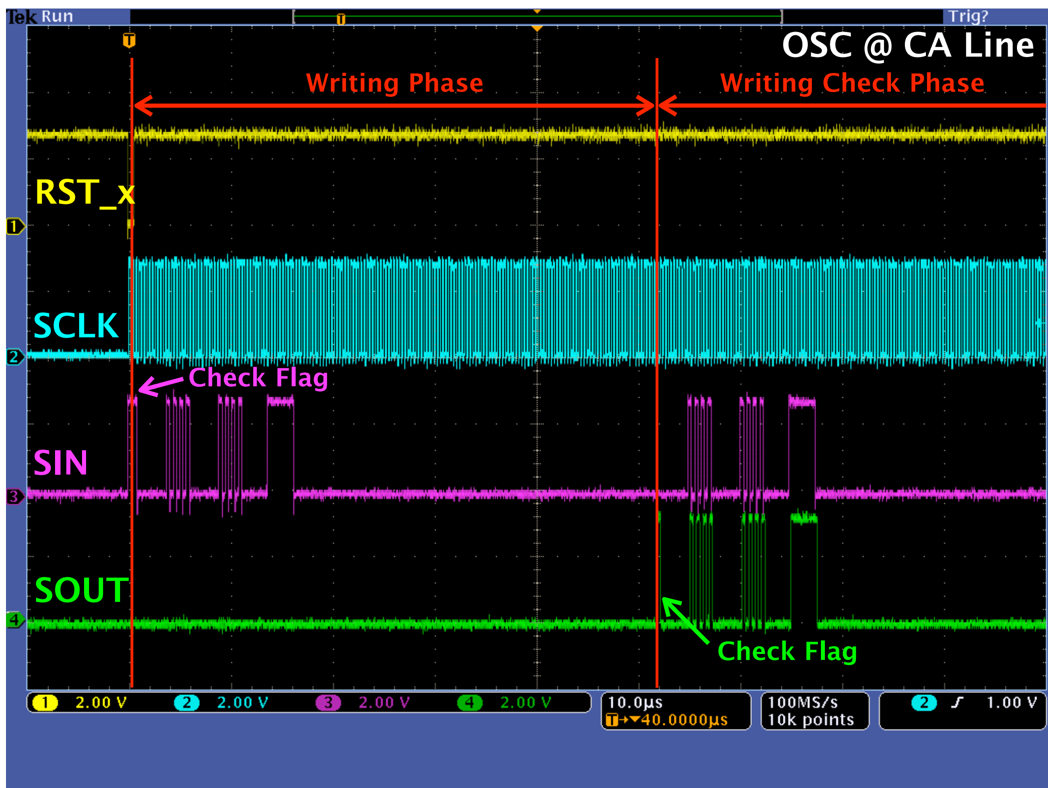


Figure 5.13: Hit pattern information output by oscilloscope.

5.6.3 Writing of Bad Pixel Mask and Control Register

XRPIX can write a bad pixel mask and a control signal in a register for advanced operation. It has two lines of CA and RA. Figure 5.14 is a waveform of the bad pixel mask and a control signal writing with the oscilloscope. The control signal shows RST_x of a data clear, SCLK of a serial clock required for writing data, SIN of a data input, and SOUT of a data output for check each of CA and RA lines. This timing diagram was shown by Section 4.4.3 of the Chapter 4.

Operation was tested by writing in arbitrary patterns and checking the output. As a result, the output of data had only CA line. However, the writing of the bad pixel mask of RA line works good from the test results. This is considered for "Clock Race" problem (see Section 6.2 for more detail). It is necessary to change arrangement of a next design.



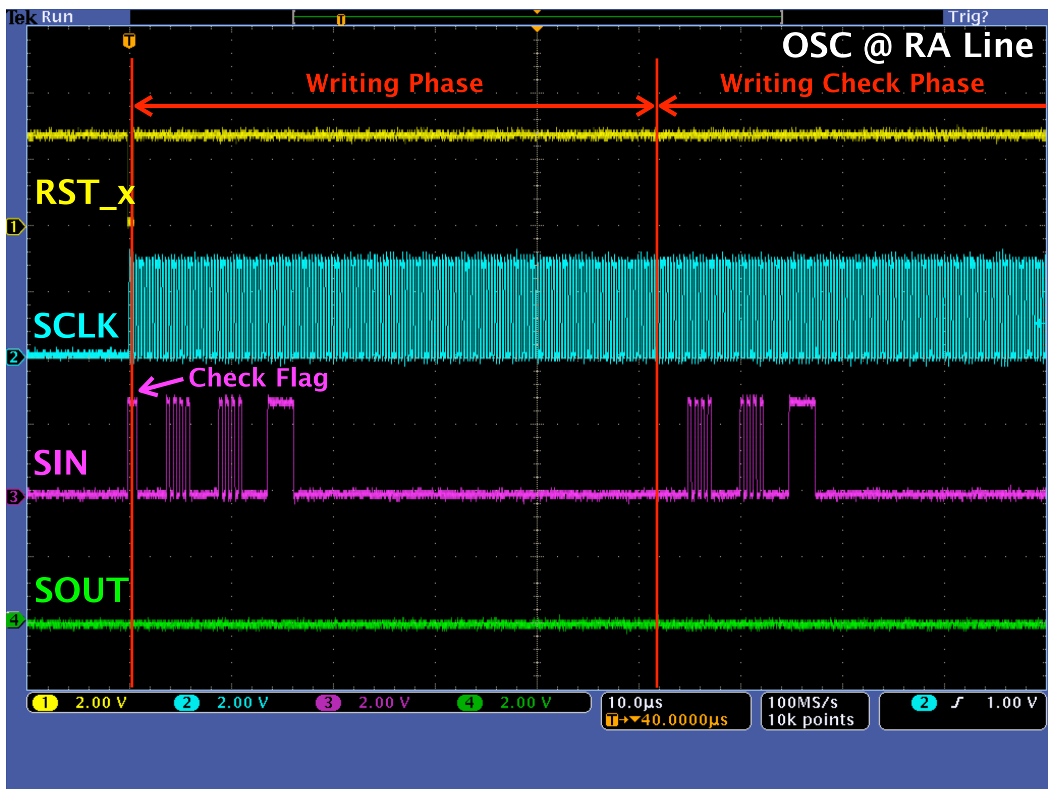


Figure 5.14: Bad pixel mask and a control signal writing.

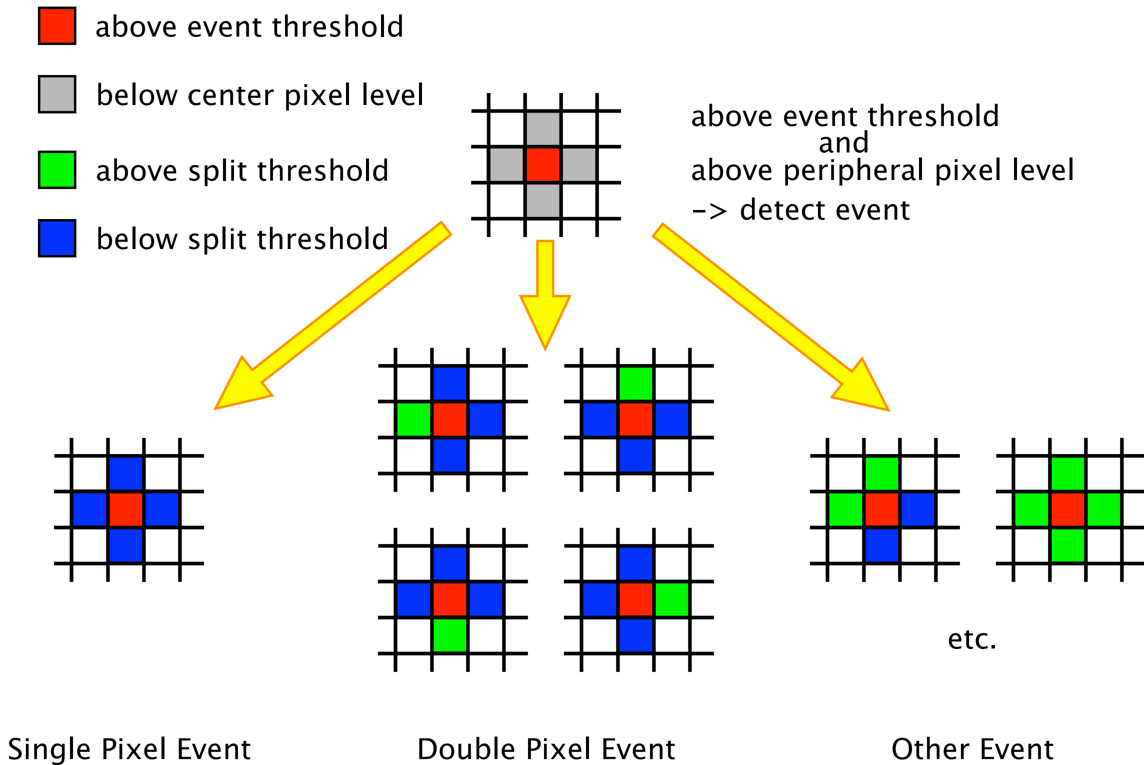


Figure 5.15: Schematic view of analysis method.

5.7 X-ray Responsivity

5.7.1 Analysis Method

In this study, two kinds of data readout methods, "Frame readout" and "Event-Driven readout", are used. "Frame readout" is the method of reading the signal of all the pixels for every frame, and analyzing data off-line. On the other hand, "Event-Driven readout" is signal readout by the trigger information output function of XRPIX, as Section 4.4.2 described. This reads only the signal of the pixel which exceeded threshold for every event (i.e., charge sharing is ignored). In the following, the analysis method of frame readout data is described.

Detect Event

First, pedestal level is calculated and it holds as data for every pixel. And the difference of a signal and a pedestal is calculated for every pixel, and this is set to pulse height (PH). In the case of X-ray events, the threshold level for judging is required. This is defined as "event threshold (ETH)" and it is set to 10 σ of a readout noise. If PH is above ETH and

higher than surrounding pixel level, it is defined as an event. Then, it divides into three patterns, Single Pixel Event, Double Pixel Event, and Other Event, with PH level of the surrounding pixel (Figure 5.15).

Single Pixel Event

The kind of event is further distinguished with the 2nd step threshold after event detection. This value is defined as "split threshold (STH)" and it is set to 3 σ of a readout noise. If the surrounding pixel level is lower than STH, this is defined as Single Pixel Event. Only PH of the pixel beyond ETH is used as energy of X-rays. Therefore, a spread of few electric charges in the surrounding pixel will be ignored. This causes the tail on the low energy side by a spectrum.

Double Pixel Event

If Single Pixel Event is removed from the detected event, the event in which the electric charge spread will remain in the surrounding pixel. Especially, when the number of the surrounding pixels exceeding STH is one, this event is defined as Double Pixel Event. In this case, the sum total value of PH of the pixel beyond ETH and STH is used as energy of X-rays.

Other Pixel Event

If Single Pixel Event and Double Pixel Event are removed from a detection event, the event which has two or more surrounding pixels more than STH in the remains. These events are removed from an analysis target.

5.7.2 X-ray Spectra

We describe the X-ray responsivity when reading out the entire area without using the Event-Driven readout mode. The comparator circuit is kept from operating by setting CDS_RSTV voltage as 400 mV and VTH voltage as 700 mV. In this test, the sensor is biased to 100 V and is cooled to -50 °C so as to suppress the dark current. Figure 5.16 shows the spectra of the X-ray emission from ^{241}Am and ^{109}Cd radio isotope samples by single pixel event. Here, the double pixel event is not used because the sharing event has the problem that charge collection efficiency is not good [1]. From these spectra, the energy

resolution is about 650 eV FWHM at 13.95 keV ($\mathrm{Np-L_\alpha}$) and 900 eV FWHM at 22.2 keV ($\mathrm{Ag-K_\alpha}$). Then, the readout noise can be calculated to be about 68 electrons rms. This value obtained from the pedestal peak.

5.7.3 Calibration

Figure 5.17 shows the plot of X-ray energy calibration using ^{241}Am and ^{109}Cd X-ray lines at 13.95 keV, 17.74 keV ($\mathrm{Np-L_\beta}$), 20.77 keV ($\mathrm{Np-L_\gamma}$), 22.2 keV, 24.9 keV ($\mathrm{Ag-K_\beta}$), and 26.3 keV (^{241}Am). The ADC gain is 7.9 (ADU/keV), based on the slope of the linear fitting. The number of electron-hole pairs generated by a traversing particle can be calculated by dividing the deposited energy by the mean energy needed for ionization which for silicon is about 3.65 eV. Therefore, 274 electron-hole pairs (1000 eV / 3.65) are generated on the average at an X-ray energy of 1 keV in silicon. As a result, the total gain of the XRPIX2b is calculated

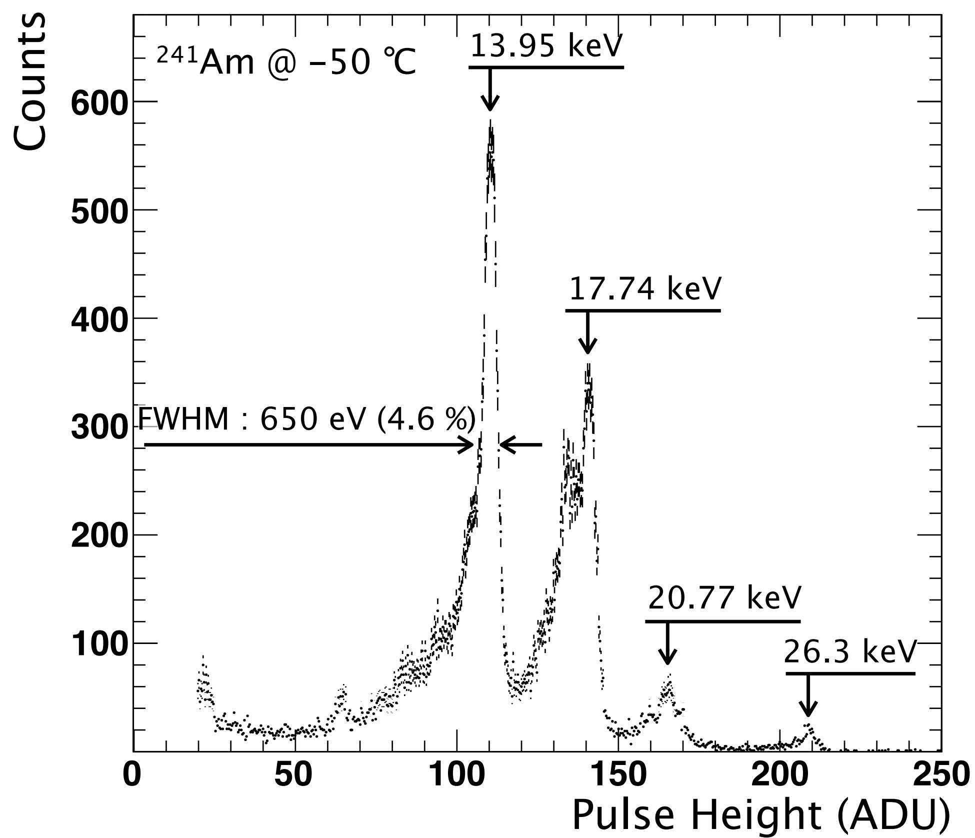
$$\mathrm{G_{fr}} \;=\; 7.9\ (\mathrm{ADU/keV}) \;\times\; 244\ (\mu\mathrm{V/ADU})\ /\ 274\ (\mathrm{e-/keV}) \;=\; 7.0\ (\mu\mathrm{V/e-}) \qquad (5.3)$$

In addition, Figure 5.17 also shows the plot of XRPIX1 and XRPIX1b for comparison. The total gain of XRPIX1 / XRPIX1b are 3.6 (μV/e$-$) / 6.2 (μV/e$-$), respectively.

5.7.4 Improvement of Spectroscopic Performance

As the Section 4.2.6 described, XRPIX3 was designed in order to improve spectroscopic performance with CSA pixel circuit. In this section, CSA pixel circuit was compared with Normal pixel circuit in order to obtain the effect of CSA. Figure 5.18 shows the plot of X-ray energy calibration using ^{55}Fe and ^{109}Cd X-ray lines at 5.9 keV ($\mathrm{Mn-K_\alpha}$), 22.2 keV, and 24.9 keV. The gain of Normal pixel is 5.2 μV/e$-$, CSA pixel is 17.9 μV/e$-$. It is 3.4 times higher gain as compared with Normal pixel circuit. This result shows that the CSA pixel circuit works good. However, observed gain (17.9 μV/e$-$) is lower than the design (50 μV/e$-$), which would be due to parasitic capacitance.

Moreover, in order to compare the performance of Normal and CSA pixels, the spectrum was obtained from ^{55}Fe radio isotope in each and they were pile up. Figure 5.19 is this spectrum. The pixel gain was not calibrated. The readout noise of Normal is 76 electrons rms, CSA is 33 electrons rms. This value is obtained from the pedestal peak. From this



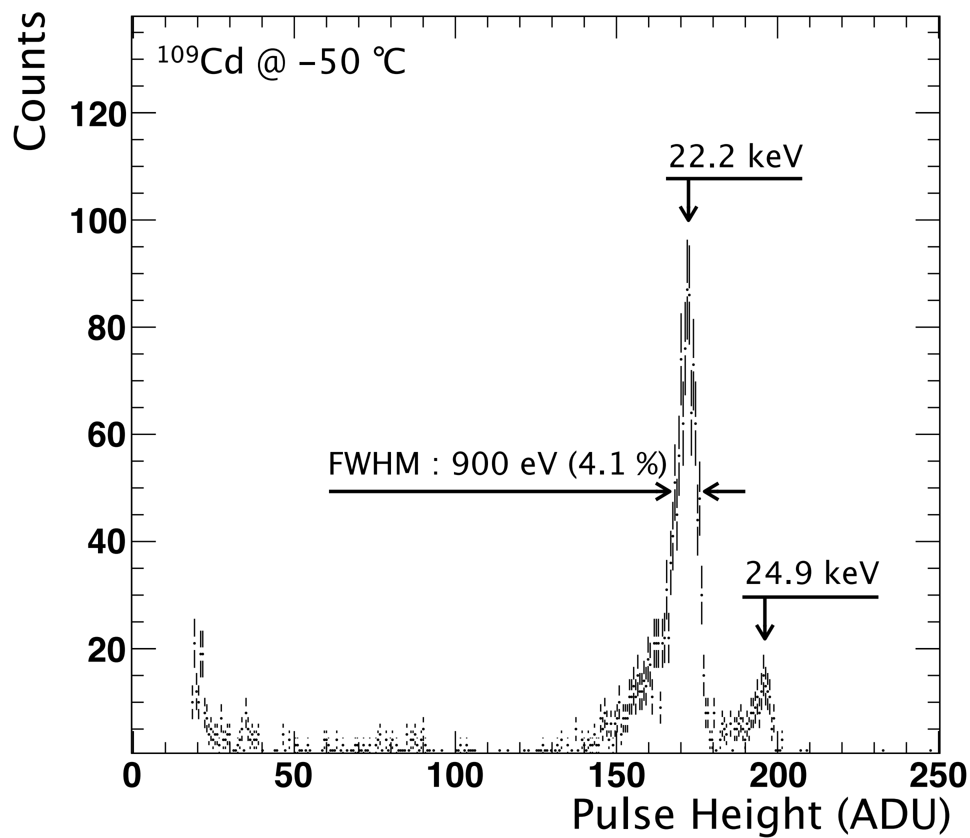


Figure 5.16: X-ray pulse height in analog digital unit (ADU) of the ^{241}Am (top) and ^{109}Cd (bottom) radio isotopes in all pixel mode. 1 ADU is 244 μV (1 V / 12 bits).

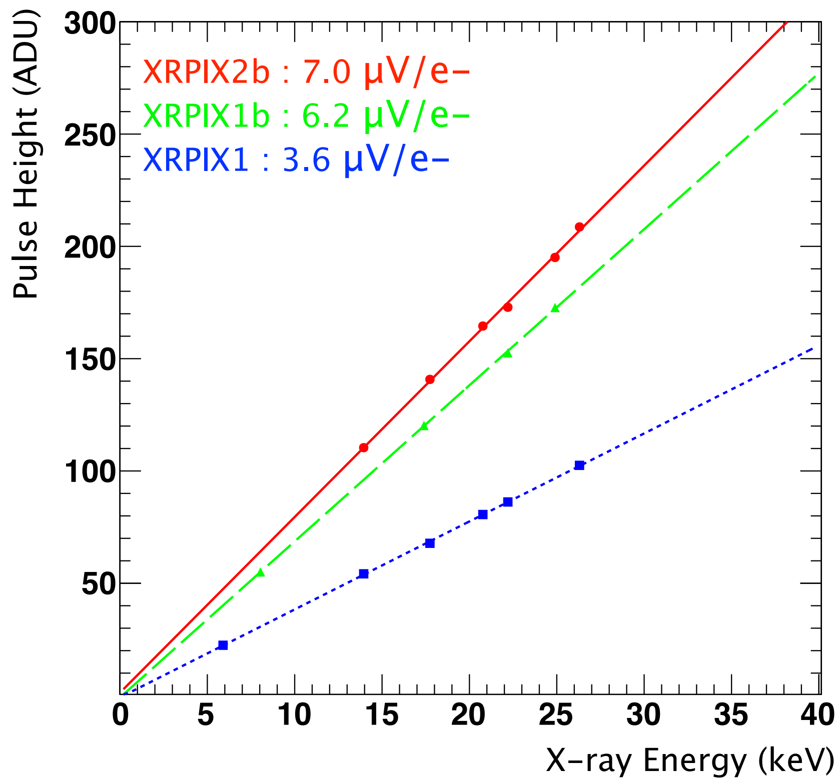


Figure 5.17: Calibration between X-ray energy and signal pulse height (ADU). The solid/dashed/dot lines show XRPIX2b/XRPIX1b/XRPIX1, respectively.

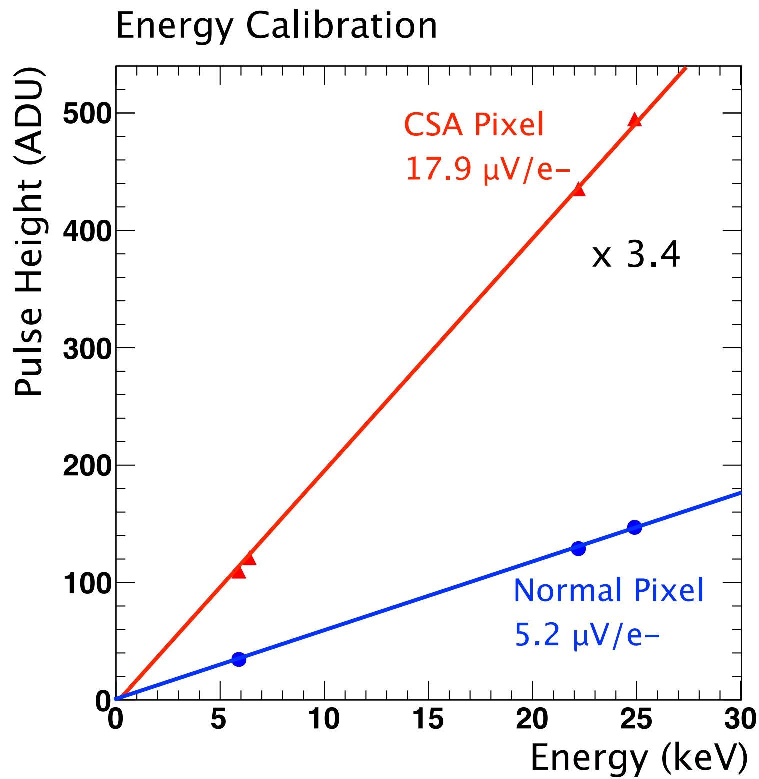


Figure 5.18: Calibration plot of Normal and CSA between X-ray energy and signal pulse height. The pulse height is shown by the unit of analog digital unit (ADU).

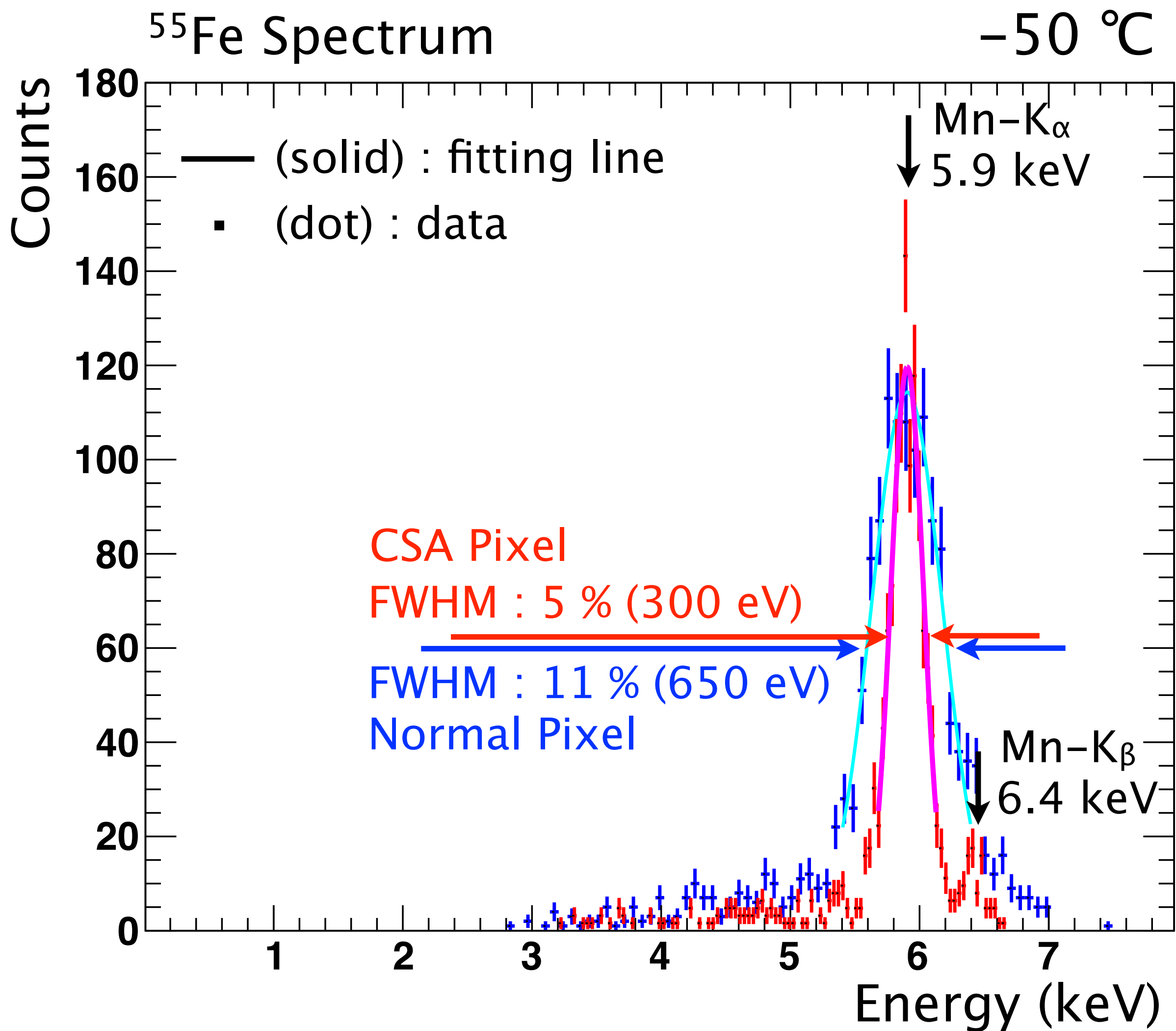


Figure 5.19: Comparison spectra of Normal and CSA pixel circuit. It is using ^{55}Fe radio isotope obtained in all pixel mode.

results, the energy resolution of Normal pixel is about 650 eV FWHM (11 %) and CSA pixel is 300 eV (5 %) at 5.9 keV. Furthermore, XRPIX3 resolved $\mathrm{Mn-K_\alpha}$ and $\mathrm{Mn-K_\beta}$ (6.4 keV) successfully for the first time in XRPIX series. By CSA pixel circuit, energy resolution has improved.

Here, it calculates about energy resolution from the obtained result. From a Formula (2.11), the energy resolution of CSA is calculated to

$$\Delta E_{CSA} = 2.35 \cdot 3.65\sqrt{5900 \cdot 0.1/3.65 + 33^2} = 300\ eV \tag{5.4}$$

$$\Delta E_{Normal} = 2.35 \cdot 3.65\sqrt{5900 \cdot 0.1/3.65 + 76^2} = 660\ eV \tag{5.5}$$

Thus, the value of energy resolution obtained from the spectrum is consistent. Although energy resolution of Normal pixel ($\Delta \mathrm{E_{Normal}}$) a little differ, this is considered because $\mathrm{Mn-K_\alpha}$ and $\mathrm{Mn-K_\beta}$ are not separable.

5.8 Event-Driven X-ray Readout

5.8.1 X-ray Spectra

The experiment most important for XRPIX is explained from here. It is about the spectra by Event-Driven readout mode at first. In this test, the sensor is biased to 100 V and is cooled to -50 °C. Figure 5.20 shows the spectrum of the X-ray emission from ^{241}Am radio isotope sample by Event-Driven with XRPIX2b. The CDS_RSTV voltage is 400 mV and the VTH voltage is 440 mV. The numbers of data are 100,000 events. The energy resolution is about 1 keV FWHM at 13.95 keV. This is not good compared with Frame readout mode. Event-Driven readout can make a 2D counts map using hit position information. The right of Figure 5.20 is this counts map. X-ray is detected uniformly. There is no count in edge (4 pixels) because the bad pixel mask is set to a trigger output. Thus the pixel of edge has the unstable characteristic, this is required. Moreover, since CA 88 was a bad column line, this has also set up the mask. Therefore, the mask can be set up correctly. Figure 5.21 is a spectrum of ^{109}Cd. A setup is the same as Figure 5.20 except VTH voltage is 470 mV. The energy resolution is about 1.2 keV FWHM at 22.2 keV.

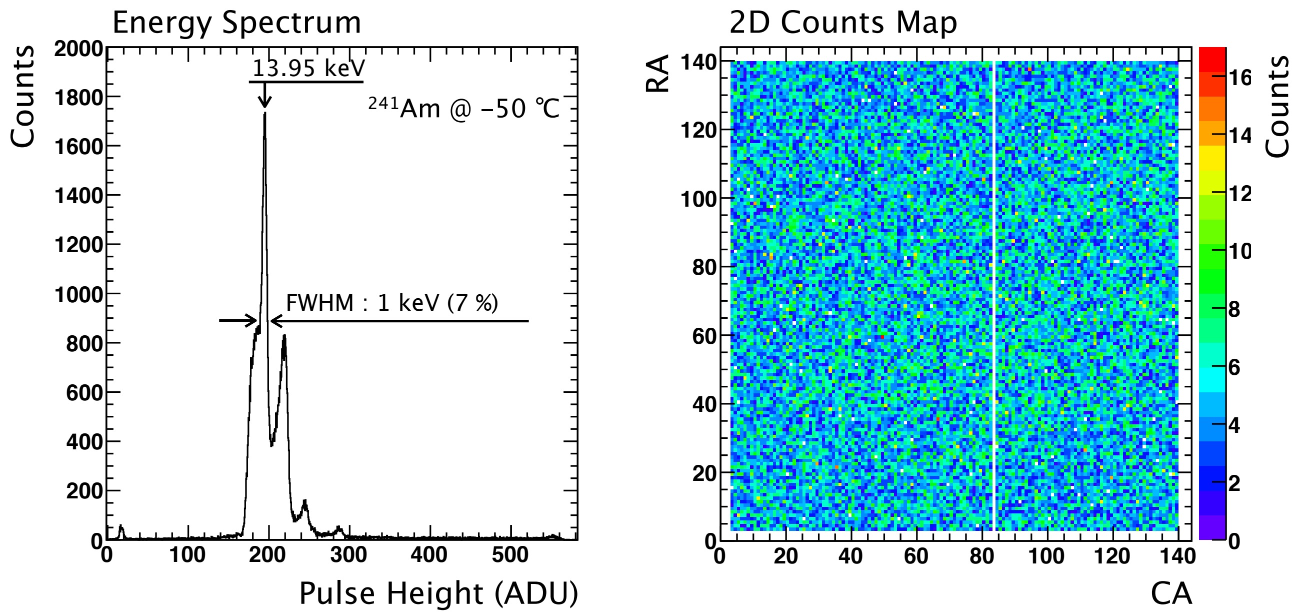


Figure 5.20: X-ray energy spectrum of ^{241}Am by Event-Driven Mode. The CDS_RSTV voltage is 400 mV and the VTH voltage is 440 mV.

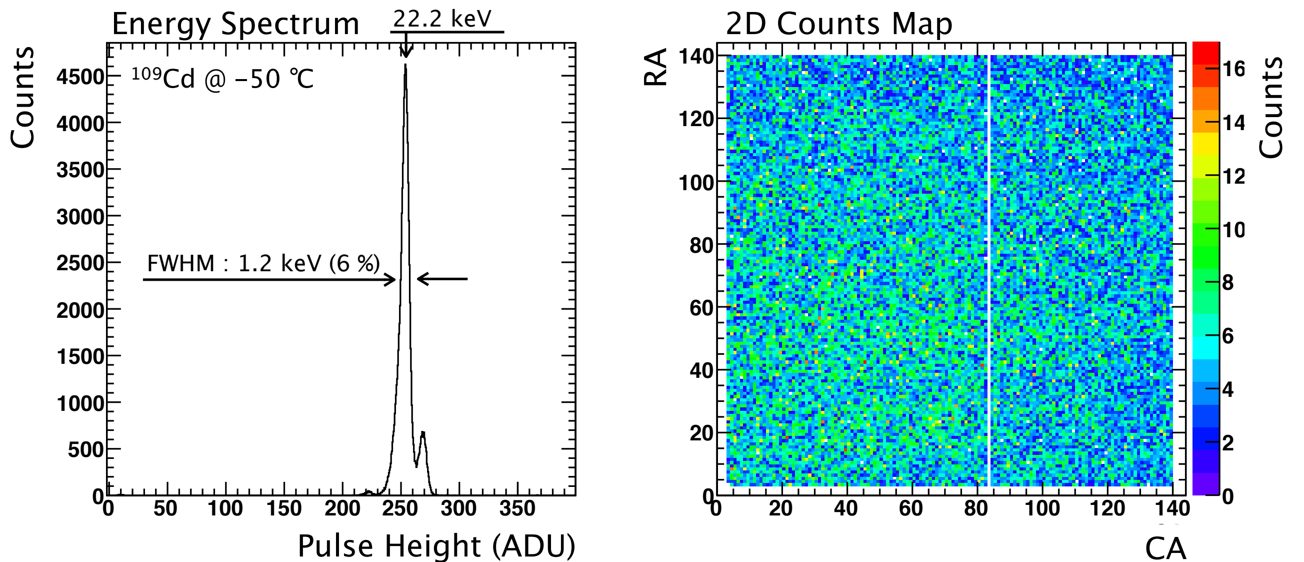


Figure 5.21: X-ray energy spectrum of ^{109}Cd by Event-Driven Mode. The CDS_RSTV voltage is 400 mV and the VTH voltage is 470 mV.

5.8.2 Calibration

Figure 5.22 shows the plot of X-ray energy calibration using ^{241}Am, ^{109}Cd, ^{55}Fe, and ^{133}Ba X-ray lines at 5.9 keV, 13.95 keV, 17.74 keV, 20.77 keV, 22.2 keV, 24.9 keV, 26.3 keV, 31 keV, and 35 keV. The ADC gain is 6.8 (ADU/keV), based on the slope of the linear fitting. Thus, the gain of X-ray response is 6.1 (μV/e$-$) by Event-Driven readout mode. However, there are three strange points in this result. First, it has offset of about 100 ADU (i.e.,

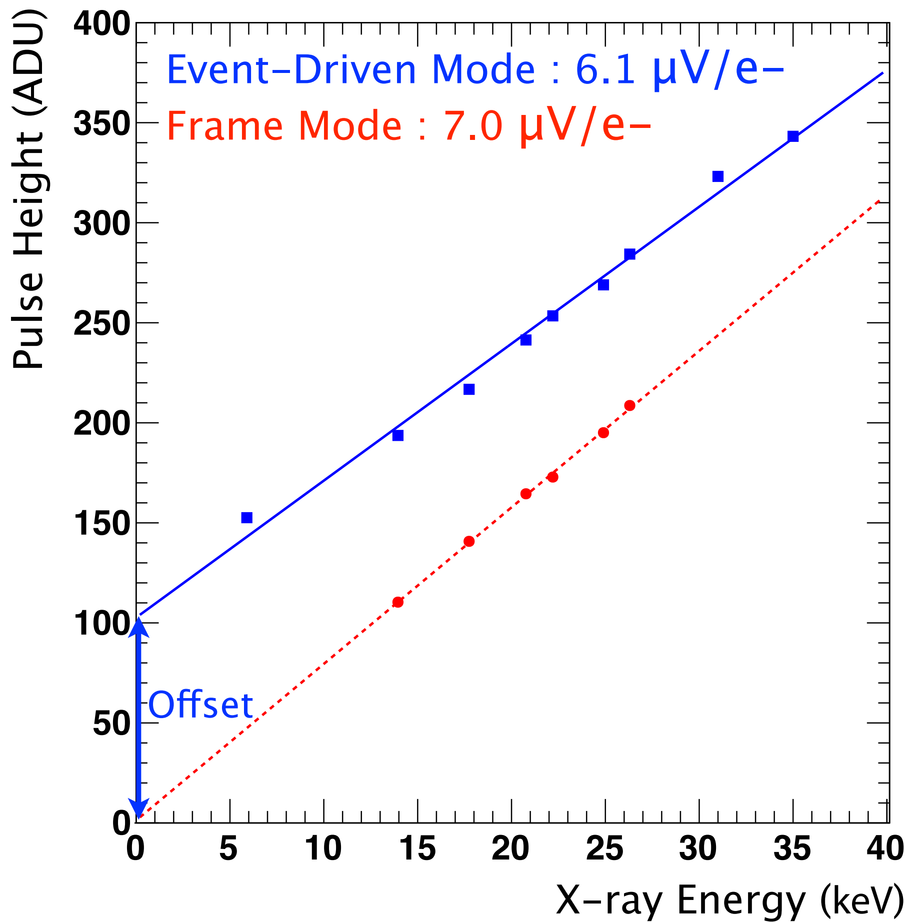


Figure 5.22: Calibration between X-ray energy and signal pulse height (ADU). The solid/dot lines show Event-Driven/Frame Mode, respectively.

~25 mV). Next, the gain of X-ray response is decreasing as compared with a frame readout mode. Finally, the linearity of fitting decreases and variation is large. It is necessary to investigate these causes and to understand phenomena. The cause of these phenomena is described from the following sections.

5.8.3 Observing of Analog Signal

In order to understand the result obtained with the section 5.8.2, the analog waveform was observed with the oscilloscope. Figure 5.23 is a waveform of Event-Driven readout mode when the X-rays emission from ^{109}Cd radio isotope. The control signal shows TRIG_OUT which is the logic output signal of a comparator circuit, and Event Assert which is fixed signal of X-ray event. By setting up bad pixel mask, only one pixel makes a trigger signal output. And by assigning this pixel, the trigger signal and the analog waveform when X-rays enter can be observed. From this waveform, when X-rays enter, the large negative pulse has

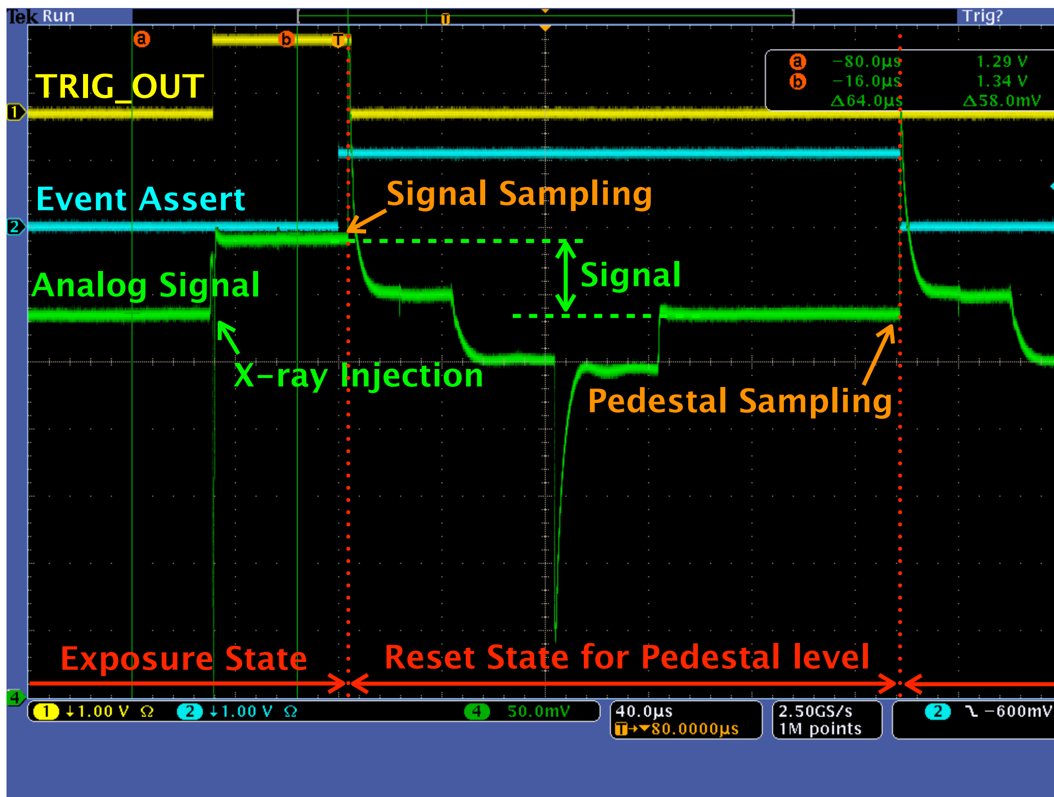


Figure 5.23: The Event-Driven waveform when the X-rays injection from ^{109}Cd radio isotope.

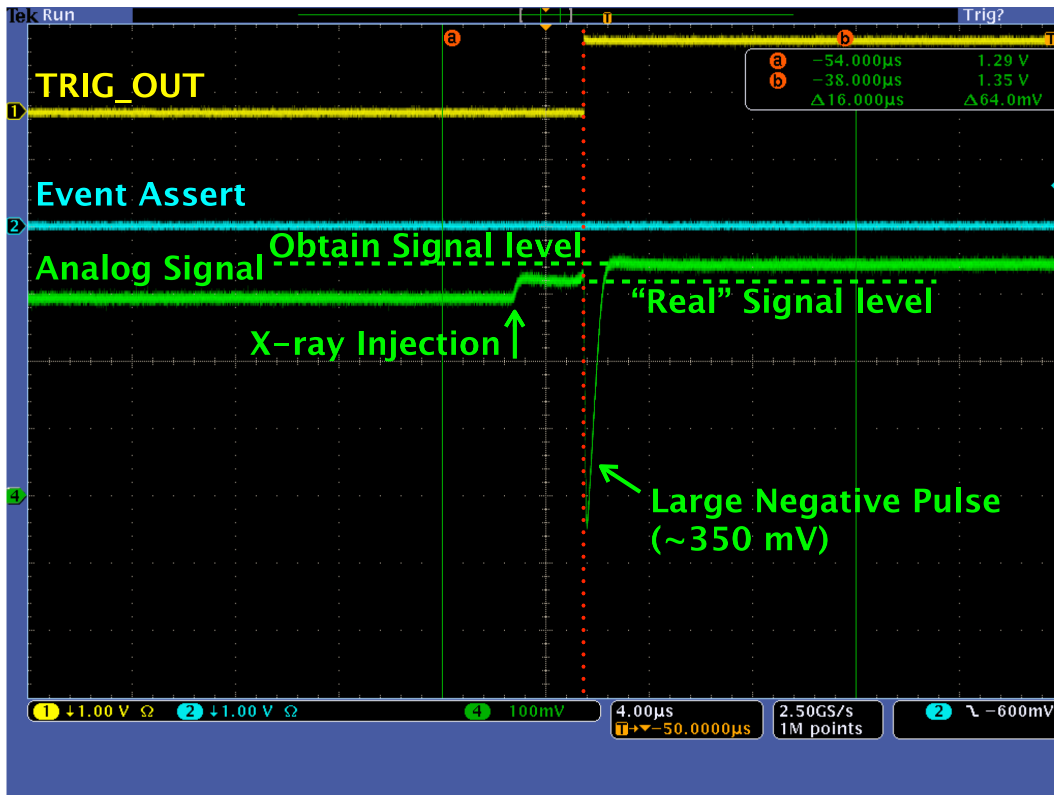


Figure 5.24: The waveform which expanded the time of X-ray injection of Figure 5.23. There are many problems in this waveform.

occurred in the analog signal. Figure 5.24 shows the waveform which expanded the time of X-ray injection of Figure 5.23. There are four problems in this waveform. First, it has a large negative pulse when TRIG_OUT changed the logic from Low to High, of course. It is about ∼350 mV. Next, it has a difference between the "real" signal level and "obtain" signal level. Furthermore, a logic converting time is long. In this case, it is about ∼5 μs (typically, ∼50 ns). Finally, the analog signal is changed from X-rays enter to the logic of TRIG_OUT is converted. It is required to understand these phenomena in order to solve the problem of Event-Drive readout mode. Although it was not easy, we were able to understand almost about these phenomena.

The large negative pulse appears for the parasitic capacitance by wiring. This was checked on the layout level for the large crosstalk of a trigger signal and an analog signal. As a result, the trigger signal and analog signal of the direction of a column are parallel (see Section 6.1.2 for more details). This is confirmed also in the HSpice circuit simulation. Fortunately, this does not happen in the usual data acquisition. It is the phenomenon of appearing only when a pixel is fixed and it observes the analog signal. However, in order to reduce a crosstalk, it is necessary to take care by a next design.

The difference of a "real" signal level and an "obtain" signal level appears by the capacitive coupling of a trigger signal line and an analog signal line. This is understood from an analog signal level "jumping" and not returning to the original level. Of course, this is unrelated to a large negative pulse. It is thought that it is in the same situation as the Section 5.6.1. However, this place has not been specified. The difference of an observation signal level is equivalent to offset of calibration plot (Figure 5.25). This is existing offset which cannot be prevented under the present circumstances.

From the test result, the long logic converting time has observed what is depended on VTH voltage. Figure 5.26 shows the waveform of X-ray injection of ^{109}Cd by changing a threshold voltage. The CDS_RSTV voltage is 400 mV. The VTH voltage is every 10 mV from 440 to 470 mV. Its horizontal axis is for the time to X-ray signal readout processing, and the vertical for the voltage on the basis of pedestal level. The time is so required for logic reversal that the difference of threshold and signal voltage is small. It is about 5 μs at the maximum. This is the characteristic of a comparator circuit (see Section **??** for more detail). This phenomenon is confirmed by the HSpice circuit simulation. Therefore, this is signal change which can be explained only in a pixel circuit.

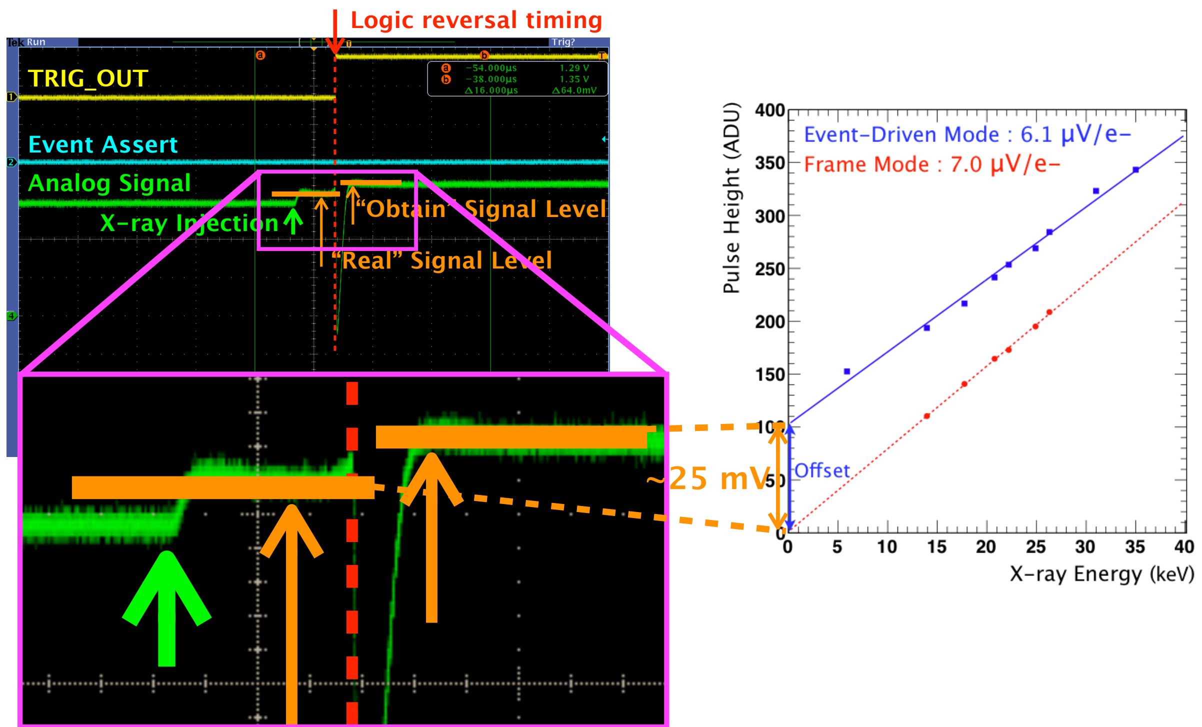


Figure 5.25: About the difference of an observation signal level. The difference of a "real" signal level and an "obtain" signal level is equivalent to offset.

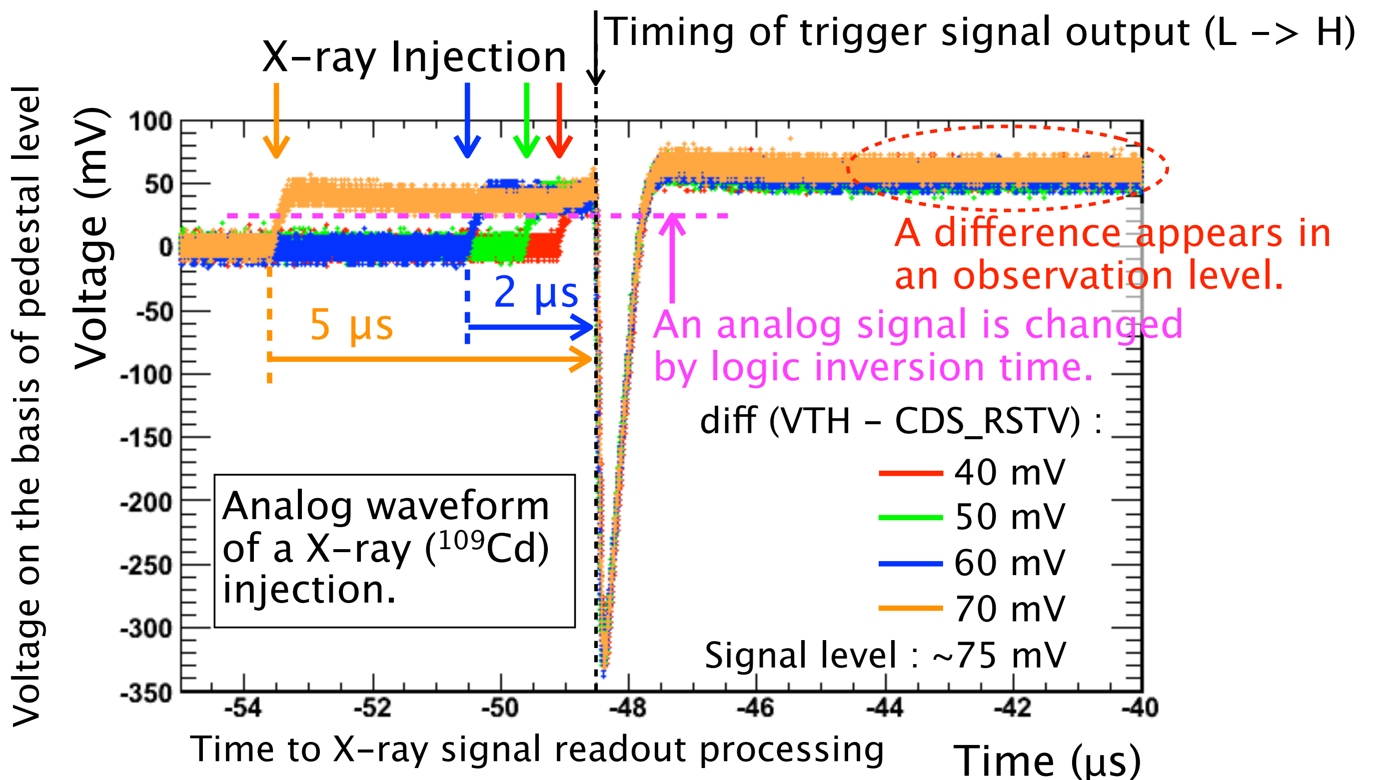


Figure 5.26: The waveform of X-ray injection of ^{109}Cd by changing a threshold voltage. The CDS_RSTV voltage is 400 mV. The VTH voltage is every 10 mV from 440 to 470 mV.

The Figure 5.26 can obtain information also about change of the analog signal from X-rays enter to the logic converting of TRIG_OUT. The change of this analog signal has appeared as a difference of an observation level. Then, why does an analog signal change? It is considered to be the cause that it has not separated the power supply line of the analog and the digital circuit. The long logic inversion time makes the long intermediate state of a CMOS circuit, and consumes much current in the pixel circuit. Thereby, the output level of analog signal is affected.

These are understanding of the problem of the Event-Drive readout mode. As for the waveform which appears when X-rays enter, many phenomena are involved. We have to reflect these solutions on the next design.

5.8.4 Spectra Shape of Frame and Event-Driven Readout

From Section 5.8.3, operation of the comparator circuit affected the analog signal and it indicated that the influence was based on the relation of the threshold voltage and the signal level. That is, it is not related to readout method of Frame and Event-Driven. Therefore, if CDS_RSTV voltage and VTH voltage are the same conditions, it was able to be shown that Frame readout and Event-Driven readout do not have a difference in a spectrum shape. In order to know change of the spectra by threshold voltage in detail, evaluating by Frame readout mode is effective.

5.8.5 Energy Peak Shift by Changing a Threshold Voltage

In order to obtain the relation of an input signal and a threshold voltage, the X-ray spectrum from ^{241}Am was obtained by changing threshold voltage on Frame readout mode. Figure 5.27 shows the relation of threshold voltage and each peak from emission of X-ray energy (i.e., pulse height of signal level) when CDS_RSTV voltage is set to 400 mV. Furthermore, the gain of the X-ray responsivity in each threshold voltage obtained by three or four points is also plotted in the second axis. There was an energy peak shift from this result. The jump of pulse height in the voltage of 450 to 475 mV is offset by the comparator circuit operating. From this plot, when the difference of a signal level and a threshold voltage is small, it seems that the gain decreased by having influence on output signal. Furthermore, if there is a difference of an input signal and a threshold voltage, it is shown that linearity is maintained. Figure 5.28 is the plot at the time of setting threshold voltage as 430 mV by

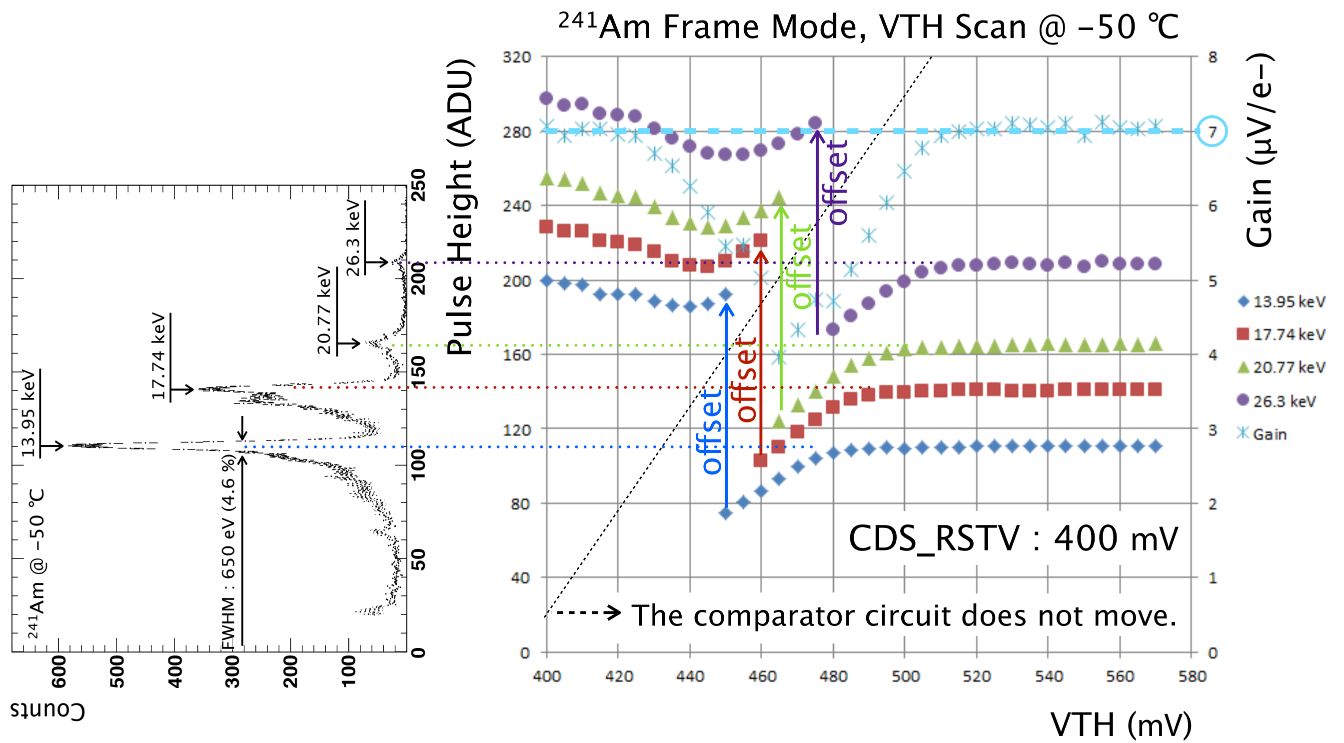


Figure 5.27: Energy peak shift of ^{241}Am by changing a threshold voltage.

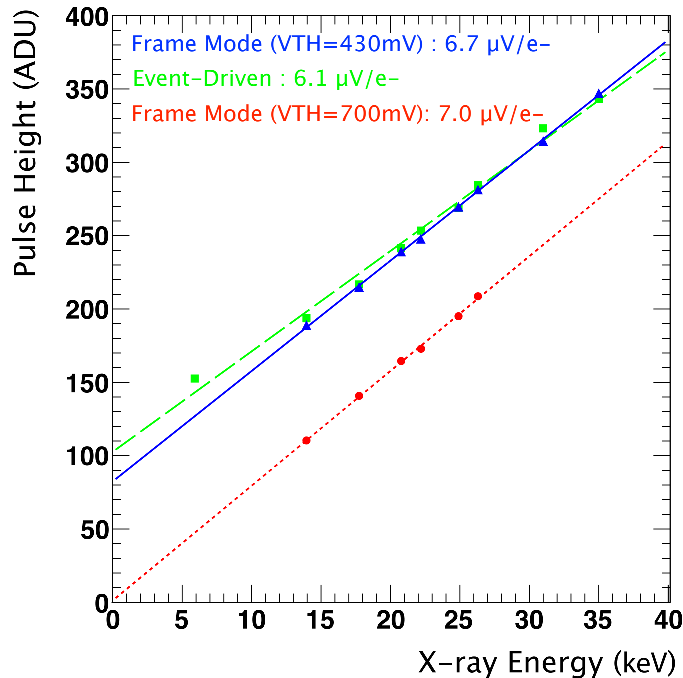


Figure 5.28: Calibration between X-ray energy and signal pulse height (ADU). The solid/dashed/dot lines show Frame Mode (VTH = 430 mV)/Event-Driven Mode/Frame Mode (VTH = 700 mV), respectively.

Frame readout mode. Therefore, when obtaining a spectra by Event-Driven readout mode, it is necessary to set up threshold voltage low above a noise level.

References

[1] H.Matsumura et al., "Investigation of Charge-Collection Efficiency of Kyoto's X-ray Astronomical SOI Pixel Sensors, XRPIX", *Nucl. Instrum. Methods*, 2014 .

Chapter 6

Discussion

This thesis describe about basic development of the new detector for future X-ray astronomy. In previous chapters, we showed about the development and the evaluation results of XRPIX. In this chapter, we discuss the evaluation results and future works from previous contents.

6.1 Crosstalk of the Control Signal in the Layout

The XRPIX2b has some crosstalks from the test result of Chapter 5. These causes are the problems of a layout. The LSI design needs to take care especially about crosstalk of an analog and a digital signal. Furthermore, since the sensor layer of SOIPIX is very close to a circuit layer (∼200 nm), we have to take care also about the crosstalk of this part.

6.1.1 The Crosstalk in Reset Operation of Pixel Circuit

In Section 5.6.1, we obtained the waveform in which PD_RST signal and EN_TRIG_O signal influence an analog signal. This is for the capacitive coupling between each wiring or sense-node (BPW). Figure 6.1 is the relation in the pixel layout of analog line, PD_RST signal, EN_TRIG_O signal and sense-node.

First, PD_RST signal wiring has capacitive coupling with the analog signal wiring which approaches in the same layer. The size of parasitic capacitance is about ∼0.5 fF. Thus, the sizes in all the pixels (∼20 k) are about ∼10 pF. This can be greatly reduced by arrangement of wiring. Furthermore, a time constant can be made small by expanding the input wiring width of PD_RSTV voltage.

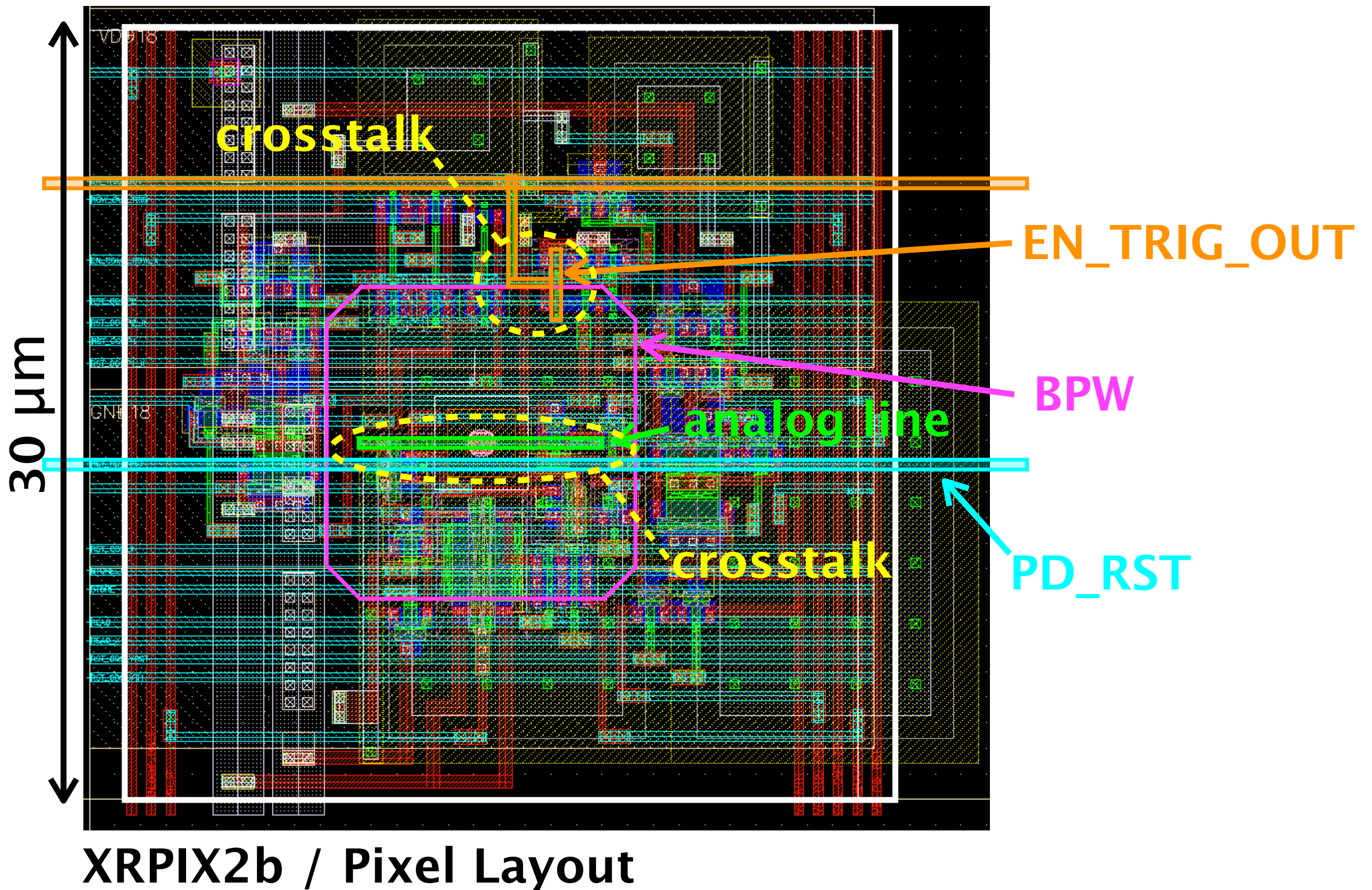


Figure 6.1: The relation in the pixel layout of analog line, PD_RST signal, EN_TRIG_O signal and sense-node (BPW).

Next, EN_TRIG_O signal wiring has capacitive coupling with the sense-node. The size of parasitic capacitance is about ∼0.4 fF. This can also be greatly reduced by arrangement of wiring. Moreover, it is avoidable by changing timing diagram, i.e., change EN_TRIG_O signal in the state of "PD Reset".

Although these waveforms disappear in the HSpice simulation of only a pixel circuit, they appear by adding capacitive coupling. This means that the layout caused the crosstalk.

6.1.2 The Crosstalk by Trigger Signal Conversion

In Section 5.8.3, we obtained the waveform of the large negative pulse to the analog signal under the influence of a trigger signal. This is for the capacitive coupling between each wiring. Figure 6.2 is the relation in the pixel and chip layout of COL_TRIG_OUT signal and COL_OUT signal. These wiring constitutes capacitive coupling as long as 4.6 mm by a column line. The size of parasitic capacitance is about ∼250 fF. This crosstalk can also be

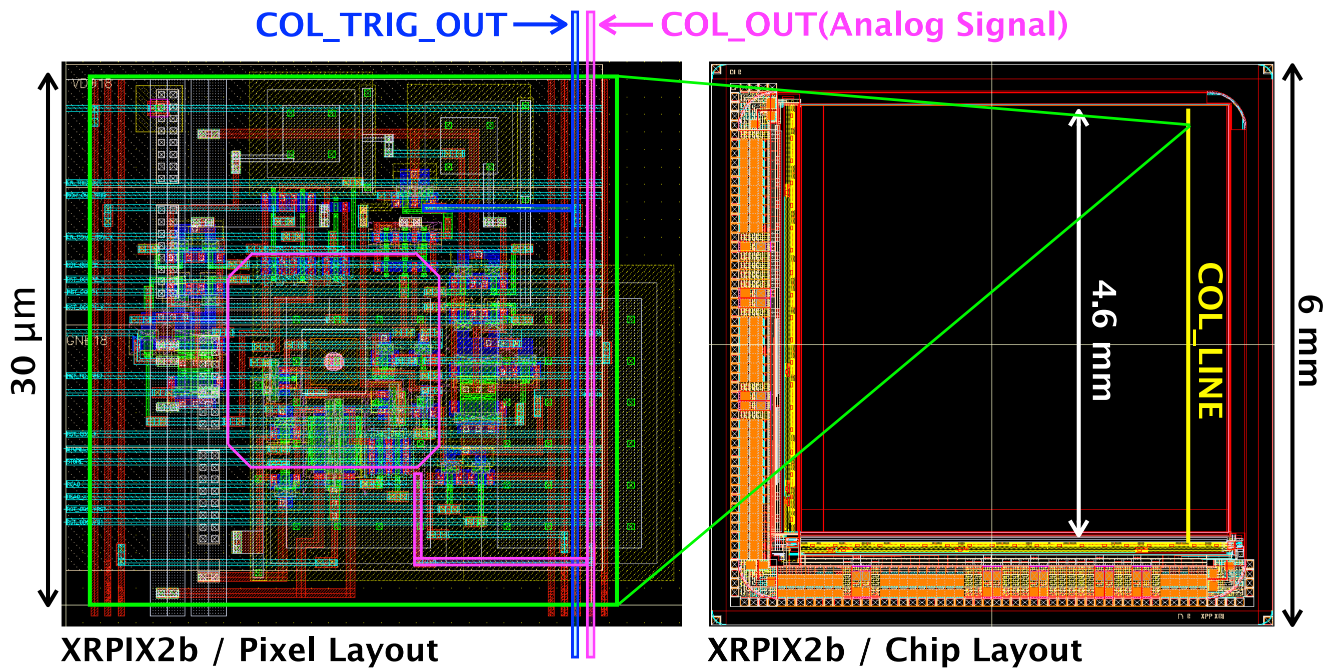


Figure 6.2: The relation in the pixel and chip layout of COL_TRIG_OUT signal and COL_OUT signal.

checked by the HSpice circuit simulation. However, if the pixel does not be selected, this cross talk does not affect an analog signal. Of course, it is good to detach wiring and to reduce capacitive coupling.

6.2 "Clock Race" Problems

In Section 5.6.3, we have checked the output of data only from CA line. However, the writing of the bad pixel mask of RA line works good from the test results. This is considered for Clock Race problem. It is a phenomenon which cannot write in the data to a shift register by a signal delay. In most registers of CMOS circuit, these delays are very small and each type of register has characteristic setup and hold times due to the circuit construction. In a synchronous circuit, if the data input to register does not obey the setup and hold-time constraints, then potential "clock race" problems may occur. These races result in erroneous data begin stored in registers.

Figure 6.3 shows the block diagram of RA line registers. In a shift register of bad pixel mask, the signal flow of a clock and data lines is opposite. Therefore, the possibility of a clock race problem is low. By contraries, in a shift register of control register, those signal flows are the same. This has the high possibility of a clock race problem. Thus, it is thought that the problem was caused by arrangement of the circuit element.

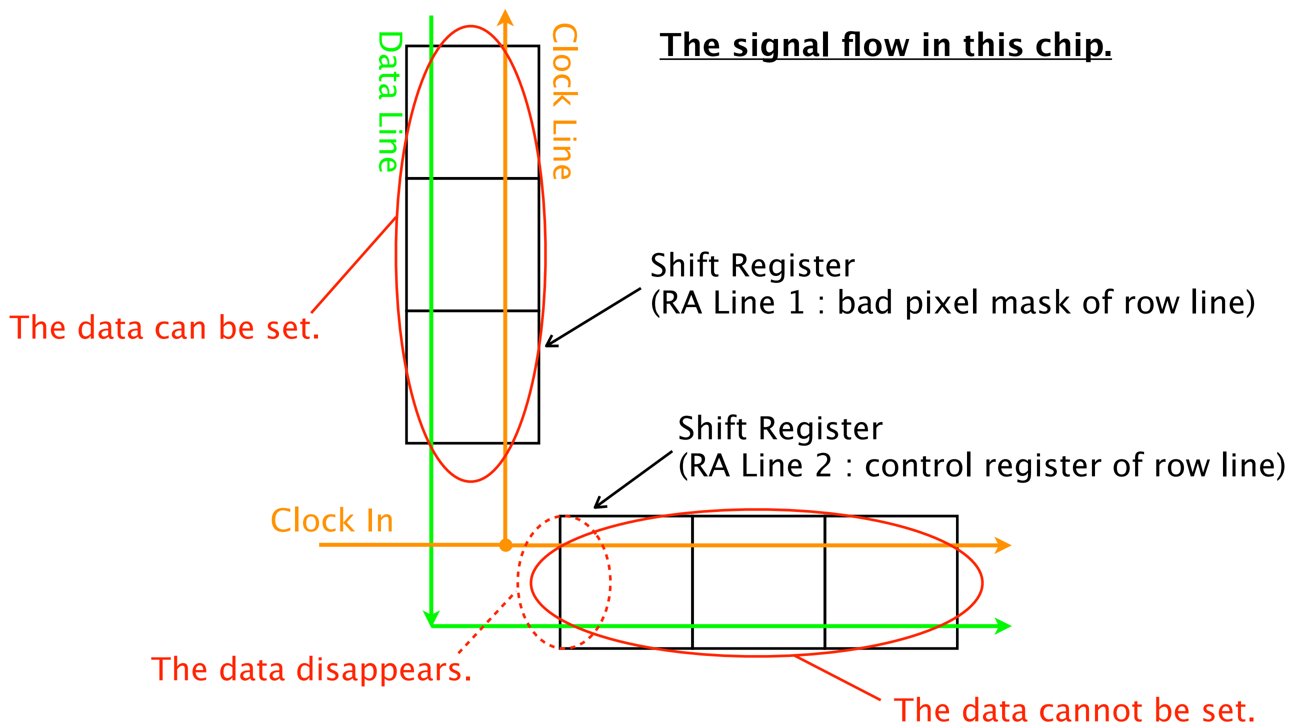


Figure 6.3: The block diagram of RA line registers. This composition caused the clock race problem.

6.3 Event-Driven Readout

The greatest advantage of XRPIX is Event-Driven readout. Acquisition of the X-ray spectrum was realized by such operation for the first time in the world in this thesis. It is important for this operation to maintain spectroscopic performance and to readout the X-ray signal fast. In XRPIX2b of middle size, reset time ($\sim 100\ \mu$s) has been restriction of event rate tolerance. In small size, reset time is below 5 μs. Furthermore, time for readout of a hit-pattern is required about 50 μs. For this reason, the event rate tolerance of XRPIX2b is about 1 kHz. In the future, shorter reset time and quicker readout time of trigger information will be required towards the increase in detector size and the number of pixels.

We have an idea to each subject. First, although it is about short reset time, it corresponds by strengthening trace of reset voltage, and attaching a bypass capacitor to the both ends of trace. Next, although it is about the quicker readout time of trigger information, it corresponds by dividing of a hit-pattern readout line, and attaching an encoder with a hit-pattern judging function. About this encoder, the simple prototype is mounted in XRPIX3. Furthermore, since operation of a comparator circuit is also influential, change of composition is required.

6.4 Spectroscopic Performance

In order to improve energy resolution, it is necessary to increase the gain of an X-ray responsivity. To XRPIX2b, a pixel circuit is constructed based on source follower circuit. In order to increase the gain, it becomes a design with small sensor capacitance, i.e., it means a design with a small BPW region of a pixel. However, since this method reached the limit, the pixel circuit introduced the charge sensitive amplifier circuit from XRPIX3. As a result, the gain increased greatly without changing BPW size, and it has improved spectroscopic performance. The gain by the SF circuit of XRPIX2b (BPW area is 12 μm sq.) is 7.0 μV/e$-$, and a readout noise obtained from pedestal peak is 68 electrons. The gain by the CSA circuit of XRPIX3 (BPW area is 14 μm sq.) is 17.9 μV/e$-$, and a readout noise obtained from pedestal peak is 33 electrons.

Figure 6.4 shows the history of readout noise with XRPIX series and future expectation. The readout noise was able to be reduced from the time of 400 electrons (rms) by INTPIX3[1] to 10 % by XRPIX3. Thus, reduction of a readout noise is one of the future big subjects.

By the way, the gain should not just necessarily only increase. Then, may a pixel circuit increase a gain? For example, suppose that the energy of 80 keV is covered with the dynamic range of 1 V. At this time, electron-hole pair is generated in the 22,000 sum totals (= 80 keV / 3.65 eV). Therefore, the upper limit of the gain in this case is 45 μV/e$-$ (= 1 V / 22,000 e-h pairs). By optimization of a pixel circuit, spectroscopic performance still improves.

6.5 Pixel Circuit

As the Section 6.3 and the Section 6.4 described, Event-Driven was successful, however change of a circuit is required. Now, the comparator circuit has adopted the inverter-chopper type. Since only the time of logic change consumed current, this circuit was adopted as a circuit of XRPIX with which low power consumption is required. However, when the difference of threshold voltage and a signal level is small, logic change takes much time (~ 5 μs) to this circuit. This behavior can be checked also by HSpice. Thus, it is not possible detect low energy X-ray. Therefore, change of comparator circuit composition becomes indispensable. A differential comparator can be considered as a candidate. The Event-Driven readout is completed by this new circuit composition.

[1]INTPIX3 is the SOIPIX X-ray imager of a normal charge integration-type.

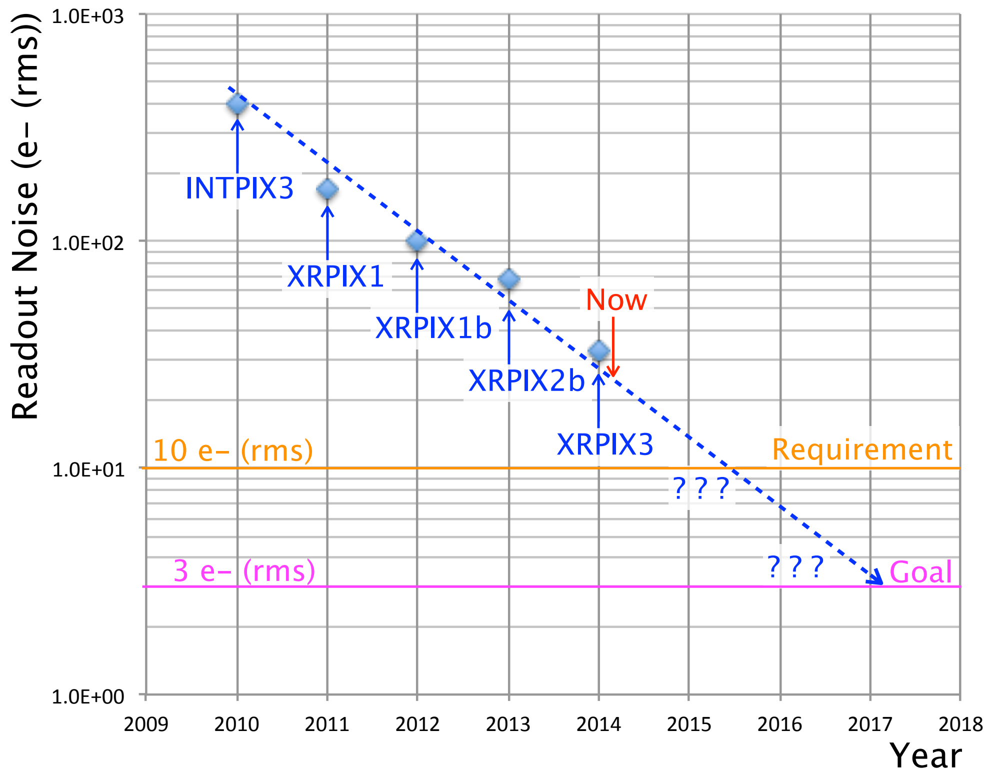


Figure 6.4: History of readout noise with XRPIX series. And future expectation.

6.6 Pixel Structure

As the Section 6.4 described, the gain has been increased by designing a BPW region small. However, this has some problems. First, a pixel circuit has influence of back gate effect. Next, a charge collection efficiency decreases. In order to solve these problems, introduction of Double SOI wafer and study of pixel structure are required. By introducing Double SOI wafer, even if it makes BPW size small, the back gate effect can be suppressed. Moreover, even if it makes BPW size small, it is necessary to realize pixel structure with high charge collection efficiency. This may be able to be made from implanting in BNW between pixels.

Chapter 7

Conclusion

In this thesis, a new detector called XRPIX series based on SOIPIX technology developed for future X-ray astronomical satellite mission is described. This detector has a comparator circuit in each pixel. Therefore, it has a capability to output timing and a hit-position information simultaneously when X-rays and charged particles signal crosses the threshold voltage of the pixel. This function offers us new operation regime of "Event-Driven readout" which judges whether it is a "real X-ray signal" for every detection events.

As of 2013, XRPIX series has designed six devices of XRPIX1/1b/2/2b/3/3b. In each chip, Event-Driven readout and spectroscopic performance are tested and improved. XRPIX2b has a middle size of sensing area (effective area is 4.6 mm square, pixel size is 30 μm square, number of pixels is 20 k) and succeeded in acquisition of the spectrum by Event-Driven readout mode. We think this is a world first detector realized this function. The event rate tolerance is over 1 kHz.

In view point of the spectroscopic performance, XRPIX3 achieved best performance in the SOIPIX detectors. It includes a charge sensitive amplifier in each pixel for the first time in the XRPIX series. The gain of X-ray responsivity is 17.9 μV/e$-$. The readout noise is 33 electrons rms from the pedestal peak and the energy resolution is about 300 eV FWHM at 5.9 keV from ^{55}Fe radio isotope. Furthermore, XRPIX3 resolved $\mathrm{Mn} - \mathrm{K}_\alpha$ (5.9 keV) and $\mathrm{Mn} - \mathrm{K}_\beta$ (6.4 keV) successfully for the first time in our series. Thereby, XRPIX reached the spectroscopic performance accepted as an X-ray detector.

Appendix A

More Experimental Result

We showed many evaluation results of XRPIX in Chapter 5. However, there are also some evaluation results used as the supplement of a main subject. In this chapter, we describe the result of the others which are consulted by this study.

A.1 IV Measurement of Other Chip

We showed the result of measurement with the Section 5.2.1. However, it was described that there are some from which behavior differs on the back bias voltage above 250 V. The Figure A.1 is a result of this example. This is based on individual specificity. As a cause, the increase in the leakage current by the depletion region having touched the side of chip can be considered. Furthermore, Figure A.2 is the arrhenius plot obtained from the Figure A.1. This figure shows that the main ingredients of leakage current are except generation current on the back bias voltage above 250 V.

A.2 Consumed Power of XRPIX2b

In the Section 5.4, we described that XRPIX2b could not measure consumed power correctly for the mistake of a layout design. Figure A.3 is a comparison plot of DAQ standby (not DAQ) which consumed power is the maximum. XRPIX2b has the back gate effect in 3.3 V power supply line (HV). This means disappearance of BPW area. The layout design was checked in order to investigate the cause of behavior of HV. By applying BPW layer which is a shield of back bias voltage red, it turned out that there is no area of BPW layer in IO Buffer. It is mainly using HV. The BPW layer of IO Buffer cannot erase here by simple

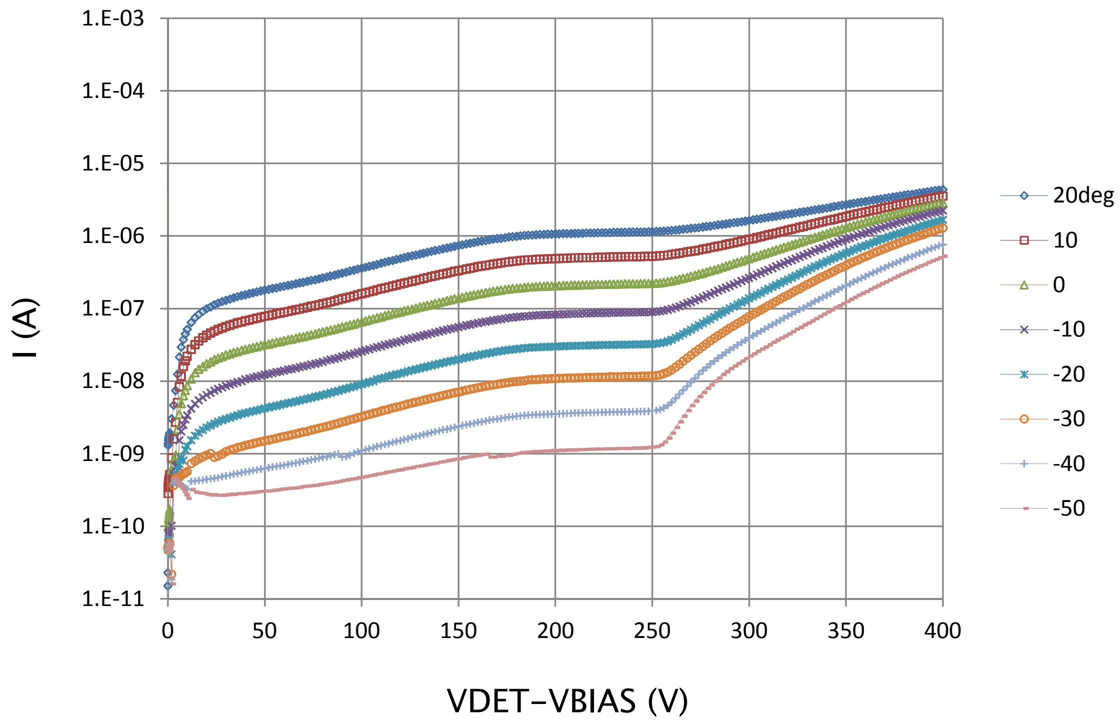


Figure A.1: I-V measurement of XRPIX2b in other case.

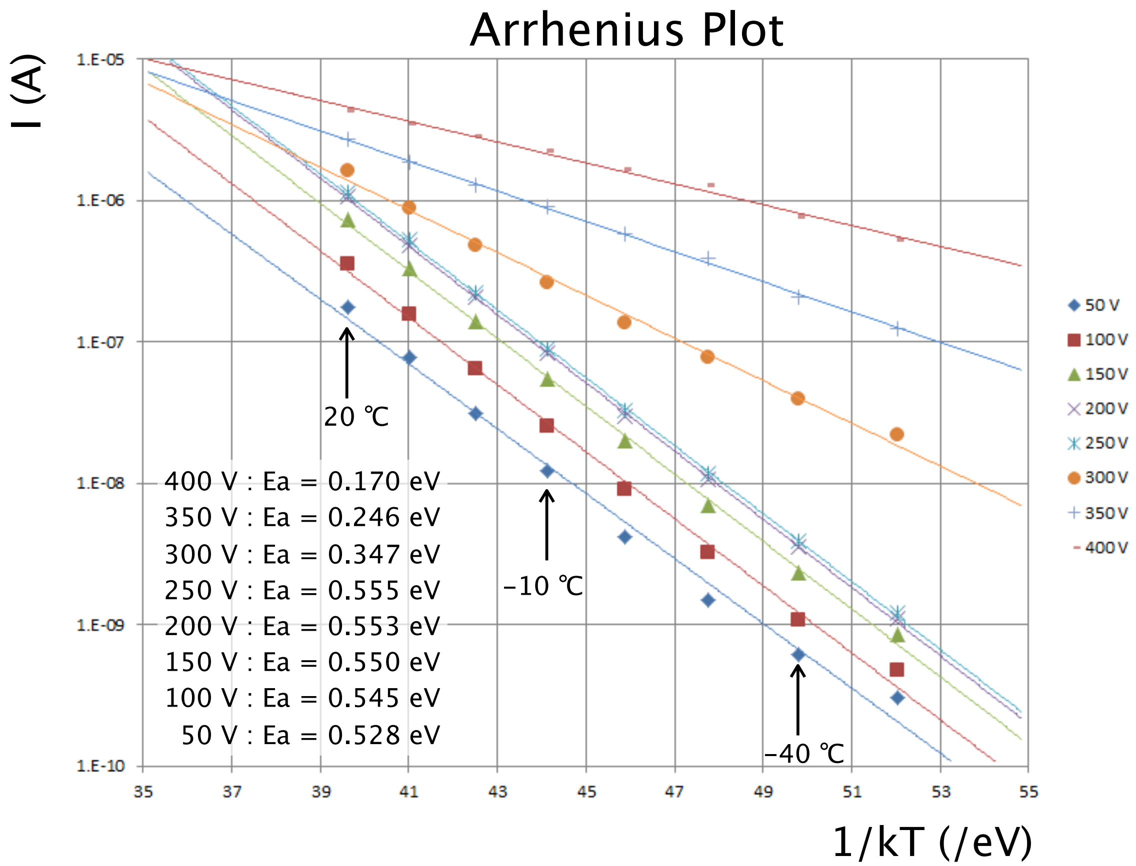


Figure A.2: Arrhenius plot from Figure A.1.

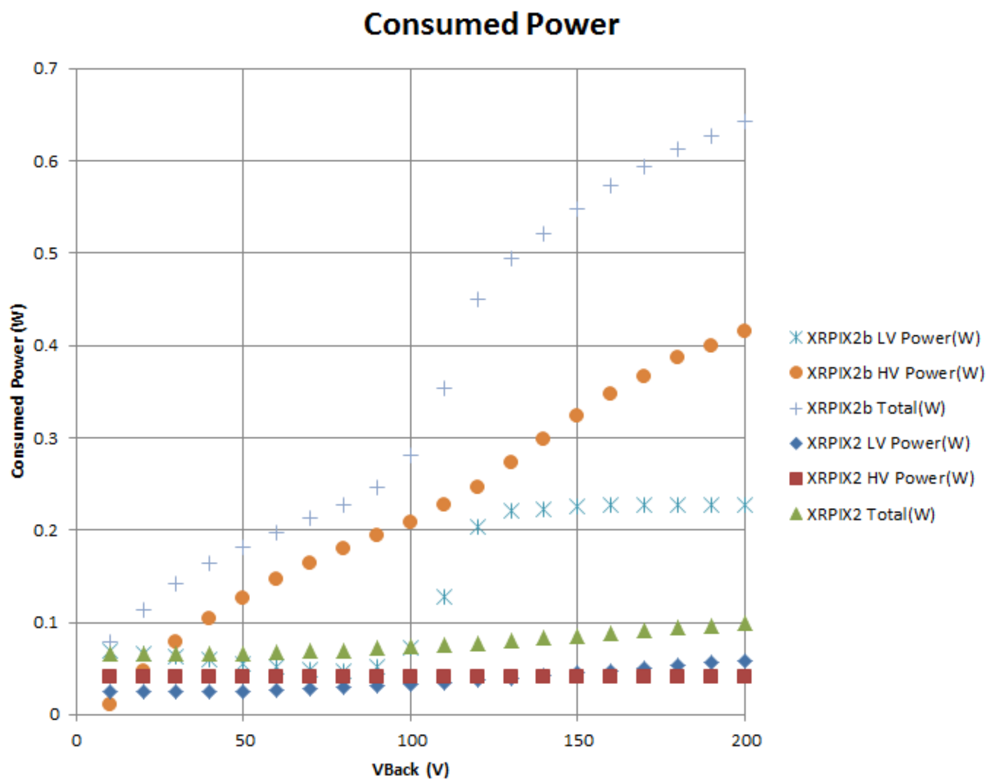


Figure A.3: Comsumed power measurement by comparison with XRPIX2.

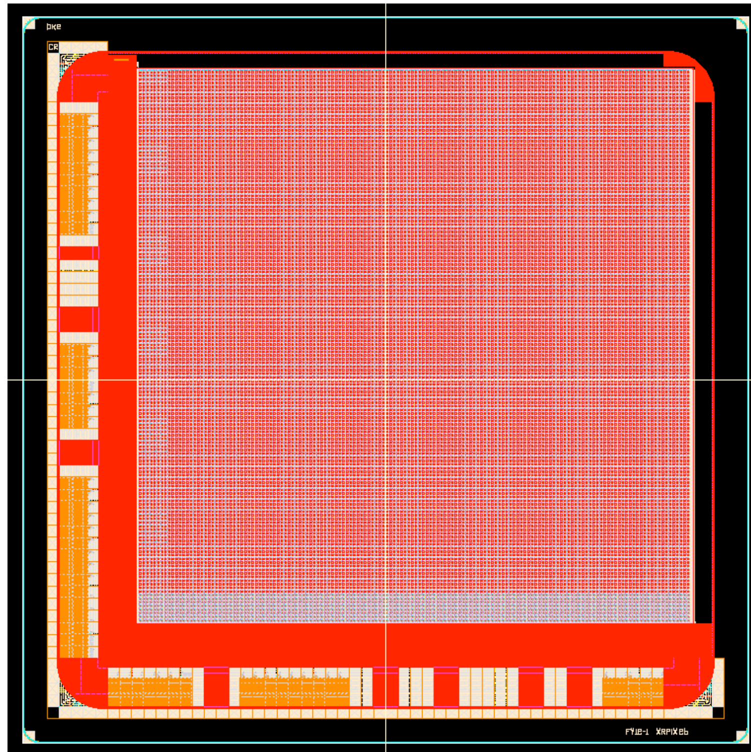


Figure A.4: Layout design of XRPIX2b. BPW layer is applied red. This showed that there was no BPW layer in IO Buffer.

mistake. Therefore, the cause which disappeared is unknown. However, the increase in the consumed power to the back bias voltage of HV has been explained.

A.3 Sense-node Capacitance

From the gain obtained with the section 5.7.3, the capacitance of a sensor is calculable. The sense-node capacitance is calculated to

$$Q = CV \tag{A.1}$$

$$C = \frac{1.602 \times 10^{-19}}{(7.0 \times 10^{-6} / 0.95)} = 22 \text{ [fF]} \tag{A.2}$$

Q is elementary charge (i.e. 1.602×10^{-19} C), and V is the output voltage of 1 electron including the circuit gain 0.95. This value is the observed capacitance also containing the parasitic capacitance of transistors and wiring.