THESIS

Digital Low-Level RF Control System Development for International Linear Collider

国際リニアコライダーのためのデジタル低電力RF制御系の 開発

Sigit Basuki Wibowo

DOCTOR OF PHILOSOPHY

Department of Accelerator Science

School of High Energy Accelerator Science

The Graduate University for Advanced Studies

2017

Supervisor:	Prof. Toshihiro Matsumoto
Reviewer:	Prof. Takako Miura
	Prof. Shinichiro Michizono
	Prof. Tetsuya Kobayashi
	Prof. Fang Zhigao
	Prof. Takashi Ohshima

Day of submission: 9^{th} of June 2017

For:
my family

Abstract

The objective of this study is to develop an appropriate digital low-level radio frequency (LLRF) control system for the International Linear Collider (ILC). The ILC requires RF amplitude and phase stabilities of 0.07 % (RMS) and 0.35° (RMS), respectively. Feedback control will be used to meet the stability requirements.

The large size of ILC may cause issues for its subsystems, including the digital LLRF control system. One RF station is composed of one klystron for driving multiple cavities and operated with the feedback control of the vector sum of the cavities. However, one RF station spans approximately 60 m in length and the length of signal transmission to the controller board are different among the cavities. The different signal transmission delays among the cavities may contribute to the vector sum error and may affect the RF stability.

In digital LLRF control systems, a signal from a cavity is down-converted by a down-converter to obtain an intermediate frequency (IF) signal and then digitized by an analog-to-digital converter (ADC). In order to carry out the vector sum feedback control, the information of amplitude and phase of all cavities are required. In the case of the ILC LLRF, the large number of signals should be measured. It is said generally that one ADC is required to get the information of amplitude and phase from one cavity. However, it can be difficult to place a large number of ADCs on one board of a digital LLRF control system because of the limited number of field-programmable gate array (FPGA) pins that can be connected to ADCs. Even though a large FPGA is chosen to accommodate the large number of signals, it will be difficult to fabricate a board with a large number of FPGA pins because some pins may not connect to the board properly, leading to an unstable operation. Furthermore, other issues such as the need to handle a large number of cables, a cool the ADC chips, and handle a huge amount of data traffic also make a single board realization difficult.

For research and development toward ILC realization, a minimum setup for a digital LLRF control system for the ILC was demonstrated at the Superconducting RF Test Facility (STF) at the High Energy Accelerator Research Organization (KEK).

A Digital LLRF control system with a master–slave configuration is proposed to eliminate these problems. The slave controller calculates the partial vector sum of its corresponding cavities and sends the result through an optical communication link to the master controller, which performs the total vector sum calculation and control algorithm. By applying the master–slave configuration, the placement of the ADCs can be distributed over several slave boards. The transmission delay from the cavity to the controller board can also be kept the same for all the cavities by adjusting the delay time in the FPGA of the master controller. Furthermore, the use of a large FPGA can also be avoided. The achieved amplitude and phase stabilities are 0.006 % (RMS) and 0.027° (RMS), respectively, which fulfill the ILC requirements.

Another way to mitigate the large number of ADCs required in the ILC is by implementing an IF-mixture technique in which four intermediate frequency (IFs) are combined and fed to one ADC. This decreases the required number of ADCs by a factor of four. The achieved amplitude and phase stabilities are 0.006 % (RMS) and 0.046° (RMS), respectively, which fulfill the ILC requirements.

Additional errors in signal estimation, such as a temperature dependent drift, may be caused by the characteristics of the down-converter. To eliminate the down-converter, a direct sampling technique for signal monitoring is developed, and the performance is estimated.

In the ILC, the klystron will be operated near its saturation. Cavity detuning caused by the Lorentz force may increase the klystron power. To avoid this phenomenon, a filling on resonance technique is demonstrated.

The experiments conducted in the STF were successfully demonstrated the digital LLRF control system with master–slave and IF-mixture configurations. Based on these results, we propose two possible digital LLRF configurations for the ILC. The first configuration is the digital LLRF control system configuration with master–slave. In this configuration, one RF station is composed of ten digital LLRF slave boards and one master board that can be connected up to 140 signals. The second configuration is the digital LLRF control system configuration with master–slave and IF-mixture technique. This configuration is composed of two slave boards and one master board that can be connected up to 168 signal. Those two configurations can be used to realize one RF station in the ILC. However, the second configuration is more promising because of the lower number of digital LLRF board requirement in one RF station.

Contents

Chapter 1

Introduction

This chapter introduces the International Linear Collider (ILC) and the Superconducting RF Test Facility (STF) at the High Energy Accelerator Research Organization (KEK). Furthermore, the motivation and structure of this dissertation are also described.

1.1 International Linear Collider

Particle accelerator plays very important role in fundamental and applied research. The upcoming ILC is expected to extend studies using accelerators.The ILC is an electron-positron collider dedicated to investigating Higgs bosons and other new particles [1]. It will complement the the Linear Hadron Collider (LHC), a high energy proton–proton collider. Because the electrons and positrons are the elementary particles, experiments can be performed with higher precision than those performed using proton–proton collision.

A schematic of the ILC is shown in Figure 1.1. It consists of the following subsystems. A polarized electron source uses a photo-cathode DC gun. A polarized positron is obtained by a pair production from a high-energy photons, which is obtained by passing a high-energy main electron beam through an undulator. The damping rings for the electrons and positrons are housed in a common tunnel with circumference of 3.2 km. For the beam acceleration, two 11 km main linacs will be used. To bring the beams to the collision point, two 2.2 km beam-delivery systems will be installed [1].

To perform the precise experiments in the ILC, the high-quality beams are necessary. The beams are accelerated in the superconducting cavities by a radio frequency (RF) field generated by the klystron. Consequently, the beam stability depends directly on the RF stability. To maintain the RF stability, field programmable gate array (FPGA)-based digital low level RF (LLRF) sys-

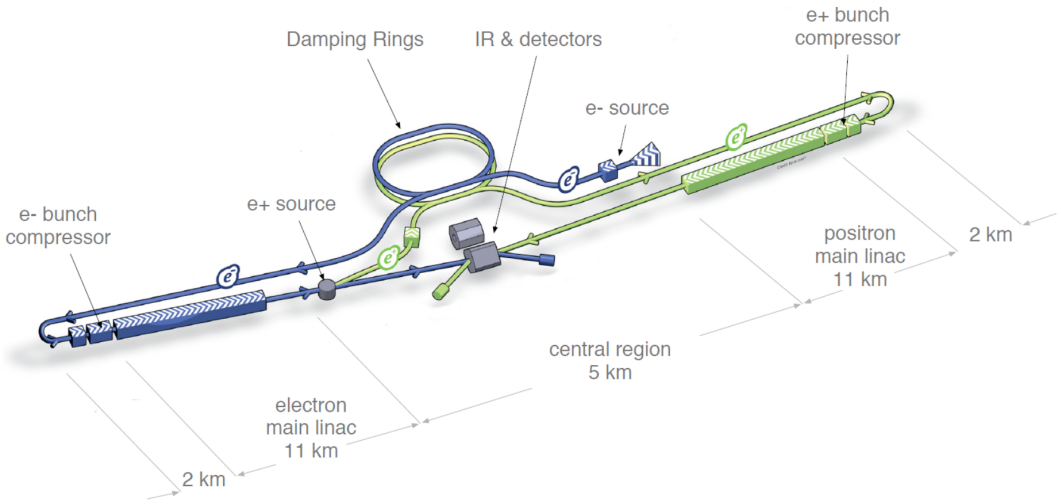


Figure 1.1: Layout of ILC showing all the major subsystems [1]. The total length is approximately 31 km.

tem with feedback control will be used. The RF amplitude and phase stability requirements are 0.07 % (RMS) and 0.35° (RMS), respectively. The RF parameters in the ILC include a frequency of 1.3 GHz, a gradient of 31.5 MV/m, pulsed mode operation with a 1.65 ms pulse duration, and a 5 Hz repetition rate [1]. The ILC consists of approximately 400 RF stations. One RF station spans approximately 60 m. It is composed of 39 cavities driven by one 10 MW multi-beam klystron (MBK).

Approximately 16,000 superconducting TESLA-like nine-cell cavities operating in pulsed mode will be installed in the main linacs of the ILC. A photograph of the cavity is shown in Figure 1.2. The cavities will be operated in RF π-mode at a resonant frequency of 1.3 GHz. The RF parameters of the cavity are summarized in Table 1.1. Two types of cryomodules for housing the cavities will be used to maintain a temperature of approximately 2 K. Type A cryomodule consists of nine nine-cell cavities. The type B cryomodule consists of eight nine-cell cavities and a superconducting quadrupole magnet in the middle, as shown in Figure 1.3. Both modules have the same length, 12.652 m. The main linac consists of 1,134 type A modules and 567 type B ones.

The RF power source used for the ILC is 10 MW L-band MBK with 65 % efficiency, 1.65 ms pulses, and a rate of up to 10 Hz [1]. The parameters of the klystron are summarized in Table 1.2. For the klystron modulator, an all solid-state Marx modulator will be used.

The horizontally mounted Toshiba klystron is one of the candidates for

Figure 1.2: A 1.3 GHz nine-cell superconducting cavity [1].

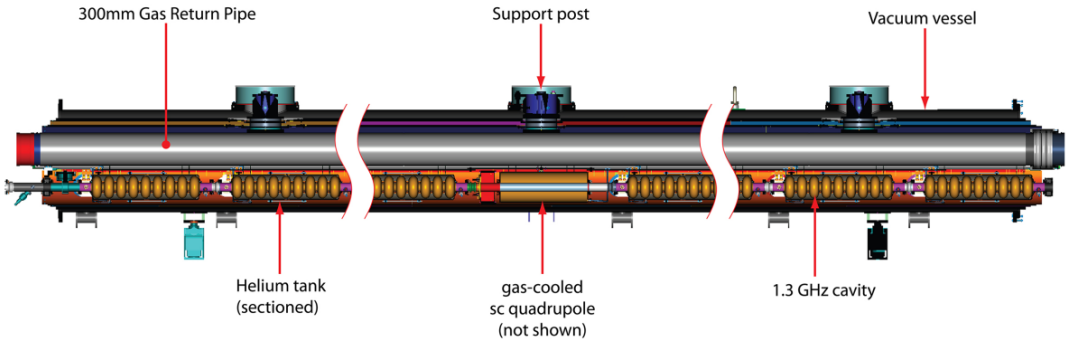


Figure 1.3: Type B cryomodule consists of eight cavities and a quadrupole in the middle. In the type A cryomodule, the superconducting cavity is installed instead of the quadrapole. [1]

Table 1.1: ILC main linac cavity and RF parameter.

Parameter	Value	Unit
Resonance frequency	1.3	GHz
Beam current	5.8	mA
Average accelerating gradient	31.5	MV/m
Q factor Q_0	$1 \cdot 10^{10}$	
Matched loaded Q (Q_L)	$5.5 \cdot 10^6$	
Matched driving power (P_k)	190	kW
Effective length	1.038	m
r/Q	1036	Ω
Accepted operational gradient spread	$\pm 20\%$	
Cavity fill time	923	μs
Cavity flattop time	727	μs
Total RF pulse length	1650	μs

Table 1.2: Parameters for 10 MW multibeam klystron

Parameters	Specification
Frequency	1.3 GHz
Peak power output	10 MW
RF pulse width	1.65 ms
Repetition rate	5.0 Hz
Average power output (5 Hz)	82.5 kW
Efficiency	65 %
Saturated gain	$>$ 47 dB
Instantaneous 1 dB BW	$>$ 3 MHz
Cathode voltage	$>$ 120 kV
Cathode current	$<$ 140 A
Filament voltage	9 V
Filament current	50 A
Power asymmetry (between two output windows)	$<$ 1 %
Lifetime	$>$ 40 000 hours

installation in the ILC. To improve the operation efficiency, the klystron in the ILC will be operated near its saturation level, so the LLRF overhead is only 7 % [1].

1.2 Superconducting RF Test Facility

The STF at KEK in Japan was built for the purpose of research and development for realization of the ILC. The cavity installed at the STF is operated with an RF of 1.3 GHz and a 5 Hz repetition rate. The STF is shown in Figure 1.4.

Several experiments were conducted during the STF construction, such as the S1-Global [2] and Quantum Beam [3] projects. The goal of the S1-Global cryomodule experiment was to operate at least one cryomodule with a 31.5 MV/m average gradient required for the ILC. However, the achieved average gradient was 26.0 MV m for seven cavities in simultaneous operation. This situation may be caused by the cavity assembly process or transportation [2].

The goal of the Quantum Beam experiment was to demonstrate the creation of high-brightness X-ray by inverse laser Compton-scattering. During this project, the normal conducting photocathode RF gun and two superconducting nine-cell cavities in the capture cryomodule (CCM) were installed. The superconducting cavities in the CCM were used for pre-acceleration of the electron

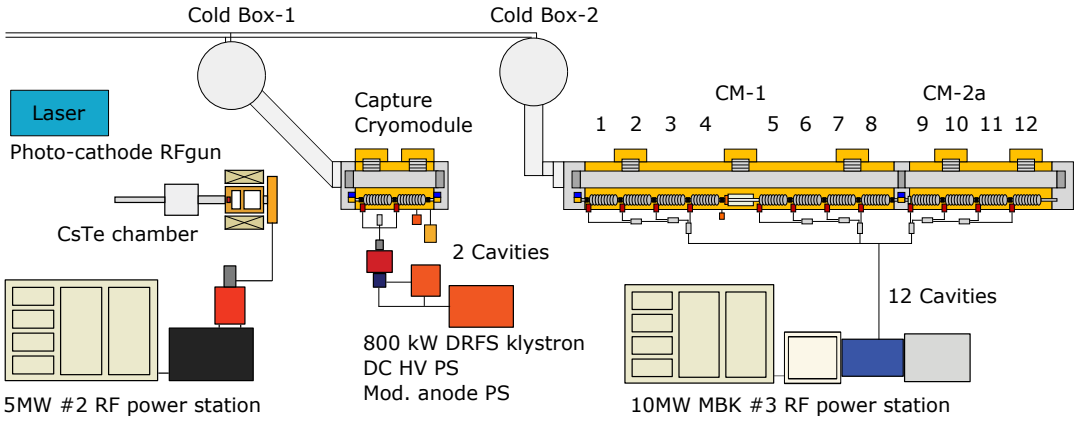


Figure 1.4: Layout of the STF. It consists of a normal conducting photo-cathode RF gun, two superconducting nine-cell cavities in the capture cryomodule, eight superconducting nine-cell cavities in the cryomodule CM-1, and four superconducting nine-cell cavities in the cryomodules CM-2a.

beam to 40 MeV. Both superconducting cavities were driven by one 800 kW klystron [3–5].

The main accelerator, which is composed of eight superconducting nine-cell cavities in cryomodules CM-1 and four superconducting nine-cell cavities in the cryomodules CM2-a, was constructed in 2013 and assembled in the STF tunnel in 2014. The length of cryomodules CM-1 and CM2-a are 12.652 m and 6.9 m, respectively [6, 7].

The experiment was conducted using only eight cavities (cavity #1, #2, #3, #4, #8, #10, #11, and #12) because the other four cavities (cavity #5 ,#6, #7, and #9) exhibited degraded performance [8].

To control the accelerating field of the two superconducting cavities in CCM, a digital LLRF control system that is compliant with MTCA.0 hardware was installed. To control the accelerating field of the 12 cavities in CM-1 and CM-2a, a digital LLRF control system that is compliant with MTCA.4 hardware was installed.

The planned accelerating beam train length was 0.9 ms in length with a 5.7 mA peak intensity and 2.7 MHz bunch repetition in a train with 5 Hz train repetition [6].

There are currently three RF sources at the STF. In the first station, a bouncer-type insulated gate bipolar transistor (IGBT) modulator is used. A 5 MW klystron, TH2104C, is used for RF gun operation [9]. The second source is an 800 kW pulsed klystron for driving two nine-cell superconducting cavities in the capture cryomodule. The third source is a 10 MW MBK, which was used

for the experiment described in this thesis. This klystron was used to drive two cryomodules, CM-1 and half-size cryomodule CM-2a.

In the STF, several digital LLRF control systems have also been developed. Detailed descriptions of these systems are presented in the chapters that covers each system.

1.3 Motivation

The motivation for this thesis is to propose an appropriate digital LLRF control system for the ILC that can satisfy the RF stability requirements of the ILC. To fulfill the requirements, we selected an FPGA-based digital LLRF system with feedback control.

The digital control system is preferable to an analog control system because it has several advantages, such as ease of data manipulation and flexibility of parameter adjustment. For example, in vector sum control, the summing process in digital control system is much simpler than that in analog control systems. Furthermore, during the development or operation, several changes in the parameters may be necessary. It is easier to change the parameters in a digital control system than in an analog control system.

Regarding the control system, this thesis considers two main issues. The first issue is the large size of the RF station. In the ILC, the multiple cavities are driven by one klystron. In this configuration, the RF control system has to control the vector sum of the accelerating fields of all the cavities. In the vector sum control, the difference in the signal transmission delay among the cavities may contribute to the vector sum error and may affect the RF stability.

The second issue is that a large number of signals must be measured. To ensure the stable operation of the ILC, parameters such as the cavity detuning must be monitored. To estimate the cavity detuning, signals from each cavity—the cavity field, the forward power, and the reflected power—must be measured. In the ILC, one RF station consists of 39 cavities. Thus, the total number signals to be measured is approximately 120. In a digital control system, an analog-to-digital converter (ADC) is necessary to convert the analog signals to digital signals. Each signal requires one ADC, but it is difficult to put all of the ADCs on one board because the number of the lines in the FPGA available for connect to ADCs is limited. Even though a large FPGA is chosen to accommodate the large number of signals, unstable operation may occur because of improper connection of some pins on the board.

A digital LLRF control system with a master–slave configuration is one of the solutions for the large system such as the ILC. One RF station is separated into subsystems consisting of master and slave digital LLRF controllers. By

distributing the controller over several slave boards, groups of a few cavities are connected to a slave board, so that the signal transmission delay time of the cavities in that group can be kept at the same value. Furthermore, the number of signals sent to a processor is reduced by using several slave boards, and the fabrication of one board with a large number of input channels can be avoided. In this configuration, the slave controller computes the partial cavity vector sum of the cavity signals in the cryomodules. The master controller computes the total vector sum from the signal sent from the slave controller and performs the amplitude and phase regulation, exception handling, and overall system coordination. Data transfer between the master and slave controllers uses an optical communication link. This involves the electrical to optical (E/O) and optical to electrical (O/E) conversion processes, which may introduce a delay in the control loop. This additional delay may affect the RF stability. This thesis also reports an investigation of the effect of the delay to confirm its effect on the RF stabilities.

The other way to resolve the issues is by implementing the an intermediate frequency (IF)-mixture technique. This technique uses different IFs that are combined by a passive combiner and read by only one ADC. In the digital signal processor (DSP), each IF signal can be decoded independently. Implementing this technique reduces the number of ADCs required for the system. This thesis explains the design and evaluation of the IF-mixture technique.

The thesis also considers is the characteristic of the down-converter, which may contribute to the error in the estimated signal. To mitigate this problem, the down-converter can be eliminated by implementing a direct sampling technique. Furthermore, the system becomes simpler when the local oscillator (LO) and down converter are removed. In the direct sampling technique, the signal from the cavity is sampled directly by a high speed and wide-bandwidth ADC. However, the high-frequency input of the ADC degrades the signal-to-noise ratio (SNR). The degradation can be ameliorated by implementing a digital filter. This thesis reports an experiment in which the direct sampling technique is implemented for signal monitoring.

In the ILC, the klystron is operated near its saturation level to achieve higher power efficiency. Because the ILC is operated in a pulsed mode, a finite time (filling time) is necessary for the cavity field to reach its designed gradient after power feeding. The required klystron power during the filling time depends on the cavity detuning due to the Lorentz force. To keep the klystron power from exceeding its saturation level, the cavity should be kept in resonance during the filling time by applying the filling on resonance method. This thesis reports the experiment using this method.

Two possible configurations of digital LLRF control systems are proposed

in this thesis. The first configuration is the digital LLRF control system with master–slave. The second configuration is the digital control system with mater–slave and IF-mixture technique. Both configurations can accommodate the number of signal to be measured in one RF station of the ILC. However, the second configuration is more interesting because of the lower number of digital LLRF board requirement for one RF station.

1.4 Structure of the Thesis

This thesis is structured into seven chapters. The followings are the short descriptions of each chapter.

- Chapter 2 describes the principle of the digital LLRF control system. The main components of the digital LLRF control system are alos described.
- Chapter 3 presents the digital LLRF control system with a master–slave configuration. This chapter covers the minimum setup of the digital LLRF control system for the ILC and considers the optical link delay consideration in the master–slave configuration.
- Chapter 4 explains the digital LLRF control system with an IF-mixture algorithm. In this chapter, the design and evaluation of this technique are explained in detail.
- Chapter 5 explains the direct sampling method used for signal monitoring. The use of a direct sampling method to detect two different signals with a common sampling frequency is also explained in this chapter.
- Chapter 6 details the methods of reducing the required klystron power during the filling time by implementing a filling on resonance method. Furthermore, the microphonics measurements are also reported in this chapter.
- Chapter 7 summarizes the thesis. The possible configurations of a digital LLRF control system for the ILC are also presented.

Chapter 2

Digital LLRF Control System Techniques

The principle of the digital LLRF technique is presented in this chapter. The main task of the digital LLRF control system is to regulate the amplitude and phase of the accelerating field. To perform that task, feedback control is necessary. The digital LLRF control system has advantage over analog control systems, such as ease of data manipulation and flexible parameter adjustment.

A simplified schematic of a digital LLRF control system configuration with N cavities is shown in Figure 2.1. The RF signal from the cavity is down-converted into an IF signal by mixing it with a signal from an LO. At the STF, frequencies of 1.3 GHz, 10 MHz, and 1.31 GHz are used for the RF the signal, IF, and LO signals, respectively. This down conversion process does not alter the amplitude and phase information of the RF signal. To remove unwanted frequencies from the mixer output, a low pass filter (LPF) is used. Then the analog signal is converted to a digital signal by an ADC. The signal is converted into *in-phase* (I) and *quadrature* (Q) components. The gain and phase offset of the I/Q signal is corrected by entering it into a rotation matrix, and then the vector-sum is computed. The signal is filtered by infinite impulse response (IIR) LPFs and subtracted from the set value to obtain the I/Q errors. These errors are fed to the controller. A feedback (FB) controller is applied to compensate for unpredictable disturbances. A feed-forward controller is applied to compensate for repetitive disturbances. The digital signal is converted into an analog signal by a digital-to-analog converter (DAC). The DAC output is then up-converted to a 1.3 GHz signal and used to drive the klystron.

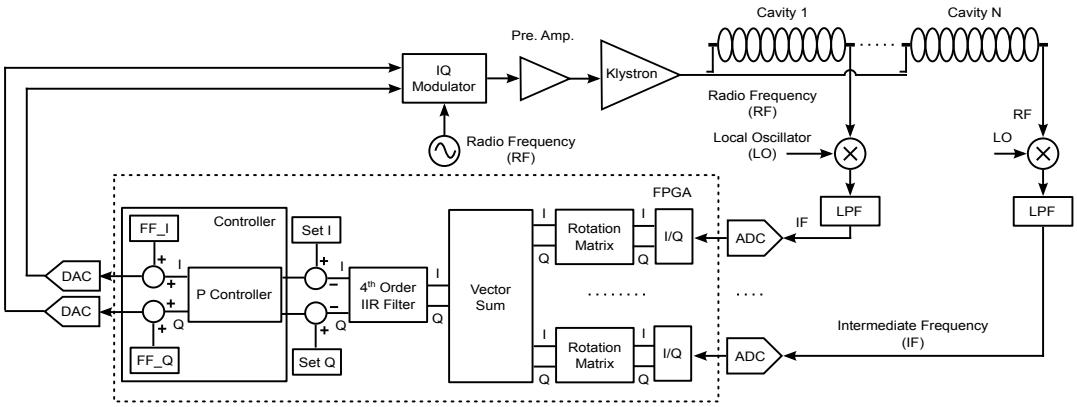


Figure 2.1: Simplified schematic of digital LLRF control system configuration with N cavities. Each component of the feedback loop is explained in the text.

2.1 Down Conversion

The ADC bandwidth is much lower than the RF; therefore a down-conversion process is necessary. Down-conversion is performed by mixing the input signal (RF) with an LO signal to obtain an IF signal which typically has a much lower frequency than the RF signal. Mathematically, the mixing process is multiplication in the time-domain.

In the STF, the RF frequency is 1.3 GHz, and the IF frequency is 10 MHz. To obtain this IF frequency, an LO signal of 1.310 GHz is required. The down conversion process is explained as follows. Suppose that the RF signal is represented as

$$\mathrm{RF} = A_{\mathrm{RF}} \cdot \cos(2\pi \cdot 1.30[\mathrm{GHz}]t + \phi_{\mathrm{RF}}) \tag{2.1}$$

where A_{RF} is the amplitude, and ϕ_{RF} is the phase. The LO signal is governed

$$\mathrm{LO} = A_{\mathrm{LO}} \cdot \cos(2\pi \cdot 1.31[\mathrm{GHz}]t + \phi_{\mathrm{LO}}) \tag{2.2}$$

where A_{LO} is the amplitude, ϕ_{LO} is the phase. Then, those two signals are mixed (multiplied) by mixer. A simplified down conversion schematic is shown in Figure 2.2. The output of the mixer is given by the following equations.

$$\begin{aligned} V_{\mathrm{OUT}} &= \mathrm{RF} \cdot \mathrm{LO} \\ &= A_{RF}A_{LO}\cos(2\pi 1.30[\mathrm{GHz}]t + \phi_{RF}) \cdot \cos(2\pi 1.31[\mathrm{GHz}]t + \phi_{LO}) \\ &= \frac{1}{2}A_{RF}A_{LO}\{\cos(2\pi 10[\mathrm{MHz}]t + (\phi_{LO} - \phi_{RF})) \\ &\quad + \cos(2\pi 2.61[\mathrm{GHz}]t + (\phi_{LO} + \phi_{RF}))\} \end{aligned} \tag{2.3}$$

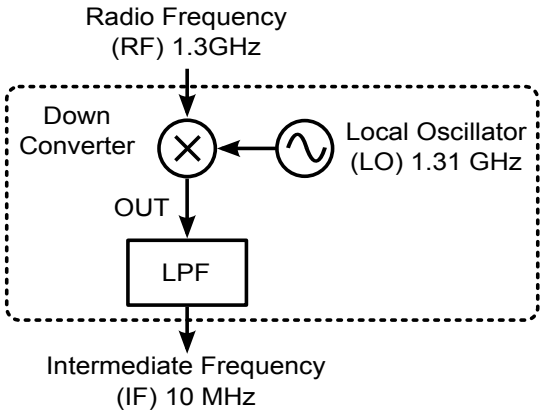


Figure 2.2: Simplified down conversion schematic. The process is actually multiplication of two inputs. The multiplication yields two frequencies, but only one frequency (the IF) is extracted by filtering the other frequency out.

Equation 2.3 shows that the output of the mixer contains 10 MHz and 2.61 GHz components. The 10 MHz signal is the desired IF signal. Therefore, to obtain the IF signal, an LPF of higher than 10 MHz is necessary. In the STF, the 10.7 MHz LPF from Mini-Circuits Company with a cut-off frequency of 14 MHz was used [10]. A simplified down conversion schematic is shown in Figure 2.2.

Even tough the frequency of the IF signal is much lower than that of the RF signal, the amplitude and phase information of the RF signal is still preserved in the IF signal. To extract the original amplitude and phase from the IF signal precisely, a stable LO signal is required.

The IF signal can be represented in polar coordinates (amplitude/phase representation) or in Cartesian coordinates. Suppose that a signal of $y(t) = A\cos(\omega t + \phi_0)$ has an amplitude A, angular frequency ω, and initial phase ϕ_0 and can be decomposed into its sine and cosine components using trigonometric functions [11]:

$$\begin{aligned} y(t) &= \underbrace{A\cos\phi_0}_{I}\cos(\omega t) - \underbrace{A\sin\phi_0}_{Q}\sin(\omega t) \\ &= I\cdot\cos\omega t - Q\cdot\sin\omega t \end{aligned} \tag{2.4}$$

The amplitudes of the cosine and sine components are defined as the *in-phase* component (I) and *quadrature-phase* component (Q), respectively. The signal representation in terms of I and Q is illustrated in Figure 2.3.

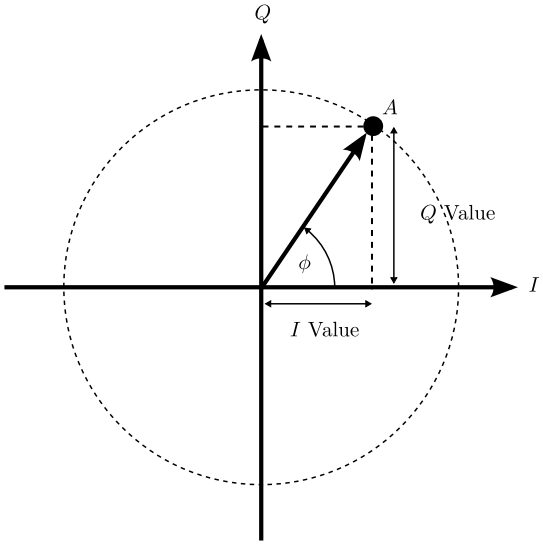


Figure 2.3: Representation of signal in the Cartesian coordinates. The symbol of A and ϕ are the amplitude and phase, respectively. The I component is the in-phase or real part and the Q component is the quadrature or imaginary part.

2.2 Digital Signal Processing

Digital signal processing is based on the FPGA. The FPGA can be configured using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) programming. Functions in the FPGA are implemented in modules. The main modules implemented for digital LLRF control are as follows.

- The I/Q conversion
- Rotation matrix
- Vector sum calculation
- Digital filter
- Controller

Those modules are discussed in more detail in the following subsections.

2.2.1 The I/Q conversion

The analog signal from the down-converter must be converted to digital before it can be processed by the DSP. The process of analog to digital con-

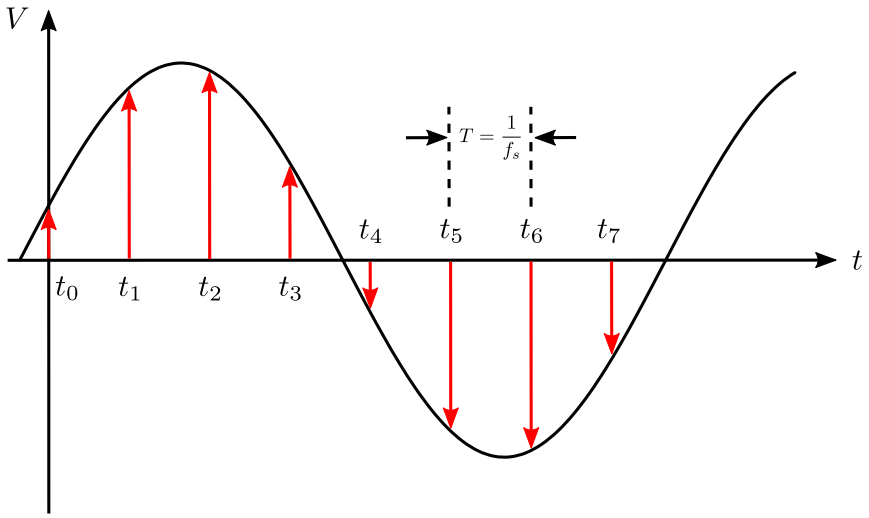


Figure 2.4: Concept of digitization of analog signal digitization. Analog signal is sampled at discrete interval with the same period T. Each sampled signal is then quantized.

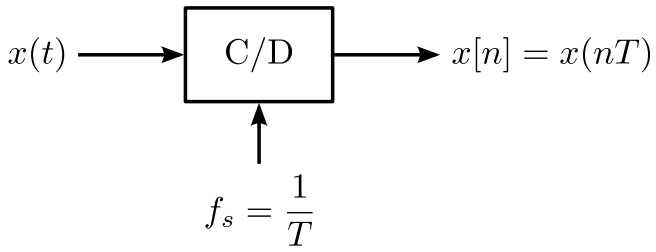


Figure 2.5: Continuous to discrete time converter block diagram.

version consists of two stages: *sampling* and followed by *quantization*. The concept of the process is illustrated in Figure 2.4. The analog signal (black line) is sampled by a pulse with the equal rate f_s. The signal is sampled by a continuous-to-discrete converter as illustrated in Figure 2.5. In the sampling process, the continuous signal is converted to a discrete time signal. The continuous signal $x(t)$ is sampled at a sampling frequency f_s, and the output is the sequence signal $x[n]$.

Sampling methods can be categorized as oversampling and undersampling methods. The relationship between the analog signal and sampling signal can

be written as

$$\frac{f_s}{f_{\text{IF}}} = \frac{L}{N} = m \tag{2.5}$$

where N and L are integers. If the sampling clock is higher than the Nyquist rate or $m > 2$, this technique is called oversampling. If the sampling clock is lower than the Nyquist rate, the technique is called undersampling. This method is implemented in a direct sampling technique in which the down conversion process is eliminated. The direct sampling technique is presented in Chapter 5.

Sampling is followed by quantization. In this process, the sampled data are mapped to discrete levels represented by a sequence of bits. Suppose the number of bits in the sequence B; then the number of quantization levels is 2^B. The value of B determines the ADC resolution. The quantization process introduces a small error that can be defined as.

$$e[n] = x[n] - x_{\text{Q}}[n] \tag{2.6}$$

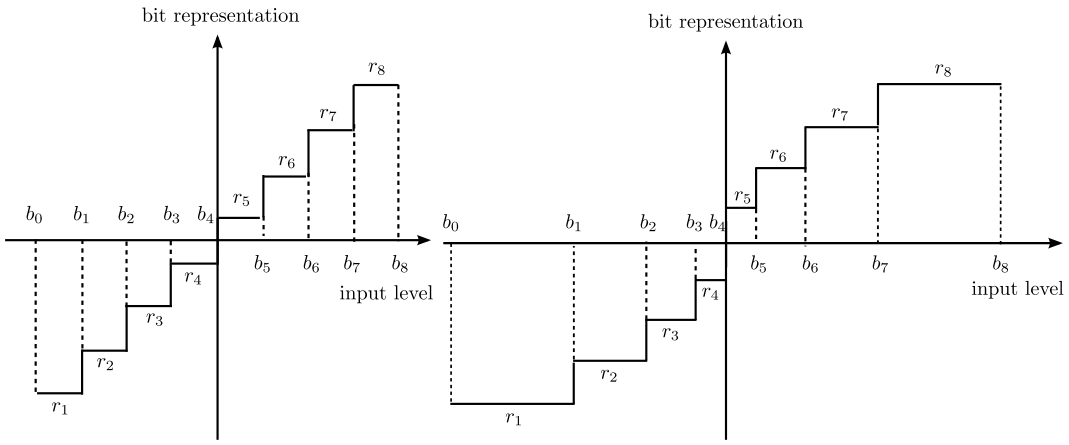
where $e[n]$ is the quantization error of the nth sampled, $x[n]$ is the real value of the nth sample, and $x_{\text{Q}}[n]$ is the quantized value of the nth sample. Quantization can be categorized as uniform or nonuniform. In the uniform quantization, the space of between two quantization levels is equal for all possible quantization levels. When the space is not equal, the process is called nonuniform quantization. Uniform and non-uniform quantization are illustrated in Figure 2.6. If the signal x is the input of quantizer that has amplitude between b_k and b_{k+1} then x is mapped to r_{k+1}, where b_k is the amplitude of input signal and r_k is the bit representation. In practical implementations, the sampling and quantization process are both performed in the ADC.

The ADC output is further processed for conversion to I and Q components. When the sampling rate (SR) and IF signal satisfy the condition $L \cdot \text{IF} = N \cdot \text{SR}$ and $L > N$ (where L and N are integers), the I and Q components of the sampled IF signal can be numerically calculated using the following equations [12, 13].

$$I = \frac{2}{L} \sum_{n=0}^{L-1} x[n] \cos\left(\frac{2\pi \cdot N}{L} \cdot n\right) \tag{2.7}$$

$$Q = \frac{2}{L} \sum_{n=0}^{L-1} x[n] \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \tag{2.8}$$

where $x[n]$ is the sampled signal.



(a) Uniform quantization mapping.

(b) Nonuniform quantization mapping.

Figure 2.6: Quantization mapping diagram. An input level b_k is mapped to bit representation r_k.

Different approaches to estimating the I and Q values can be applied in terms of the Fourier series. In Fourier series theory, we know that any periodic sequence can be represented as a sum of complex exponential sequences.

$$x(t) = \sum_{k=-\infty}^{\infty} c_k e^{j\omega kt} = \sum_{k=-\infty}^{\infty} c_k e^{\frac{j2\pi kt}{T}} \tag{2.9}$$

where $x(t)$ is the function of t that has frequency components at $\omega = 0, \pm\omega, \pm 2\omega, \cdots$ and c_k is the Fourier coefficient, which is a complex number.

Consider that the digitized signal $x[n]$ is periodic with period L, so that $x[n] = x[n + rL]$ for any integer values of n and r. The discrete Fourier transform is defined as the transformation of a sequence of L complex numbers $x[0], x[1], \cdots, x[L-1]$ into another sequence of complex numbers, $X[0], X[1], \cdots, X[L-1]$. This can be written as follows.

$$X[k] = \sum_{n=0}^{L-1} x[n] \cdot e^{j(2\pi k/L)n} \tag{2.10}$$

where $j = \sqrt{-1}$. Using the Euler formula $e^{j\theta} = \cos\theta + j\sin\theta$, Equation 2.10 can be written as

$$X[k] = \sum_{n=0}^{L-1} x[n] \cdot [\cos((2\pi k/L)n) + j\sin((2\pi k/L)n)]. \tag{2.11}$$

To find the coefficient of Equation 2.11, a Fourier series approximation can be performed. Recall that every signal can be represented as a Fourier series.

$$x(t) = \sum_{k=-\infty}^{\infty} c_k e^{j\omega kt} \tag{2.12}$$

The coefficient of c_k is a complex numbers. The Fourier series can be written as follows.

$$x(t) = a_0 + \sum_{k=1}^{\infty} [a_k \cos(\omega kt) + b_k \sin(\omega kt)] \tag{2.13}$$

The coefficients of the Fourier series are defined as follows.

$$a_0 = \frac{1}{2\pi} \int_{-\pi}^{\pi} x(t) \mathrm{d}t \tag{2.14}$$

$$a_k = \frac{1}{\pi} \int_{-\pi}^{\pi} x(t) \cdot \cos(\omega kt) \mathrm{d}t \tag{2.15}$$

$$b_k = \frac{1}{\pi} \int_{-\pi}^{\pi} x(t) \cdot \sin(\omega kt) \mathrm{d}t \tag{2.16}$$

The Fourier coefficient can be approximated by the Riemann sum. Let a close interval $[a, b]$ be partitioned by points $a < t_1 < t_2 < \cdots < t_{n-1} < b$ where the lengths of the resulting intervals between the points are denoted by $\Delta t_1, \Delta t_2, \ldots, \Delta t_n$. Let t_k^* be an arbitrary point in the k^{th} subinterval. Then the quantity

$$\sum_{k=1}^{n} x(t_k^*) \Delta t_k \tag{2.17}$$

is called the Reimann sum of the given function $x(t)$ and the partition Δt_k, and the value $\max \Delta t_k$ is called the mesh size of the partition.

Substituting the continuous signal $x(t)$ into the expression for $x[n]$, Equation 2.14 can be approximated by the left Riemann sum

$$a_0 = \frac{1}{2\pi} \sum_{n=0}^{L-1} x[n] \cdot \Delta t. \tag{2.18}$$

where Δt is the distance between samples. Thus, in one period of the sampled signal, $\Delta t = \frac{2\pi}{L}$. Then the approximation becomes the following.

$$\begin{aligned} a_0 &= \frac{1}{2\pi} \sum_{n=0}^{L-1} x[n] \cdot \frac{2\pi}{L} \\ &= \frac{1}{L} \sum_{n=0}^{L-1} x[n] \end{aligned} \tag{2.19}$$

In Equation 2.15, consider $\omega_k = 2\pi f_k$ with $f_k = \frac{N}{L} \cdot f_s$, where f_k is the frequency of the signal to be sampled, f_s is the sampling frequency, and N and L are integer values. Thus, an approach similar to that implemented for approximating a_0 can be applied for the coefficients a_k and b_k as follows.

$$\begin{aligned} a_k &= \frac{1}{\pi} \sum_{n=0}^{L-1} x[n] \cdot \cos\left(\frac{2\pi \cdot N}{L} \cdot n\right) \cdot \Delta t \\ &= \frac{1}{\pi} \sum_{n=0}^{L-1} x[n] \cdot \cos\left(\frac{2\pi \cdot N}{L} \cdot n\right) \cdot \frac{2\pi}{L} \\ &= \frac{2}{L} \sum_{n=0}^{L-1} x[n] \cdot \cos\left(\frac{2\pi \cdot N}{L} \cdot n\right) \end{aligned} \tag{2.20}$$

$$\begin{aligned} b_k &= \frac{1}{\pi} \sum_{n=0}^{L-1} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \cdot \Delta t \\ &= \frac{1}{\pi} \sum_{n=0}^{L-1} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \cdot \frac{2\pi}{L} \\ &= \frac{2}{L} \sum_{n=0}^{L-1} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \end{aligned} \tag{2.21}$$

In Equation 2.19, a_0 is the direct current (DC) offset of the signal $x[n]$. The a_k and b_k values in Equation 2.20 and 2.21, respectively, are the in-phase (I) and quadrature (Q) components of $x[n]$. To minimize the processing delay of single values of I and Q, moving window averaging is adopted. This means that the I and Q values are updated every time new sampled data are available. This can reduce the latency of data updating. The averaging effect of this technique can also reduce the ADC noise.

In the moving window averaging technique, when the new data arrive, the oldest data are removed. I_k is the average value of I at time $t = k$. Suppose that at time $t = 0$, eight values are available and are averaged ($L = 8, N = 1$). For example, at the time $t = 1$ the new data point x_8 arrives, and the old data

point x_0 is removed. The technique is expressed as follows.

$$
\begin{aligned}
t = 0 \rightarrow I_0 &= \frac{2}{L} \sum_{n=0}^{7} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \\
t = 1 \rightarrow I_1 &= \frac{2}{L} \sum_{n=1}^{8} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \\
&= \frac{2}{L} \left[\left(\sum_{0}^{7} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) - x[0] \cdot \sin(0) + x[8] \cdot \sin(2\pi)\right)\right] \\
t = 2 \rightarrow I_2 &= \frac{2}{L} \sum_{n=2}^{9} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) \\
&= \frac{2}{L} \left[\left(\sum_{1}^{8} x[n] \cdot \sin\left(\frac{2\pi \cdot N}{L} \cdot n\right) - x[1] \cdot \sin(\pi/4) + x[9] \cdot \sin(9\pi/4)\right)\right] \\
&\vdots
\end{aligned}
\tag{2.22}
$$

There are two considerations in implementing the I/Q conversion algorithm in the FPGA. The first consideration is the term $\left(\frac{2}{L}\right)$. If the relation of $\left(\frac{2}{L}\right) = \frac{1}{2^K}$ holds, where L and K are integers, the calculation can be performed by a K-bit right-shift. If the term $\left(\frac{2}{L}\right)$ cannot be expressed as $\frac{1}{2^K}$, the approximation can be performed as follows.

$$
\frac{2}{L} = \frac{1}{2^{n_1}} + \frac{1}{2^{n_2}} + \frac{1}{2^{n_3}} + \cdots + \frac{1}{2^{n_k}} \tag{2.23}
$$

where L, M, n_1, n_2, n_3, and n_k are integers. The values of k and $n_1 \cdots n_k$ are chosen to obtain the value closest to $2/L$. For example, to approximate $1/9 = 0.1111\ldots$, value of $n_1 = 4$, $n_2 = 5$, $n_3 = 6$, and $n_4 = 9$ can be chosen. The approximation result is as follows.

$$
\begin{aligned}
\frac{1}{9} &\approx \frac{1}{2^4} + \frac{1}{2^5} + \frac{1}{2^6} + \frac{1}{2^9} \\
&\approx 0.1113
\end{aligned}
$$

The second consideration is the calculation of the value of the sine/cosine coefficient. For fast operation and simple design of the FPGA, the sine and cosine coefficients are not calculated in real time; instead, they are obtained from a look-up table (LUT). Fortunately, in this algorithm, the sine/cosine coefficients are fixed. Therefore, the FPGA resources used for the LUT are not large because only a small number of sines and cosines must be saved.

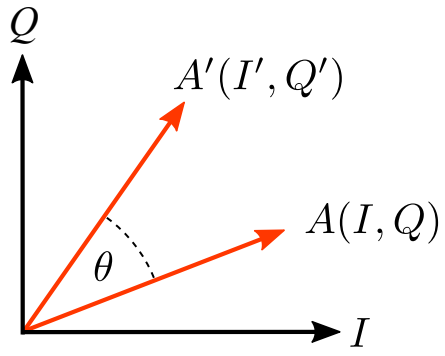


Figure 2.7: Vector A is rotated by θ

2.2.2 Rotation matrix

To operate the control system properly, it is necessary to calibrate the signal (amplitude and phase) before feedback control is activated. As the signal is presented as I and Q values, the gain and phase adjustment can be calibrated by applying a rotation matrix. Consider the vector A illustrated in Figure 2.7, which is rotated in the counterclockwise direction by an angle θ. Then

$$R(\theta) = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \tag{2.24}$$

so

$$A' = R(\theta)A \tag{2.25}$$

Thus, the new I and Q values can be obtained as

$$\begin{bmatrix} I' \\ Q' \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix}. \tag{2.26}$$

After the I and Q signals are calibrated by the rotation matrix, the signals from all the cavities are then summed and divided by the value according to the number of cavities to be summed. In the implementation, because the signal calibration is done only once, the sine and cosine coefficient are calculated outside of the FPGA. This can simplify the system and also conserve FPGA resource.

2.2.3 Vector sum calculation

In this module, all the signals are summed and divided by the number of cavities. This calculation is applied independently to both I and Q components

as follows.

$$I_{\mathrm{vs}} = \frac{1}{N}\sum_{i=1}^{N} I_i \tag{2.27}$$

$$Q_{\mathrm{vs}} = \frac{1}{N}\sum_{i=1}^{N} Q_i \tag{2.28}$$

where N is the number of cavities, I_i is the I component of the ith cavity, Q_i is the Q component of the ith cavity, I_{vs} is the vector sum of the I components, and Q_{vs} is the vector sum of Q components. In the FPGA, this division was implemented using multiplication and a bit-shift as follows.

$$I_{\mathrm{vs}} = \left(\frac{1}{2^{12}}\right)\cdot\left(\frac{2^{12}}{N}\right)\cdot\sum_{i=1}^{N} I_i.$$

$$Q_{\mathrm{vs}} = \left(\frac{1}{2^{12}}\right)\cdot\left(\frac{2^{12}}{N}\right)\cdot\sum_{i=1}^{N} Q_i.$$

The multiplication with by the first term on the right-hand side, $\left(\frac{1}{2^{12}}\right)$, was implemented by a 12-bit right-shift. The term $\left(\frac{2^{12}}{N}\right)$ was implemented by the LUT of the closest integer value. For example, for $N = 5$ the real value of the second term is $\left(\frac{2^{12}}{5}\right) = 819.2$. Thus, the value of 819 was chosen. The second and third terms on the right-hand side were multiplied by the DSP provided by the FPGA.

2.2.4 Digital filter

In the digital LLRF control system, the plant is the cavity in which the beams are accelerated by the RF field. A TESLA-like nine-cell cavity will be used in the ILC. The cavity has nine normal modes, called pass band modes. Only the highest mode (1.3 GHz) is used for beam acceleration. This mode is called the π-mode and the other modes are called parasitic modes. The parasitic modes limit the feedback gain and can be suppressed by a digital filter. Furthermore, the digital filter can also reduce the influence of the clock jitter.

The digital filter is a discrete time, discrete amplitude convolver. Linear convolution of two sequences in the time domain is the same as multiplication of two corresponding spectral sequences in the frequency domain. Digital filters can typically be categorized as finite impulse response (FIR) and infinite inpulse response (IIR) filters.

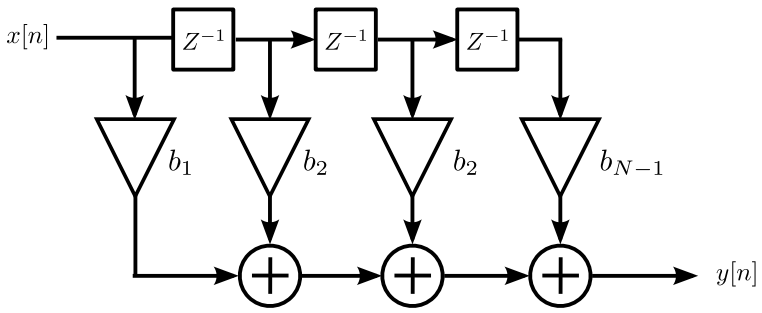


Figure 2.8: Representation of equation 2.29

Filters can be constructed from a combination of linear elementary operations: the gain, adder, and unit delay. The linear difference equation of the FIR can be written as follows.

$$y[n] = \sum_{k=0}^{M} b_k \cdot x[n-k] \tag{2.29}$$

where $x[n]$ is the input signal, $y[n]$ is the output signal, b_k is the filter coefficient, and M is the order of the filter. Equation 2.29 is illustrated in the diagram in Figure 2.8. If the delayed output is added to the input signals, the filter becomes an IIR filter. The linear difference equation of the IIR filter can be written as follows.

$$y[n] = \sum_{k=0}^{M} a_k \cdot x[n-k] + \sum_{k=1}^{N} b_k \cdot y[n-k] \tag{2.30}$$

where a_k is the filter coefficient and N is the filter order. Equation 2.30 is illustrated in the diagram in Figure 2.9.

The digital IIR filter was used in the digital LLRF control system at the STF. The first-order pole position is shown on the left side of Figure 2.10. From the figure, the transfer function can be written as follows.

$$\begin{aligned} H(z) &= \frac{\alpha}{z-(1-\alpha)} \\ &= \frac{\alpha z^{-1}}{1-(1-\alpha)z^{-1}} \end{aligned} \tag{2.31}$$

The corresponding difference equation can be written as follows.

$$y[n] = \alpha \cdot x[n-1] + (1-\alpha) \cdot y[n-1], \alpha \ll 1 \tag{2.32}$$

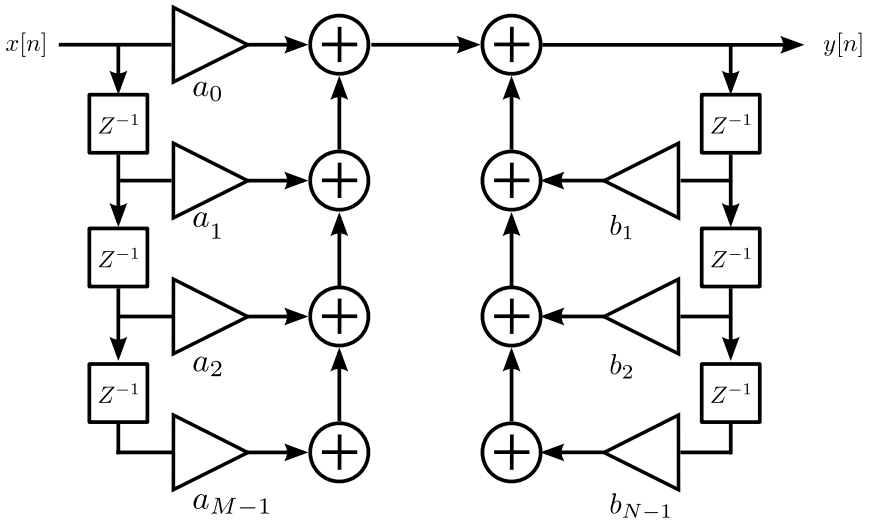


Figure 2.9: Representation of equation 2.30

where α is a parameter that defines the filter bandwidth as shown on left side of Figure 2.10. The filter bandwidth $f_{1/2}$ is defined as

$$f_{1/2} = \frac{\alpha}{2\pi} \cdot f_{\mathrm{s}} \tag{2.33}$$

where f_{s} is the sampling frequency. This bandwidth definition holds only for a single first-order IIR filter. In the first order low-pass IIR digital filter, the number of poles is always one, even if several filters are cascaded. To increase steepness of the filter slope, the number of poles can be increased. To maintain a real filter coefficient, the poles must either be real (lie on the positive or negative real axis) or occur in complex conjugate pairs [14]. The pole-zero plot of the conjugate-poles filter is shown on the right side of Figure 2.10. According to the poles position, the transfer function of the conjugate-poles IIR filter is given by.

$$\begin{aligned} H(z) &= \frac{2\alpha^2}{[z-(1-\alpha)+j\alpha]\cdot[z-(1-\alpha)-j\alpha]} \\ &= \frac{2\alpha^2 z^{-2}}{1-2(1-\alpha)z^{-1}+[(1-\alpha)^2+\alpha^2]z^{-2}} \end{aligned} \tag{2.34}$$

The corresponding difference equation can be written as following.

$$y[n] = 2\alpha^2 \cdot x[n-2] + a_1 \cdot y[n-1] + a_2 \cdot y[n-2] \tag{2.35}$$

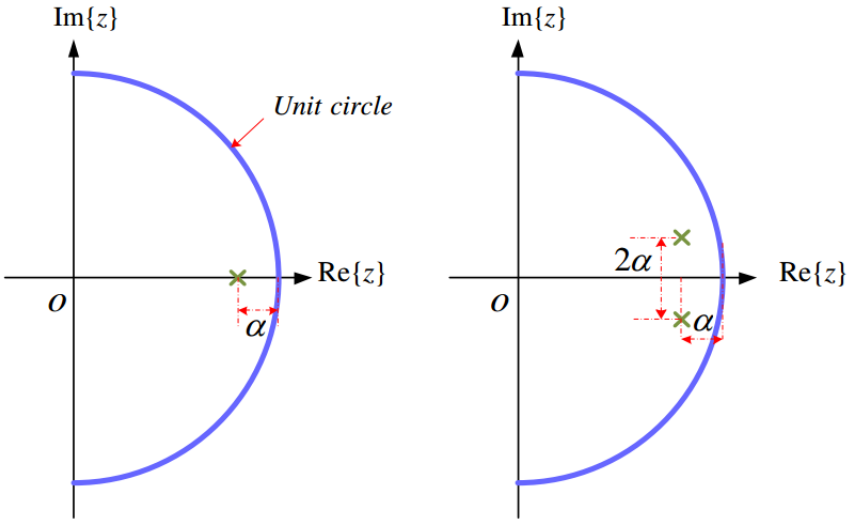


Figure 2.10: Poles-zero plot of first order digital IIR filter (left) and conjugate pole filter (right) [14].

where $a_1 = -2(1-\alpha)$ and $a_2 = (1-\alpha)^2 + \alpha^2$. The bandwidth of the filter is defined as

$$f_{1/2} = \frac{\sqrt{2} \cdot \alpha}{2\pi} \cdot f_s \tag{2.36}$$

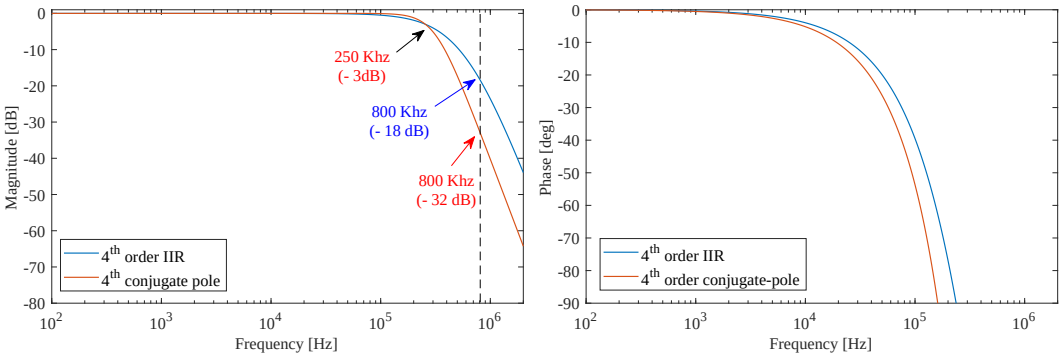
This bandwidth definition holds only for a single conjugate filter.

Figure 2.11 shows a Bode plot diagram comparing the fourth-order IIR filter (four first-order IIR filters connected in series) and the fourth-order conjugate-pole IIR filter (two second-order conjugate-pole filters connected in series). The conjugate-pole filter can provide a steeper slope than the first-order IIR filter. The achieved attenuation values of the $8\pi/9$-mode ($\approx 800\,\text{kHz}$) are approximately 18 dB and 32 dB for the first-order IIR and conjugate-pole filters, respectively. Compared to the first-order digital IIR filter, the conjugate filter has a better roll-off property. In the experiment, two conjugate-pole filters connected in series are used.

2.2.5 Controller

This section explains part of the control theory. The goal of the controller in the digital LLRF system is to regulate the amplitude and phase of the accelerating fields.

Controllers can generally be categorized as open-loop or closed-loop controllers. A diagram of an open-loop control system is shown in Figure 2.12. In



(a) (b)

Figure 2.11: Comparison of fourth-order IIR filter (four first-order IIR filters connected in series) and fourth-order conjugate-pole IIR filter (two second-order conjugate-pole filters connected in series). The bandwidth of both filters was set to 250 kHz.

the open-loop control system, the actions of the controller do not depend on the output value of the plant. Once the reference r is set, the controller output u always gives the same value. Therefore, in this system, a disturbance d cannot be compensated by the controller.

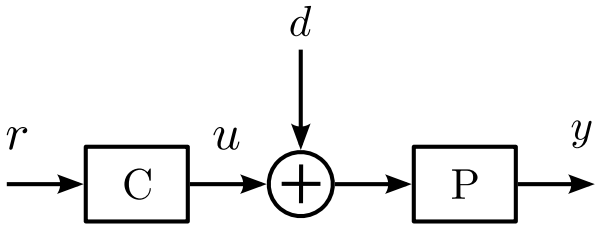


Figure 2.12: Open-loop control system. C is the controller, and P is the plant.

In closed-loop control, the control action depends on the process output. This type of control system can follow the reference signal and minimize the effect of disturbances. A basic closed-loop control system with feedback is shown in Figure 2.13. The r value is the set value that the controller will follow. The reference is subtracted from the plant output y to obtain the error e and provide the input to the controller C. Thus, the relation $e = r - y$ holds. The controller output u is used to control the plant P. A disturbance d and noise n exist in the control loop.

A well-known closed-loop control structure is the proportional–integral–derivative (PID) controller. The PID controller algorithm is governed by the

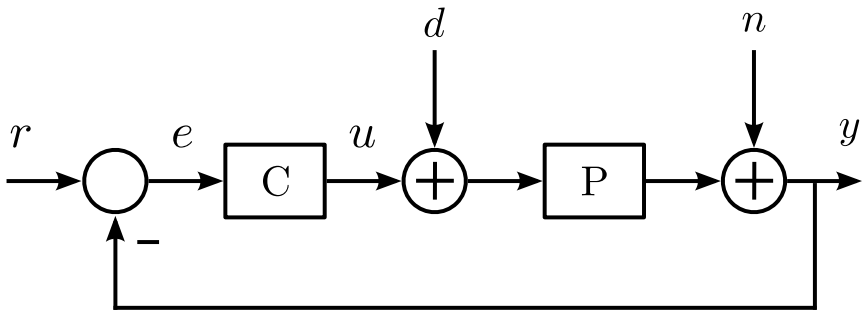


Figure 2.13: Basic closed-loop feedback control system. C is the controller, and P is the plant.

following equation.

$$u(t) = K\left(e(t) + \frac{1}{T_\mathrm{i}}\int_0^t e(\tau)\,\mathrm{d}\tau + T_\mathrm{d}\frac{\mathrm{d}e(t)}{\mathrm{d}t}\right) \tag{2.37}$$

where u is the controller output, e is the error obtained by subtracting the reference from the plant output, K is the gain, T_i is the integral time, and T_d is the derivative time. The controller output is the sum of the P (proportional), I (integral), and D (derivative) terms.

The proportional or P-controller yields an output that is proportional to the current error. An error e always exists in a P-controller. This error can be reduced by increasing the proportional gain of K. However, too much gain can make the system unstable. The integral or I-controller can reduce this error. It integrates the error over a period of time until the error value reaches zero. The action of the integral controller increases as the integral time T_i decreases. The possibility of oscillation also increases as the integral time T_i decreases. The derivative or D-controller anticipates the future behavior of the error. It is used to provide a damping effect, which increases as the derivative time T_d increases.

At the STF, a PI-controller was implemented in the digital LLRF control system. However, during operation, only the P controller is used. The loaded quality factor Q_L (see section 2.3.1) of the superconducting cavity is very high, so the cavity response is very slow. In the slow response of the plant, integral control will not reduce the error significantly. Furthermore, the addition of integral control also increases the complexity of the controller tuning process. During a tuning process, we must adjust the parameters of a feed-forward controller, which is used to reduce the error in the proportional controller. Figure 2.14 shows a diagram of a proportional and feed-forward control system.

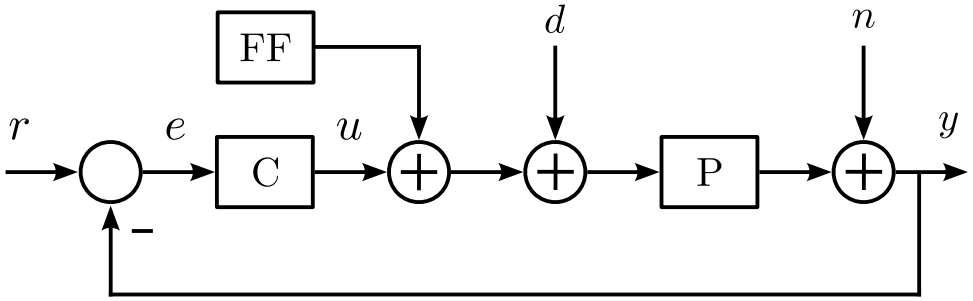


Figure 2.14: Proportional and feedforward control system. FF is feedforward controller, C is proportional controller. and P is the plant.

2.3 RF Cavity

From the viewpoint of the control loop, the cavity is the plant to be regulated. The beam is accelerated by the accelerating field in the cavity. The amplitude and phase of the accelerating field are the parameters to be controlled. The following subsections explain the RF cavity in more detail.

2.3.1 Cavity Equation

The TESLA-like cavity is a nine-cell cavity composed of nine single-cell cavities magnetically coupled. This structure implies that the cavity has nine normal modes, which are called passband modes. The cavity working mode is called the π mode; in this mode, the phase difference between consecutive cells is 180°. The coupling of the generator and beam to the equivalent resistor–inductor–capacitance (RLC) circuit of the cavity is shown in.

As a resonance device, the cavity is characterized by the quality factor Q. The quality factor of the cavity is a dimensionless parameter that indicates the energy losses within the cavity and is defined as

$$Q = 2\pi \cdot \frac{\text{stored energy in cavity}}{\text{dissipated energy per cycle}} = \frac{2\pi f_0 W}{P_{\text{diss}}} \tag{2.38}$$

where W is the stored energy, f_0 is the resonance frequency, and P_{diss} is the dissipated power. Three quality factor terms can be used to describe the cavity: the unloaded, loaded, and external quality factors. For the unloaded quality factor Q_0, only losses in the cavity walls caused by the RF surface resistance are taken into account. If the losses extracted through the power coupler and dissipated in the external load are considered, they appear in the external quality factor Q_{ext}. Finally, if both losses are considered, the loaded quality

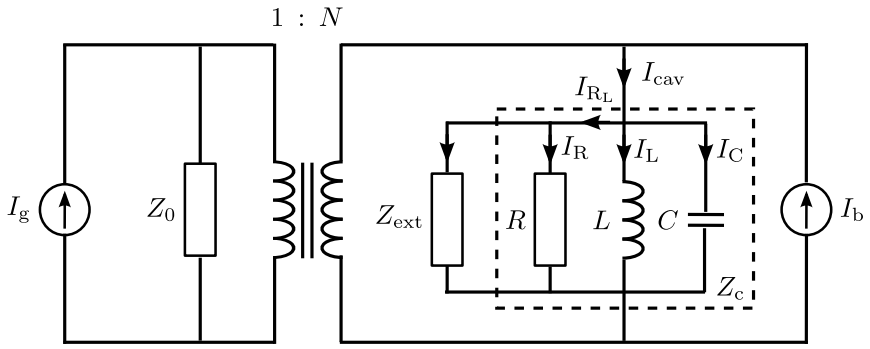


Figure 2.15: Equivalent circuit of cavity coupled to generator and beam.

factor Q_{L} is determined. The relationship among those quality factors can be written as

$$\frac{1}{Q_{\mathrm{L}}} = \frac{1}{Q_0} + \frac{1}{Q_{\mathrm{ext}}}. \tag{2.39}$$

For superconducting cavity, the approximation of $Q_{\mathrm{L}} \approx Q_{\mathrm{ext}}$ holds because typically Q_0 is much larger than Q_{ext}.

The equivalent circuit of the cavity is a parallel RLC circuit (in the dashed box) as shown in Figure 2.15. The notation of Z_0 and Z_{ext} are also introduced. The Z_0 is the transmission line impedance at the generator side and the Z_{ext} is the transmission line impedance seen from the cavity side. So the relation of those two notations is as follows.

$$Z_{\mathrm{ext}} = N^2 Z_0 \tag{2.40}$$

where N is the transformation ratio. The loaded shunt impedance R_{L} is introduced as the total parallel resistance of the cavity resistance R and the external impedance Z_{ext} as follows.

$$\frac{1}{R_{\mathrm{L}}} = \frac{1}{Z_{\mathrm{ext}}} + \frac{1}{R} \tag{2.41}$$

Therefore, the Kirchhoff current laws can be applied:

$$I_{R_{\mathrm{L}}} + I_L + I_C = I_{\mathrm{cav}} \tag{2.42}$$

where $I_{R_{\mathrm{L}}}$ is the current that flows through R_L, I_{L} is the current that flows through L, I_{C} is the current that flows through C, and I_{cav} is the total current that flows through the cavity and impedance Z_{ext}. Equation 2.42 can be rewritten in terms of the voltage as follows.

$$\frac{1}{R_{\mathrm{L}}} V_{\mathrm{cav}}(t) + \frac{1}{L}\int V_{\mathrm{cav}}(t)\,\mathrm{d}t + C\frac{\mathrm{d}V_{\mathrm{cav}}(t)}{\mathrm{d}t} = I_{\mathrm{cav}}(t) \tag{2.43}$$

where V_{cav} is the cavity voltage, R_{L} is the loaded shunt impedance, L is the inductance, and C is the capacitance. To obtain the differential equation, the integral can be eliminated by taking the derivative of Equation 2.43.

$$\frac{1}{R_{\mathrm{L}}}\frac{\mathrm{d}V_{\mathrm{cav}}(t)}{\mathrm{d}t} + \frac{1}{L}V_{\mathrm{cav}}(t) + C\frac{\mathrm{d}^2V_{\mathrm{cav}}(t)}{\mathrm{d}t^2} = \frac{\mathrm{d}I_{\mathrm{cav}}(t)}{\mathrm{d}t} \tag{2.44}$$

Then we divide Equation 2.44 by C, and the differential equation for the cavity is written as

$$\frac{\mathrm{d}^2V_{\mathrm{cav}}(t)}{\mathrm{d}t^2} + \frac{1}{R_{\mathrm{L}}C}\frac{\mathrm{d}V_{\mathrm{cav}}(t)}{\mathrm{d}t} + \frac{1}{LC}V_{\mathrm{cav}}(t) = \frac{1}{C}\frac{\mathrm{d}I_{\mathrm{cav}}(t)}{\mathrm{d}t} \tag{2.45}$$

By using the definitions $\frac{1}{R_{\mathrm{L}}C} = \frac{\omega_0}{Q_{\mathrm{L}}}$ and $\frac{1}{LC} = \omega_0^2$, where ω_0 is the resonance frequency of RLC circuit, Equation 2.45 can be rewritten as

$$\frac{\mathrm{d}^2V_{\mathrm{cav}}(t)}{\mathrm{d}t^2} + \frac{\omega_0}{Q_{\mathrm{L}}}\frac{\mathrm{d}V_{\mathrm{cav}}(t)}{\mathrm{d}t} + \omega_0^2V_{\mathrm{cav}}(t) = \frac{\omega_0}{Q_{\mathrm{L}}}R_{\mathrm{L}}\frac{\mathrm{d}I_{\mathrm{cav}}(t)}{\mathrm{d}t} \tag{2.46}$$

If we assume that the driving current I_{cav} is harmonic $[I_{\mathrm{cav}}(t) = \hat{I}_{\mathrm{cav}}\sin(\omega t)]$, the response of the cavity voltage V_{cav} will have the same oscillating angular frequency, $(V_{\mathrm{cav}}(t) = \hat{V}_{\mathrm{cav}}\sin(\omega t + \psi)$. The angle ψ is the angle between the voltage V_{cav} and the driving current I_{cav}, and it is defined as the tuning angle of the cavity. The equation 2.46 is an inhomogeneous second order differential equation. The particular solution or the stationary solution of Equation 2.46 is

$$\hat{V}_{\mathrm{cav}} = \frac{R_{\mathrm{L}}\hat{I}_{\mathrm{cav}}}{\sqrt{1 + [R_{\mathrm{L}}\cdot(\frac{1}{\omega L} - \omega C)]^2}} \tag{2.47}$$

$$\psi = \tan^{-1}\left\{R_{\mathrm{L}}\cdot\left(\frac{1}{\omega L} - \omega C\right)\right\} \tag{2.48}$$

Equations 2.47 and 2.48 can be expressed in terms of the loaded quality factor Q_L assuming that the generator frequency ω is very close to the cavity resonance frequency ω_0 $(\omega \approx \omega_0)$, as follows.

$$\hat{V}_{\mathrm{cav}} = \frac{R_{\mathrm{L}}\hat{I}_{\mathrm{cav}}}{\sqrt{1 + \left(2Q_L\frac{\Delta\omega}{\omega}\right)^2}} \tag{2.49}$$

$$\psi \approx \tan^{-1}\left(2Q_L\frac{\Delta\omega}{\omega}\right) = \tan^{-1}\left(2Q_L\frac{\Delta f}{f}\right), \tag{2.50}$$

where $\Delta\omega = \omega_0 - \omega$.

2.3.2 Cavity Detuning

The cavity resonance frequency can change because of cavity deformation, which is due mainly to Lorentz force detuning and microphonics. When a cavity is detuned, more power is required to maintain the cavity field. In this section, the cavity detuning equation is derived.

From Equation 2.50 and 2.49, the bandwidth $\omega_{1/2}$ of a loaded cavity is defined as

$$\omega_{1/2} = \frac{\omega}{2Q_L} \tag{2.51}$$

By approximating $\omega \approx \omega_0$ and substituting Equation 2.51 into Equation 2.46, the cavity differential equation becomes

$$\frac{\mathrm{d}^2 V_{\mathrm{cav}}(t)}{\mathrm{d}t^2} + 2\omega_{1/2}\frac{\mathrm{d}V_{\mathrm{cav}}(t)}{\mathrm{d}t} + \omega_0^2 V_{\mathrm{cav}}(t) = 2\omega_{1/2}R_{\mathrm{L}}\frac{\mathrm{d}I_{\mathrm{cav}}(t)}{\mathrm{d}t} \tag{2.52}$$

If the driving current is harmonic with a time dependence $e^{j\omega t}$, the relations $V_{\mathrm{cav}}(t) = \hat{V}_{\mathrm{cav}} \cdot e^{j\omega t}$ and $I_{\mathrm{cav}}(t) = \hat{I}_{\mathrm{cav}} \cdot e^{j\omega t}$ hold. Equation 2.52 can be rewritten as

$$\begin{aligned} &\frac{\mathrm{d}^2 \hat{V}_{\mathrm{cav}}}{\mathrm{d}t^2} + 2(j\omega + \omega_{1/2})\frac{\mathrm{d}\hat{V}_{\mathrm{cav}}}{\mathrm{d}t} + (\omega_0^2 - \omega^2 + 2j\omega\omega_{1/2})\hat{V}_{\mathrm{cav}} \\ &\qquad = 2\omega_{1/2}R_{\mathrm{L}}\left(\frac{\mathrm{d}\hat{I}_{\mathrm{cav}}}{\mathrm{d}t} + j\omega\hat{I}_{\mathrm{cav}}\right) \end{aligned} \tag{2.53}$$

If we assume that generator frequency ω is very close to the cavity resonance frequency ω_0, the approximation $(\omega_0^2 - \omega^2) \approx 2\Delta\omega\omega$ can be used. After Equation 2.53 is divided by $2j\omega$, it can be written as

$$\begin{aligned} &\frac{1}{2j\omega}\frac{\mathrm{d}^2 \hat{V}_{\mathrm{cav}}}{\mathrm{d}t^2} + \left(1 + \frac{\omega_{1/2}}{j\omega}\right)\frac{\mathrm{d}\hat{V}_{\mathrm{cav}}}{\mathrm{d}t} + (\omega_{1/2} - j\Delta\omega)\hat{V}_{\mathrm{cav}} \\ &\qquad = R_{\mathrm{L}}\left(\frac{\omega_{1/2}}{j\omega}\frac{\mathrm{d}\hat{I}_{\mathrm{cav}}}{\mathrm{d}t} + \omega_{1/2}\hat{I}_{\mathrm{cav}}\right) \end{aligned} \tag{2.54}$$

The second-order terms can be neglected, as they are small compared with the others. The resonance frequency is nearly equal to the RF frequency ($\omega_0 \approx \omega$). For the superconducting cavity, $\omega_{1/2}/\omega_0 \approx 10^{-7}$, and it can be neglected. In the envelope estimation, the hat sign can be omitted. Therefore, equation 2.54 can be rewritten as

$$\frac{\mathrm{d}V_{\mathrm{cav}}(t)}{\mathrm{d}t} + (\omega_{1/2} - j\Delta\omega)V_{\mathrm{cav}}(t) = \omega_{1/2}R_{\mathrm{L}}I_{\mathrm{cav}}(t) \tag{2.55}$$

The cavity detuning can be estimated by comparing the phase of the forward signal with the cavity field. An equation for estimating the detuning is derived as follows. We start with the impedance of the unloaded cavity, Z_{cav}. This impedance depends only on the cavity structure.

$$Z_{\mathrm{cav}} = \frac{R}{1 - jR\left(\frac{1}{\omega L} - \omega C\right)} \tag{2.56}$$

The power transferred from the klystron to the cavity depends on the transformation ratio of the coupler. the coupling factor β is used to describe the transformation ratio 1:N. The coupling factor is defined as

$$\beta = \frac{R}{Z_{\mathrm{ext}}} = \frac{R}{N^2 Z_0} \tag{2.57}$$

where Z_{ext} is the external impedance seen from the cavity side and Z_0 is the transmission line impedance. The loaded shunt impedance R_{L} is determined by the coupling factor β as follows.

$$R_{\mathrm{L}} = \frac{R}{1 + \beta} \tag{2.58}$$

We substitute $\tan\psi$ from Equation 2.48 and R_{L} from Equation 2.58 into Equation 2.56 to obtain

$$Z_{\mathrm{cav}} = \frac{R}{1 - j(\beta + 1)\tan\psi} \tag{2.59}$$

The cavity voltage V_{cav} is related to the forward voltage V_{for} and reflected voltage V_{ref} by

$$V_{\mathrm{cav}} = V_{\mathrm{for}} + V_{\mathrm{ref}} \tag{2.60}$$

The phase of the beam current I_{b} must be π for on-crest acceleration. However, to calculate the cavity current I_{cav}, the beam current must be added because I_{b} already includes the phase information.

$$\begin{aligned} I_{\mathrm{cav}} &= I_{\mathrm{for}} + (I_{\mathrm{ref}} + I_{\mathrm{b}}) \\ &= \frac{V_{\mathrm{for}}}{Z_{\mathrm{ext}}} + \left(-\frac{V_{\mathrm{ref}}}{Z_{\mathrm{ext}}} + I_{\mathrm{b}}\right) \\ &= \frac{2V_{\mathrm{for}} - V_{\mathrm{cav}}}{Z_{\mathrm{ext}}} + I_{\mathrm{b}} \end{aligned} \tag{2.61}$$

where I_{for} is the forward current, I_{ref} is the reflected current, and Z_{ext} is the external impedance seen from the cavity. V_{cav}, Z_{cav}, and I_{cav} are related as follows.

$$V_{\text{cav}} = Z_{\text{cav}} \cdot I_{\text{cav}} \tag{2.62}$$

By Inserting Equation 2.61 into 2.62, the cavity voltage V_{cav} becomes

$$V_{\text{cav}} = \frac{Z_{\text{cav}}}{Z_{\text{cav}} + Z_{\text{ext}}} \cdot (2V_{\text{for}} + Z_{\text{ext}} I_{\text{b}}) \tag{2.63}$$

By inserting Equation 2.59 and $Z_{\text{ext}} = \frac{R}{\beta}$ into Equation 2.63, the cavity voltage caused by both the generator and the beam current is defined as [15]

$$V_{\text{cav}} = \frac{\beta}{\beta + 1} \cdot \frac{1}{1 + \tan^2 \psi} \cdot (1 + j \tan \psi) \cdot \left(2V_{\text{for}} + \frac{R}{\beta} I_{\text{b}} \right) \tag{2.64}$$

The cavity voltage V_{cav} is composed of two parts: the generator induced voltage V_{g} and the beam induced voltage V_{b}.

$$\begin{aligned} V_{\text{cav}} &= V_{\text{g}} + V_{\text{b}} \\ \text{with} \quad V_{\text{g}} &= \frac{\beta}{1 + \beta} \cdot \frac{1}{1 + \tan^2 \psi} \cdot (1 + j \tan \psi) \cdot 2V_{\text{for}} \\ V_{\text{b}} &= \frac{\beta}{1 + \beta} \cdot \frac{1}{1 + \tan^2 \psi} \cdot (1 + j \tan \psi) \cdot Z_{\text{ext}} \cdot I_{\text{b}} \end{aligned} \tag{2.65}$$

To derive an equation to estimate the detuning, it is assumed that cavity voltage is only caused by the induced forward voltage. In case of on-resonance $\psi = 0$ and no beam $I_{\text{b}} = 0$, the cavity voltage V_{cav} becomes.

$$V_{\text{cav}} = V_{\text{g}} = \frac{\beta}{1 + \beta} \cdot 2V_{\text{for}} \tag{2.66}$$

By inserting Equation 2.66 to 2.55, we obtain the equation as follows.

$$\frac{\mathrm{d}V_{\text{cav}}}{\mathrm{d}t} + (\omega_{1/2} - j\Delta\omega) V_{\text{cav}} = \omega_{1/2} \frac{\beta}{\beta + 1} \cdot 2V_{\text{for}} \tag{2.67}$$

For a superconducting cavity, the coupling factor $\beta \gg 1$; therefore, Equation 2.67 can be simplified as

$$\frac{\mathrm{d}V_{\text{cav}}}{\mathrm{d}t} + (\omega_{1/2} - j\Delta\omega) V_{\text{cav}} = 2\omega_{1/2} V_{\text{for}} \tag{2.68}$$

V_{cav} and V_{for} can be written in polar coordinates.

$$V_{\text{cav}} = V_{\text{cav}}(t)e^{j\theta(t)} \quad , \quad V_{\text{for}} = V_{\text{for}}(t)e^{j\varphi(t)} \tag{2.69}$$

where V_{for} is the calibrated forward voltage, V_{cav} is the measured cavity voltage, θ is the angle of the cavity voltage, and φ is the angle of the forward voltage. Substituting Equation 2.69 into Equation 2.68 yields

$$\frac{\mathrm{d}V_{\text{cav}}(t)}{\mathrm{d}t} + jV_{\text{cav}}(t)\frac{\mathrm{d}\theta}{\mathrm{d}t} + (\omega_{1/2} - j\Delta\omega)V_{\text{cav}}(t) = 2\omega_{1/2}V_{\text{for}}(t)\ e^{j(\varphi-\theta)} \tag{2.70}$$

Equation 2.70 can be rearranged as

$$\begin{aligned}\frac{\mathrm{d}V_{\text{cav}}(t)}{\mathrm{d}t} + \omega_{1/2}V_{\text{cav}}(t) + j\left(\frac{\mathrm{d}\theta}{\mathrm{d}t} - \Delta\omega\right)V_{\text{cav}}(t) \\ = 2\omega_{1/2}V_{\text{for}}(t)\ [\cos(\varphi-\theta) + j\ \sin(\varphi-\theta)]\end{aligned} \tag{2.71}$$

Therefore, the real and imaginary parts of Equation 2.70 are as follows.

$$\frac{\mathrm{d}V_{\text{cav}}}{\mathrm{d}t} + \omega_{1/2}V_{\text{cav}}(t) = 2\omega_{1/2}V_{\text{for}}(t)\cos(\varphi-\theta) \tag{2.72}$$

$$\left(\frac{\mathrm{d}\theta}{\mathrm{d}t} - \Delta\omega\right)V_{\text{cav}}(t) = 2\omega_{1/2}V_{\text{for}}(t)\sin(\varphi-\theta) \tag{2.73}$$

Equation 2.72 is the real part, and Equation 2.73 is the imaginary part. The cavity detuning appears only in the imaginary part. Therefore, the cavity detuning can be estimated using [16]

$$\Delta\omega = \frac{\mathrm{d}\theta}{\mathrm{d}t} - 2\omega_{1/2}\frac{V_{\text{for}}(t)}{V_{\text{cav}}(t)}\sin(\varphi-\theta) \tag{2.74}$$

The following relation among the cavity field V_{cav}, the forward voltage V_{for}, and reflected voltage V_{ref}, is used to calibrate the signal.

$$V_{\text{cav}} = V_{\text{for}} + V_{\text{ref}} \tag{2.75}$$

The calibration factor is determined using the following equations [16].

$$V_{\text{for}} = a \cdot V'_{\text{for}} \cdot e^{i\theta\cdot b} \tag{2.76}$$

$$V_{\text{ref}} = c \cdot V'_{\text{ref}} \cdot e^{i\theta\cdot d} \tag{2.77}$$

where V_{for} is the calibrated forward signal, V_{ref} is the calibrated reflected signal, V'_{for} is the measured forward signal, and V'_{ref} is the measured reflected signal.

Further, $a, b, c,$ and d are scaling factors that are obtained using the criterion χ^2 as follows.

$$\chi^2 = \sum_n \left[|V_{\text{cav}}|^2 - (|V_{\text{for}}| + |V_{\text{ref}}|)^2\right]^{1/2} \tag{2.78}$$

where n is the nth sampled data point in one pulse. The range of n is chosen before the RF is turned off. Figure 2.16 shows an example of a signal before and after calibration. After the calibration process, it is expected that during the flattop, the amplitude of forward and reflected signal should be the same. However, the result in Figure 2.16 shows that there is difference between forward and reflected signals during the flattop. The reason is that because of coupler leakage, the measured reflected signal also includes the forward signal, and the measured forward signal also includes the reflected signal.

2.3.3 Klystron Power Requirement

In pulsed mode operation, there are two characteristic values of the feeding power: the power during the filling time and that during the flattop. The cavity voltage during the filling time can be calculated using the following equation.

$$V_{\text{fill}} = 2\left(\frac{r}{Q}\right) Q_{\text{L}} I_{\text{g}} \left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.79}$$

where I_{g} is the current of the generator. During the filling time, the power requirement is governed by the following equation [17] (see Appendix A).

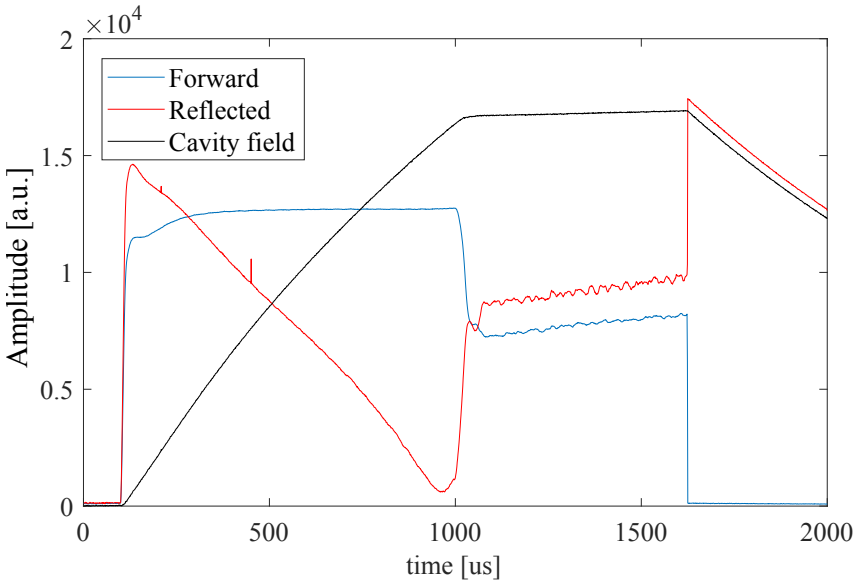
$$P_{\text{fill}} = \frac{V_{\text{cav}}^2 \left(\omega_0^2 + 4Q_{\text{L}}^2 \Delta\omega^2\right)}{4\left(\frac{r}{Q}\right) Q_{\text{L}} \omega_0^2 \left[1 + e^{-\frac{T_{\text{fill}}\omega_0}{Q_{\text{L}}}} - 2e^{-\frac{T_{\text{fill}}\omega_0}{2Q_{\text{L}}}} \cos\left(\Delta\omega T_{\text{fill}}\right)\right]} \tag{2.80}$$

When there is no detuning ($\Delta\omega = 0$), Equation 2.80 becomes simply

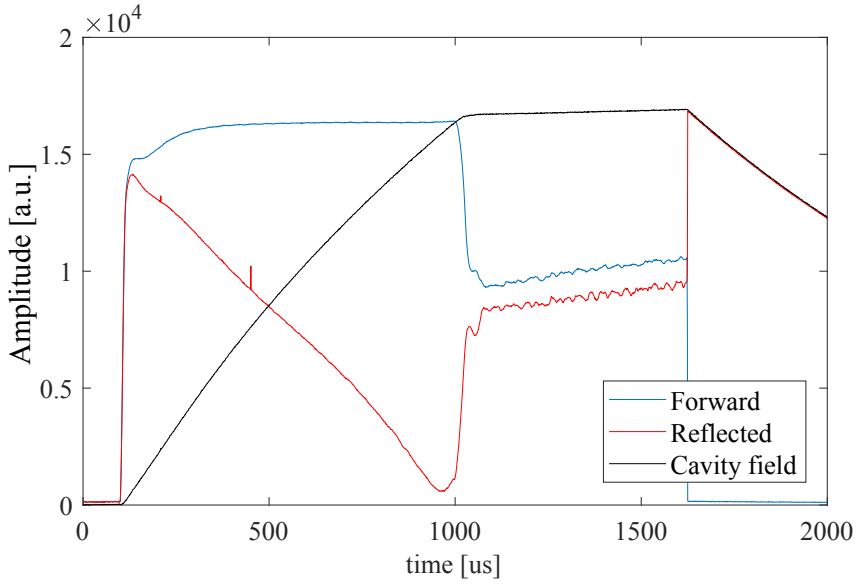
$$P_{\text{fill}} = \frac{V_{\text{cav}}^2}{4\left(\frac{r}{Q}\right) Q_L \left(1 - e^{-\frac{T_{\text{fill}}\omega_0}{2Q_L}}\right)^2} \tag{2.81}$$

where T_{fill} is the time required to fill the cavity from zero to the dedicated gradient. During the flattop for a beam current I_b, the power requirement is governed by the following equation [15].

$$P_{\text{flat}} = \frac{V_{\text{cav}}^2}{\frac{r}{Q} Q_L} \frac{\beta + 1}{4\beta} \left\{ \left(1 + \frac{\frac{r}{Q} Q_L I_{b0}}{V_{\text{cav}}} \cos(\phi_b)\right)^2 + \left(\tan(\psi) + \frac{\frac{r}{Q} Q_L I_{b0}}{V_{\text{cav}}} \sin(\phi_b)\right)^2 \right\} \tag{2.82}$$



(a) Before calibration process



(b) After calibration process

Figure 2.16: Example of amplitude of forward and reflected signal before and after calibration process.

For superconducting cavities, where $\beta >> 1$, this equation can be simplified to [15]

$$P_{\text{flat}} = \frac{V_{\text{cav}}^2}{4\frac{r}{Q}Q_L}\left\{\left(1+\frac{\frac{r}{Q}Q_L I_{b0}}{V_{\text{cav}}}\cos(\phi_b)\right)^2+\left(\frac{\Delta f}{f_{1/2}}+\frac{\frac{r}{Q}Q_L I_{b0}}{V_{\text{cav}}}\sin(\phi_b)\right)^2\right\} \tag{2.83}$$

If the direction of the beam current I_b is exactly opposite to that of the cavity voltage $V_{\rm cav}$, the beam phase $\phi_b = 0$, and the power at the flattop becomes

$$P_{\rm flat} = \frac{V_{\rm cav}^2}{4\frac{r}{Q}Q_L}\left(1 + \frac{\frac{r}{Q}Q_L I_{b0}}{V_{\rm cav}}\right)^2 \tag{2.84}$$

In terms of the klystron power requirement in the ILC, the goal is to use as little power as possible. To determine the minimum power, the optimal detuning is determined using the following equation.

$$\tan\psi_{\rm opt} = -\frac{2R_{\rm L}I_{\rm b0}}{V_{\rm cav}}\sin\phi_{\rm b} = -\frac{2}{\beta+1}\frac{RI_{\rm b0}}{V_{\rm cav}}\sin\phi_{\rm b} \tag{2.85}$$

Thus, the minimum generator power can be written as

$$P_{\rm g} = \frac{V_{\rm cav}^2}{R_{\rm L}}\frac{\beta+1}{\beta}\left[1 + \frac{2R_{\rm L}I_{\rm b0}}{V_{\rm cav}}\cos\phi_{\rm b}\right]^2 \tag{2.86}$$

The optimal coupling can be found by differentiating Equation 2.86 with respect to β.

$$\beta_{\rm opt} = 1 + \frac{2RI_{\rm b0}}{V_{\rm cav}}\cos\phi_{\rm b} \tag{2.87}$$

For superconducting cavities, the coupling parameter $\beta >> 1$, and

$$\begin{aligned}
\beta_{\rm opt} - 1 &= \frac{2RI_{\rm b0}}{V_{\rm cav}}\cos\phi_{\rm b} \\
&\Rightarrow \frac{R}{\beta} \sim \frac{R}{\beta+1} = (R_{\rm L})_{\rm opt} = \frac{1}{2}\left(\frac{r}{Q}\right)(Q_{\rm L})_{\rm opt} = \frac{V_{\rm cav}}{2I_{\rm b0}\cos\phi_{\rm b}} \\
&\Rightarrow (Q_{\rm L})_{\rm opt} = \frac{V_{\rm cav}}{\left(\frac{r}{Q}\right)I_{\rm b0}\cos\phi_{\rm b}}
\end{aligned} \tag{2.88}$$

In the ILC, with the parameters listed in Table 2.1, the optimal loaded $Q_{\rm L}$ becomes

$$\begin{aligned}
(Q_{\rm L})_{\rm opt} &= \frac{31.5\times10^6 \cdot 1.038}{1036 \cdot 5.8\times10^{-3} \cdot \cos 5^\circ} \\
&= 5.46\times10^6
\end{aligned}$$

The minimum generator power becomes

$$\begin{aligned}
(P_{\rm g})_{\rm min} &= \beta_{opt} \cdot \frac{V_{\rm cav}^2}{2R} \\
&= V_{\rm cav} \cdot I_{\rm b0} \cdot \cos\phi_{\rm b}
\end{aligned} \tag{2.89}$$

In the ILC, the minimum generator power becomes

$$\begin{aligned}(P_{\mathrm{g}})_{\mathrm{min}} &= 31.5 \times 10^{6} \cdot 1.038 \cdot 5.8 \times 10^{-3} \cdot \cos 5^{\circ} \\ &= 188.9\,\mathrm{kW}\end{aligned}$$

Table 2.1: Cavity baseline parameters from ILC-TDR [1]

Parameter	Value	Unit
Frequency	1.3	GHz
Beam current	5.8	mA
Gradient	31.5	MV/m
RF pulse	1.65	ms
Flattop	0.727	ms
Filling	0.924	ms
Loaded Q	5.5×10^{6}	
Beam phase	5.8	deg.
Cavity length	1.038	m
r/Q	1036	Ω

2.4 Digital LLRF Control System in the ILC

The ILC accelerators are operated in pulsed mode. Figure 2.17 shows the signal from a typical forward pulse from the klystron (red dashed line), the reflected signal (green dashed line), and the cavity signal (black line) when there is no beam. The filling time is the time required for the RF voltage to reach the designed value. It is followed by the flattop, where the beams are accelerated. The ILC pulse specifications are a filling time of 924 µs, flattop of 727 µs, and pulse length of 1650 µs [1].

The purpose of the digital LLRF control system is to control the RF accelerating field to meet the RF stability requirements. The requirements for the RF control system are usually determined in terms of the amplitude and phase stability of the accelerating field during the flattop.

The RF amplitude and phase stability requirements of the ILC in the bunch compressor are 0.5 % (RMS) and 0.32° (RMS), respectively. In the main linac, the ILC RF amplitude and phase stability requirements are 0.07 % (RMS) and 0.35° (RMS), respectively [1].

The ADC requirement for one RF station is large because of the large number of signals to be measured. Consequently, fabrication of the digital LLRF board is difficult. Use of a modular digital LLRF control system is one way to

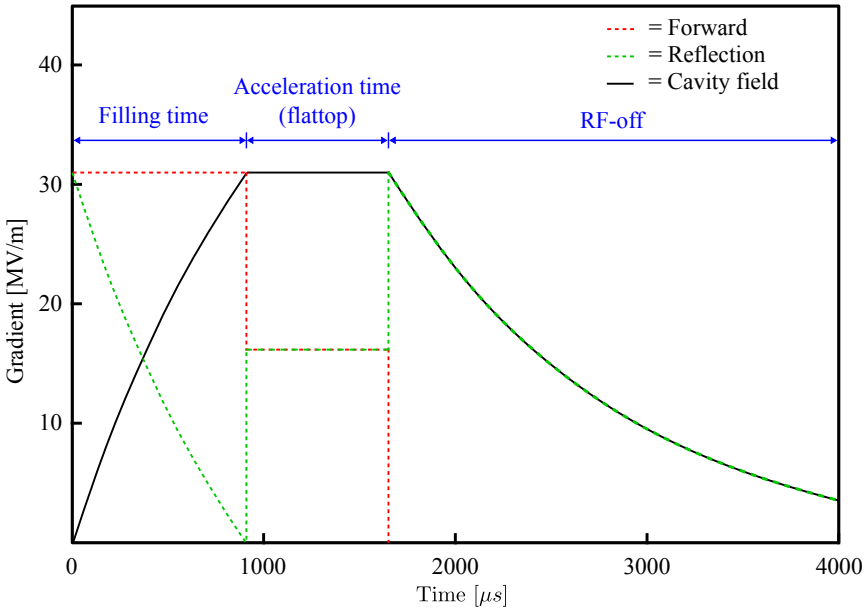


Figure 2.17: Typical RF forward pulse, reflection, and cavity field signals when there is no beam. The pulse signal consists of the filling time and beam acceleration time.

solve this problem. This method is presented in Chapter 3. The other way to mitigate this problem, combining different IFs, is presented in Chapter 4.

The digital LLRF control system configuration based on the ILC Technical Design Report (TDR) is shown in Figure 2.18. The LLRF front-end controller measures the signal from the cavity, and the result is sent to the central LLRF controller. The central LLRF controller calculates the vector sum of all the slave boards and applies the control algorithm to regulate the klystron.

2.5 Digital LLRF Control System in STF

At the STF, several digital LLRF control boards have been developed [18, 19]. The following boards are used in the work described in this thesis.

- MTCA.4-compliant digital LLRF. This board was used to implement the master–slave configuration; the details are presented in Chapter 3.

- MTCA.0-compliant digital LLRF. This board was used for IF-mixture implementation; the details are given in Chapter 4.

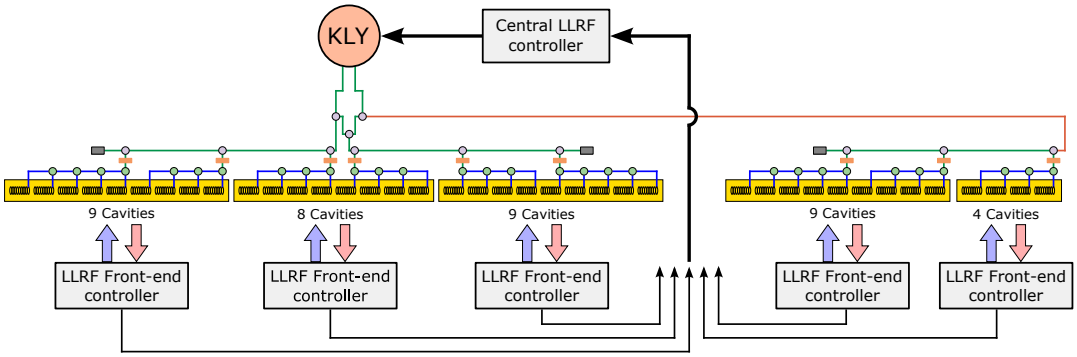


Figure 2.18: Digital LLRF control system with master–slave configuration based on the ILC TDR. LLRF front-end controller measures the signal from the cavities and sends the result to the central LLRF controller, in which the control algorithm is applied to regulate the klystron output [1].

- MTCA.0-compliant digital LLRF. This board was used to implement direct sampling; the details are presented in Chapter 5.
- cPCI-compliant digital LLRF. This board was used to monitor the cavity field, forward, and reflected signals. The details are presented in Chapter 6.

Chapter 3

Digital LLRF Control System with Master-Slave Configuration

The minimum setup of the digital LLRF control system with a master–slave configuration for the ILC was constructed at the STF [20]. Operation with eight cavities was conducted. The performance was evaluated and is presented in this chapter.

The motivation for constructing the digital LLRF control system with a master–slave configuration is to address the following issues in the ILC. By distributing the controller over several slave boards, groups of a few cavities are connected to a slave board, so the signal transmission length can be kept the same. Consequently, the signal transmission delay of cavities in that group can be kept the same. Furthermore, the many signals from the cavities can be distributed to several slave boards, so fabrication of one board with a large number of input channels can be avoided.

To demonstrate the digital LLRF control system with a master–slave configuration, the minimum setup was built at the STF. The contribution of the experiment is that this is the first implementation of a digital LLRF control system with a master–slave configuration at the STF.

3.1 Digital LLRF System Setup

Figure 3.1 shows the minimum setup of the digital LLRF control system installed at the STF. The slave board is connected to four cavities, and the master board is connected to four cavities.

During the experiment, the master and slave boards are connected by an optical cable approximately 20 m long. In the experiment, only eight cavities were operated: five cavities in cryomodule CM-1 (cavities #1, #2, #3, #4, and

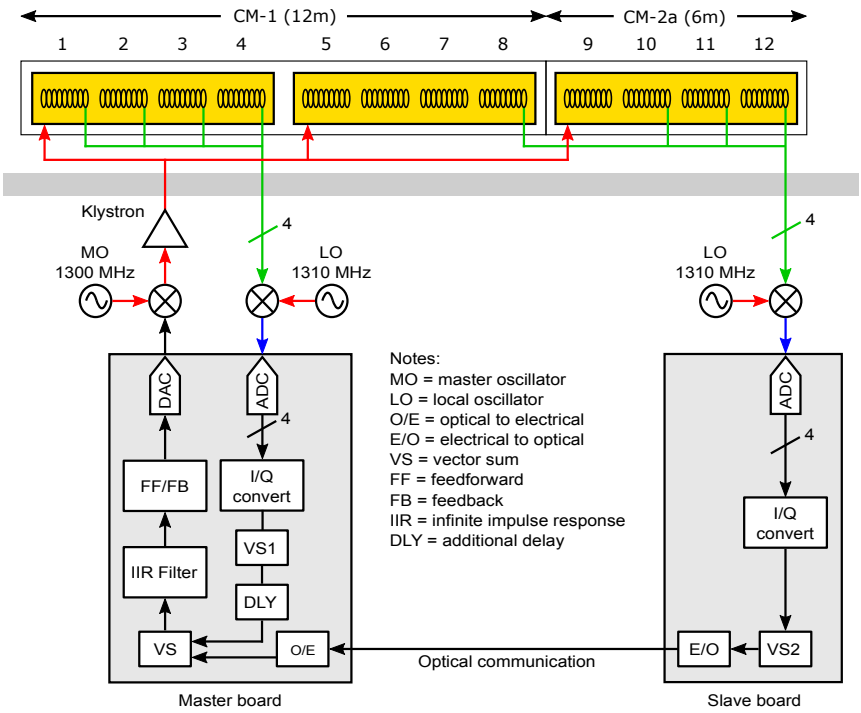


Figure 3.1: Simplified diagram of minimum setup of digital LLRF control system with master–slave configuration at STF-KEK. VS1 is the partial vector sum of the cavities connected to the master board. VS2 is the partial vector sum of the cavities connected to the slave board.

#8) and three cavities in cryomodule CM-2a (cavities #10, #11, and #12). The other cavities were not operated because their performance was degraded. There were two types of performance degradation: a gradient drop due to heavy field emission (cavities #5, #6, and #7) and a gradient drop without radiation (cavity #9) [8].

The master and slave boards use the same hardware. The system is composed of front and rear boards. The boards comply with the MTCA.4 standard [21]. Each board is equipped with 14 channels of 16-bit ADCs (AD9650, Analog Device, Inc. [22]), two 16-bit DACs (AD9783, Analog Device, [23]), a Spartan 6 (XC6SLX) FPGA, and a Zynq-7000(XC7Z045) FPGA. The system clock is 162.5 MHz.

Figures 3.2 and Figure 3.3 show a photograph and a simplified block diagram of these boards, respectively.

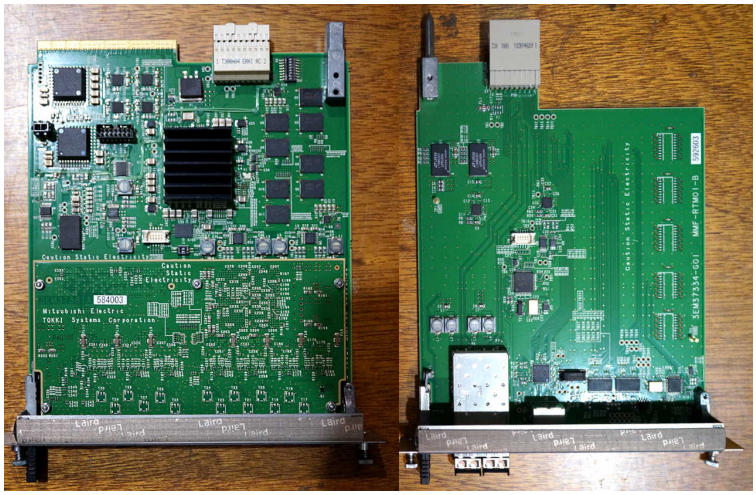


Figure 3.2: MTCA.4-compliant board for master–slave configuration. Left: front board equipped with 14 ADCs (AD9650), 2 DACs (AD9783), and Xilinx Zynq-7000 and Spartan 6 FPGAs. Right: μRTM (MTCA Rear Transition Module) equipped with a gigabit ethernet card (RJ-45), small form-factor pluggable connector, and digital input/output.

3.2 Optical Link Delay Consideration

The motivation for investigating the optical link communication delay investigation is to determine whether it affects the RF stability. Because the beam

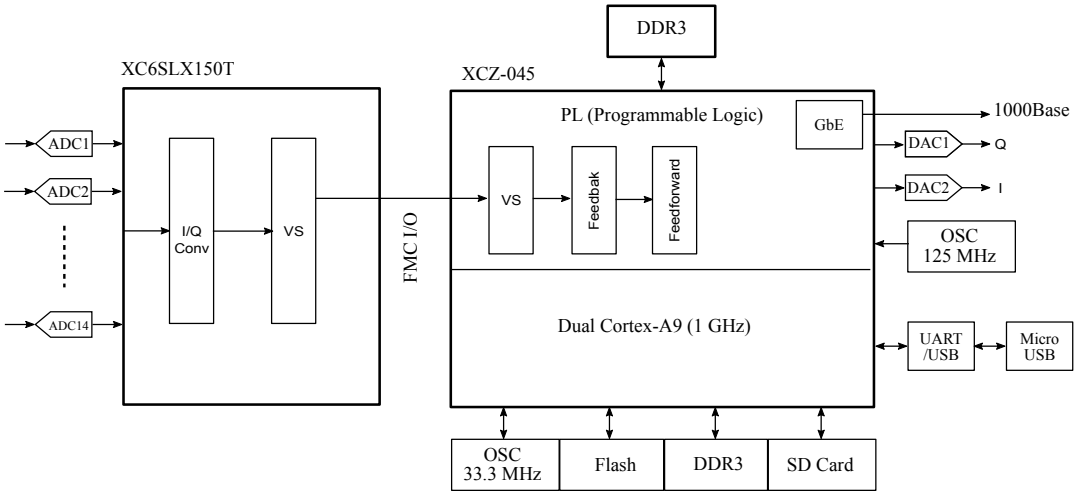


Figure 3.3: Schematic of the MTCA.4-compliant front. It is composed of two FPGAs: a Spartan 6 (XC6SLX150T) and a Xilinx Zynq-7000 (XCZ045).

was not available during the measurement, the experiments were conducted without the beam. A study involving the beam is needed in the future.

One important feature of the link between the master and slave is the delay introduced by the optical communication link. The delay is due mainly to the processes of conversion from electrical to optical (E/O) and optical to electrical (O/E) signals. This delay will increase the total loop delay of the control system. Increasing the loop delay reduces the gain margin and increases the error. This can make the system unstable. Therefore, the delay caused by the optical communication link must be evaluated.

In the master–slave configuration shown in Figure 3.1, the VS1 module calculates the partial vector sum of the master board. The VS2 module calculates the partial vector sum of the slave board. The DLY module is used to add a digital delay to the partial vector sum in the master board. The optical communication link delay affects only the partial vector sum VS2. Therefore, before the delay can be investigated, the partial vector sums VS1 and VS2 must be synchronized. To synchronize them, a delay compensation must be added to the partial vector sum VS1 by adding an additional delay on the DLY module. The additional delay should be the same as or very close to the optical communication link delay. The following procedure is applied to estimate the delay time of the optical communication link.

To estimate the optical link communication delay, the measurement setup shown in Figure 3.4 is used. The signal flow starts at the DAC output and ends at the VS input. The same signal is fed to both the master and slave

boards. In this case, the forward signal is used because it has a sharp step at the end, at which it is evaluated. Only the feed-forward controller is used in this estimation.

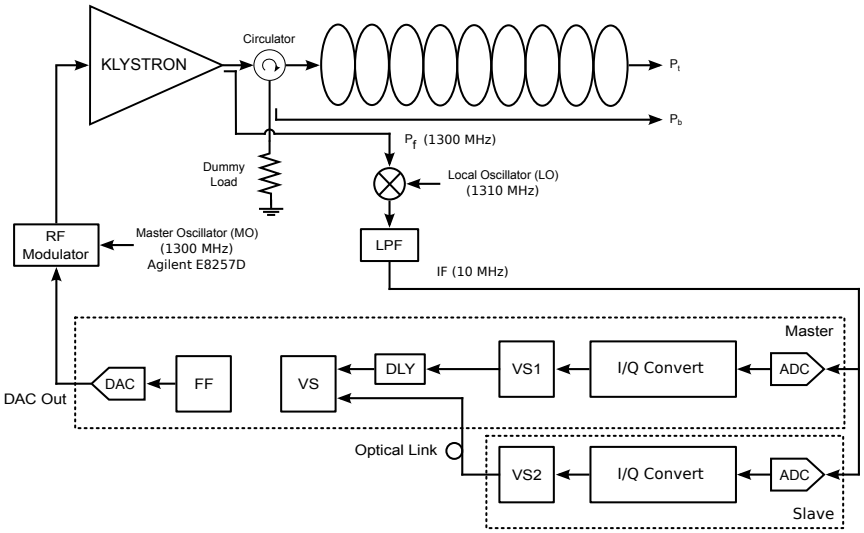


Figure 3.4: Measurement setup used to estimate the delay time introduced by the optical link communication and to estimate the loop delay. Only the forward signal is used in the evaluation. Two ADCs on the master and slave boards are fed with the same signal. The forward signal is chosen because it has a sharp edge at the end.

Three test points are evaluated to estimate the optical communication link delay and also the loop delay. The test point DLY output is the vector sum of the cavities connected to the master board with an adjustable additional delay. The test point VS2 is the vector sum of the cavities connected to the slave board. The test point DAC Out is the output of the DAC. Figure 3.5 shows the signals at these three test points.

The loop delay is estimated by measuring the time difference between the DAC output signal and the DLY output signal with DLY set to 0 clock. The estimated loop delay is approximately 1.22 µs.

To estimate the optical communication link delay, the time difference between the DLY output signal and the VS2 output signal is measured. The estimated optical communication link delay is approximately 0.56 µs, which corresponds to approximately 91 clk with a system clock of 162.5 MHz. The optical link delay estimated using this method is not precise because it is hard to determine the end of the forward signal from the graph. Thus, we developed another measurement method for obtaining a more precise delay time.

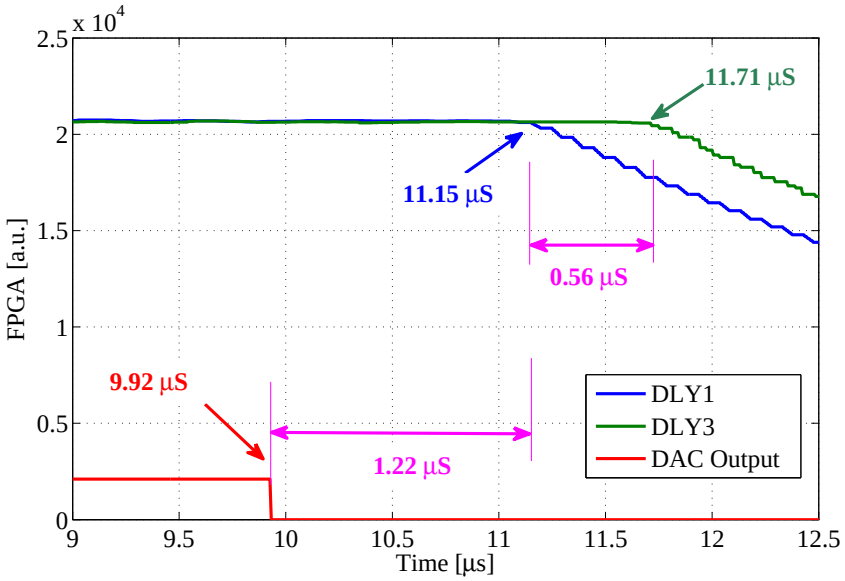


Figure 3.5: Forward signal is used to estimate the optical link communication delay and loop delay. DAC output signal is the starting point of the signal (see Figure 3.4). The signal then travels to the klystron and is finally fed to ADCs on both the slave and master boards.

For the more precise delay estimation, we use the same setup as in Figure 3.4. The end of the forward signal is then investigated and is shown in Figure 3.6. The additional delay in DLY is then varied from 50–110 clocks. The squared area in the time interval from approximately 4–8 µs is calculated for each DLY value. The squared area is chosen to calculate the difference because it gives a better estimation for values close to zero.

The calculated squared area for each DLY value is then fitted to find the minimum value, which corresponds to the estimated optical communication link delay. The graph fitted with a second-order polynomial is shown in Figure 3.7. From the fitted line, the squared area is minimum when the delay is 88.3 clk, which corresponds to approximately 546 ns with a system clock of 162.5 MHz. This value of 88 clk is used to compensate the optical communication link delay by inputting it to the DLY module.

The additional delay of 540 ns is relatively small compared with the response time of the superconducting cavity. An experiment was conducted to understand the effect of the additional delay and confirm that the additional delay produces a small perturbation to the system with proper delay compensation.

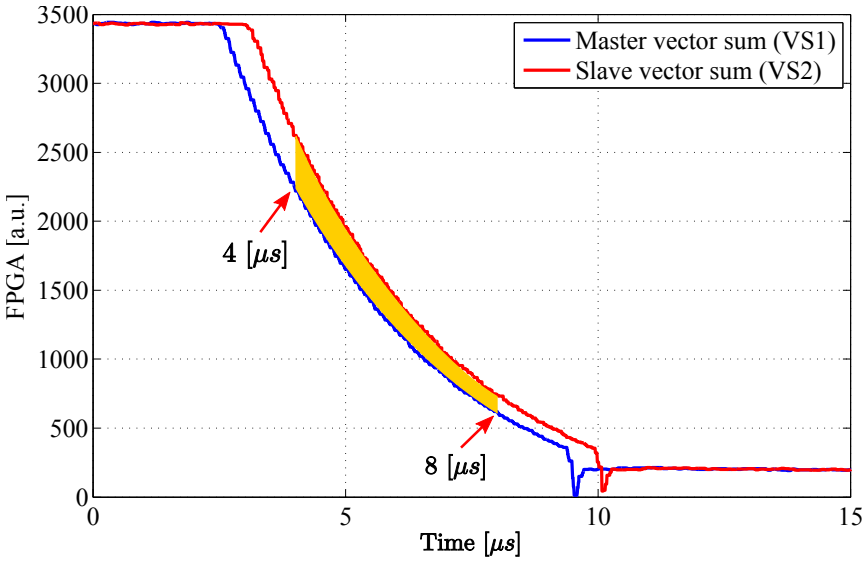


Figure 3.6: Squared area between master vector sum (VS1) and slave vector sum (VS2) was calculated from approximately 4–8 µs for each additional delay value of VS1.

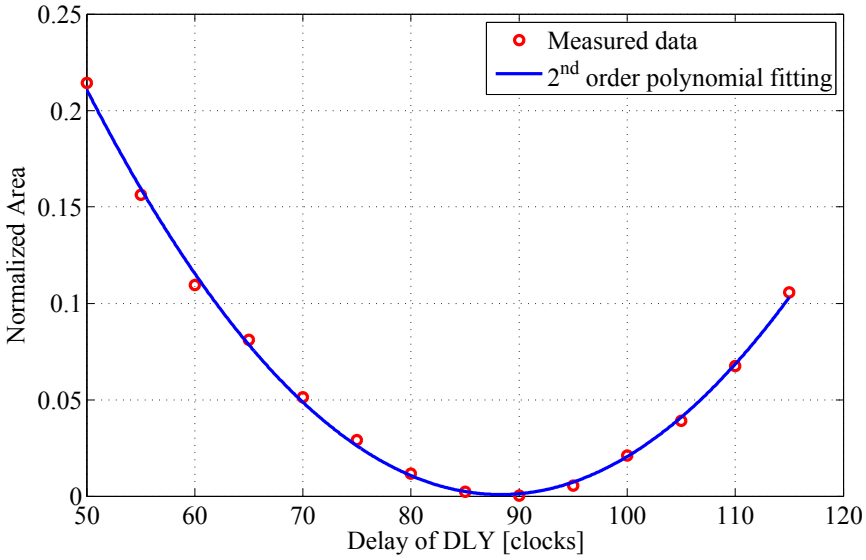


Figure 3.7: Fitted graph of normalized mean square error (MSE) between DLY1 and DLY3 signals. The MSE data are fitted with the third-order polynomial data.

3.3 Performance Evaluation

The motivation for the performance evaluation in this section was to determine the effect of the optical communication link delay on the RF stability. The optical communication link delay contributes to the control loop delay. A long delay in the control loop may lead to system instability.

To perform the evaluation, two setup configurations were evaluated. In the first configuration, four cavities (#1, #2, #3, and #4) were connected to the master board, and four cavities (#8, #10, #11, and #12) were connected to the slave board. In the second configuration, all eight cavities were connected to the master board. Feed-forward and feedback control were used in both setups.

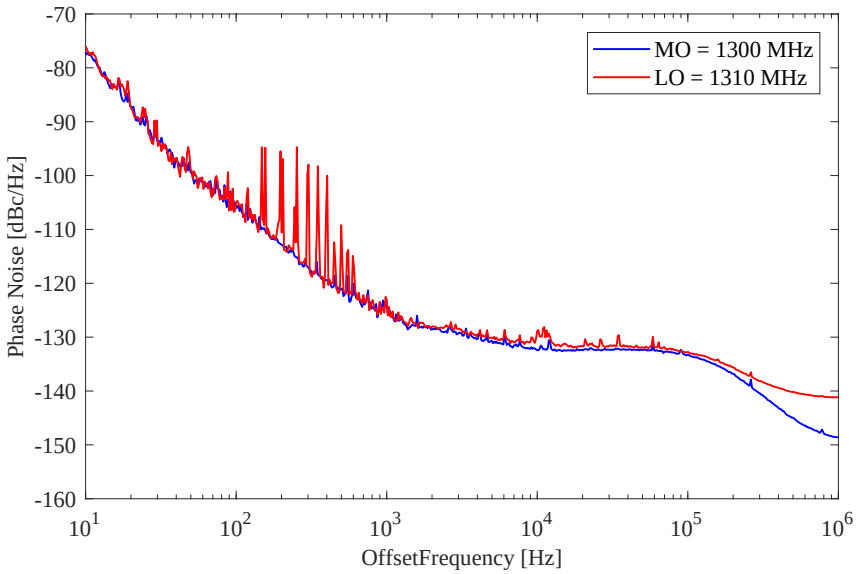
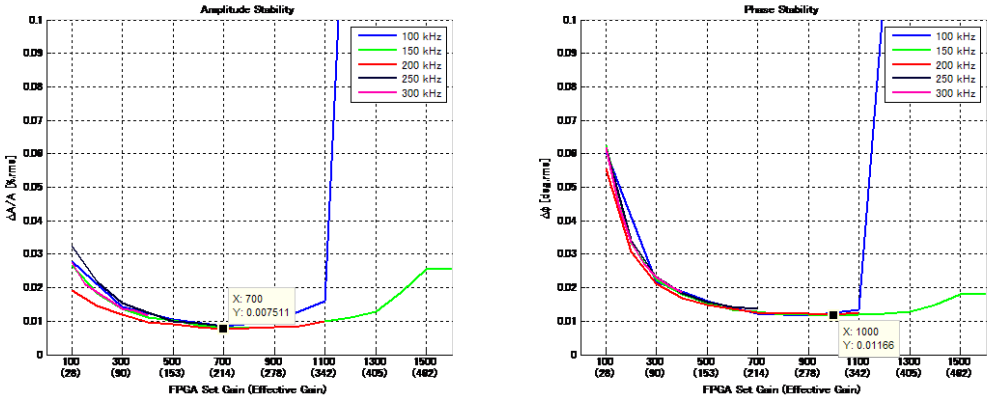


Figure 3.8: Phase noise of MO and LO. For the MO, the estimated jitter is 56 fs, which corresponds to 26 mdeg. For the LO, the estimated jitter is 60 fs, which corresponds to 28 mdeg.

Before this experiment, the contribution of the LO signal jitter was evaluated. Both the master and slave boards used an LO of 1310 MHz. The measured phase noise of the master oscillator (MO) and LO are shown in Figure 3.8. The jitter estimation was calculated from 10 Hz to 1 MHz. For the MO, the estimated jitter is 56 fs, which corresponds to 26 mdeg. For the LO, the estimated jitter is 60 fs, which corresponds to 28 mdeg. This measurement shows that LO generation adds only approximately 2 mdeg of additional phase noise. Thus, it can be concluded that LO generation did not add a significant additional error.

To determine the optimal feedback gain operation, the gain scan method was applied. The bandwidth of the digital filter was set to a certain value, and the feedback gain was varied. The gradient was set to 25 MV/m. Figure 3.9 shows the amplitude and phase stabilities for various feedback gains and digital filter bandwidths. The effective gain range that yields good stability is 150 to 300. During the experiment, a feedback gain of 150 was chosen. All the digital filter bandwidths yielded similar stability in the feedback gain range of 150 to 300. The purpose of the digital filter is to remove the $8\pi/9$ mode, the frequency of which is approximately 800 kHz lower than the π-mode frequency. To obtain higher attenuation of the $8\pi/9$-mode frequency, the digital filter bandwidth can be set lower. However, the digital filter will introduce a larger phase delay that limits the critical gain and leads to a reduction in the gain margin. On the basis of this experiment, a digital filter bandwidth of 250 kHz was chosen.

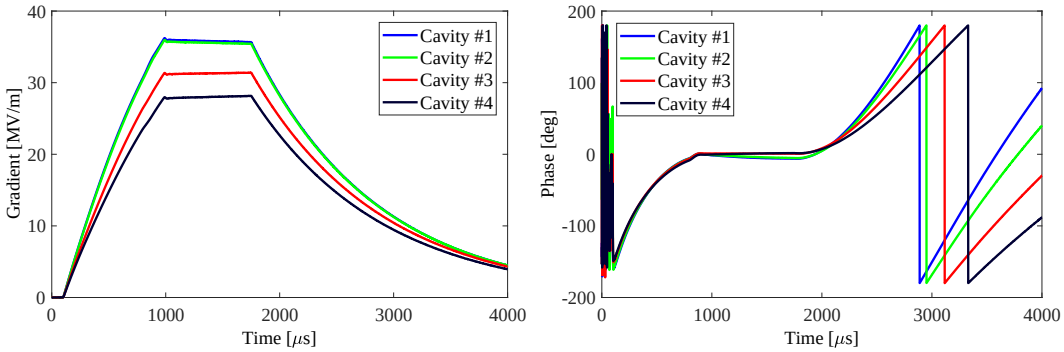


(a) Amplitude stability (b) Phase stability

Figure 3.9: (a) Amplitude and (b) phase stability for various feedback gains and digital filter bandwidths.

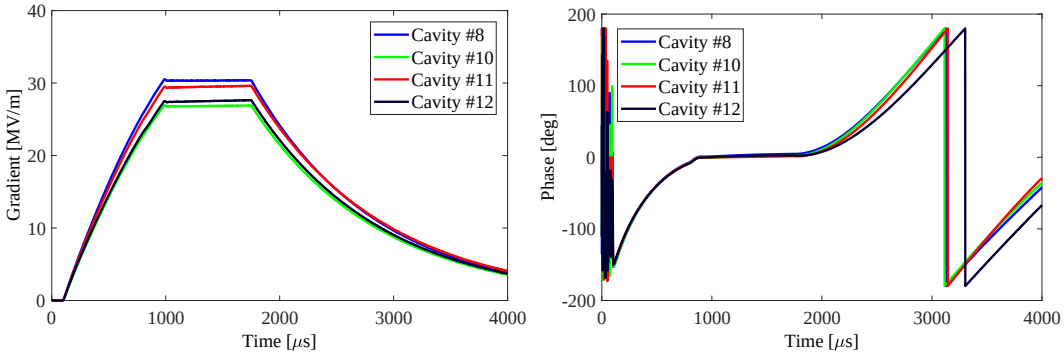
Two configurations were used to evaluate the performance. In the first configuration, an additional delay of 88 clk was set in the DLY module (see Figure 3.4). In this configuration, there is expected to be an additional delay in the control loop of approximately 540 ns caused by the optical communication link. The effective loop gain was set to 150. The digital filter bandwidth was set to 250 kHz. The amplitude and phase waveforms of the four cavities connected to the master board are shown in Figure 3.10. Those of the four cavities connected to the slave board are presented in Figure 3.11. The vector sum signals of the master board, VS1, and the slave board, VS2, (refer to Figure 3.1) are shown in Figure 3.12. The waveforms of the vector sum VS of VS1 and VS2 are shown in Figure 3.13. RF stabilities of 0.006 % (RMS) and

0.027° (RMS) can be achieved for the flattop region from 1100–1700 µs.



(a) Amplitude (b) Phase

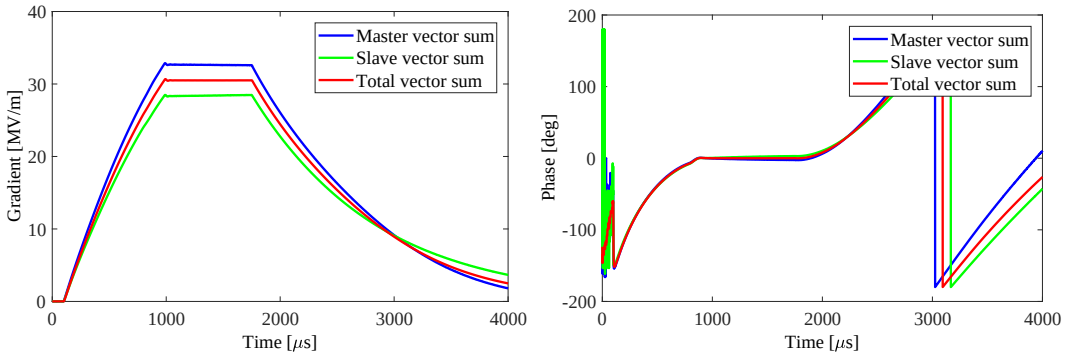
Figure 3.10: Amplitude and phase of cavities #1, #2, #3, and #4. The mean flattop gradients of each cavity are 35.8 MV/m (cavity #1), 35.6 MV/m (cavity #2), 31.3 MV/m (cavity #3), and 28.0 MV/m (cavity #4).



(a) Amplitude (b) Phase

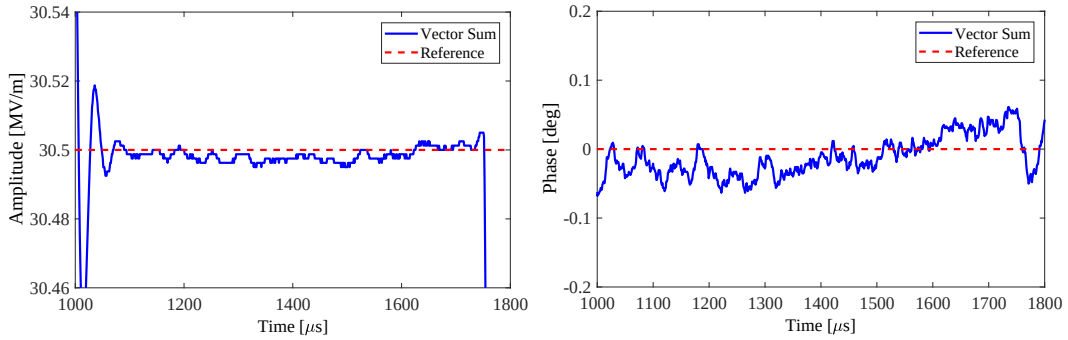
Figure 3.11: Amplitude and phase of cavities #8, #10, #11, and #12. The average flattop gradients of each cavity are 30.3 MV/m (cavity #8), 26.8 MV/m (cavity #10), 29.5 MV/m (cavity #11), and 27.5 MV/m (cavity #12).

In the second configuration, all eight cavity signals were fed only to the master board. Figure 3.14(a) and 3.14(b) show the amplitude and phase of each cavity, respectively. Figure 3.15 shows the flattop of the vector sum of the eight cavities. RF stabilities of 0.008 % (RMS) and 0.027° (RMS) are realized in the flattop region. The input configuration and results are summarized in Table 3.1. The stability is calculated for 20 pulses. From the results, we can see that both setups achieved similar RF stabilities. It can be concluded that with proper delay compensation, the optical link communication delay does not



(a) Amplitude (b) Phase

Figure 3.12: Amplitude and phase of partial vector sum from slave and master and total vector sum. The average flattop gradient are *Master vector sum* (VS1) = 32.6 MV/m, *Slave vector sum* (VS2) = 28.4 MV/m, and *Total vector sum* = 30.5 MV/m

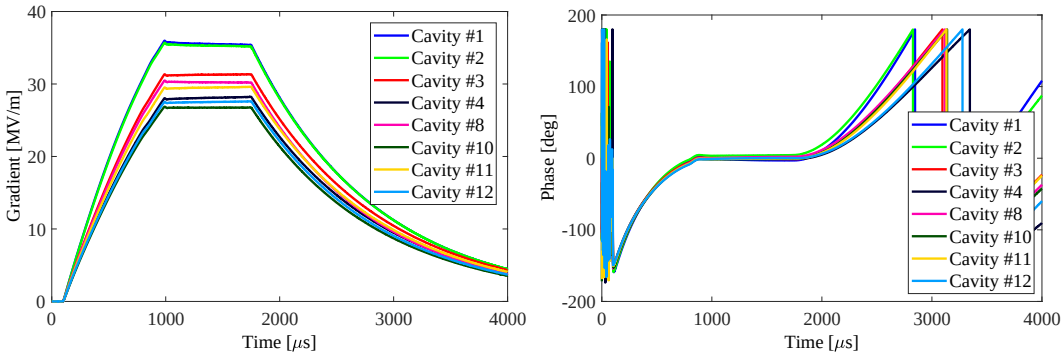


(a) Amplitude (b) Phase

Figure 3.13: Flattop of vector sum of eight cavities operated in master–slave configuration.

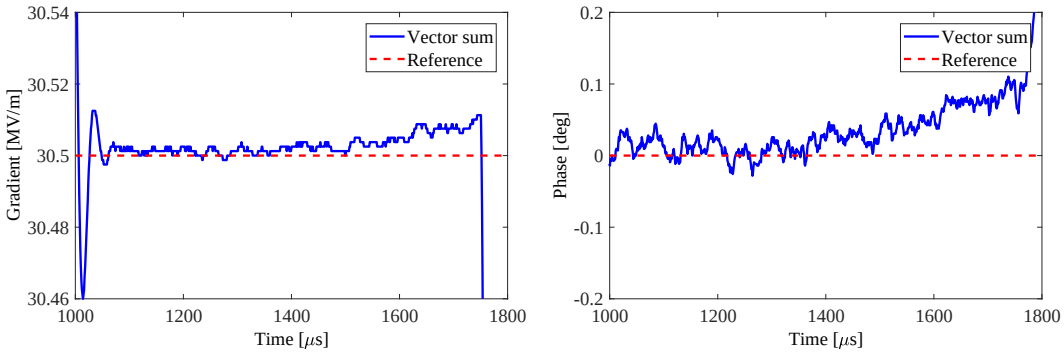
affect the RF stability when there is no beam. Both configurations can also fulfill the ILC RF stability requirements. Further investigation of the case with a beam is necessary.

Furthermore, to confirm that the optical communication link delay has no significant effect, a further additional delay of 800 clk (which corresponds to 4.9 µs) was added to DLY. The interesting part of the signal is the end of the signal, as shown in Figure 3.16. This result shows that lengthening the delay does not produce any phenomena such as spikes in the amplitude and phase waveforms. It can be inferred that even though the delay by a partial vector sum is sufficiently long, it does not generate unwanted behavior. The reason is that the delay is less than the response time of the superconducting cavity.



(a) Amplitude (b) Phase

Figure 3.14: Waveform of amplitude and phase of eight cavities connected only to master board.



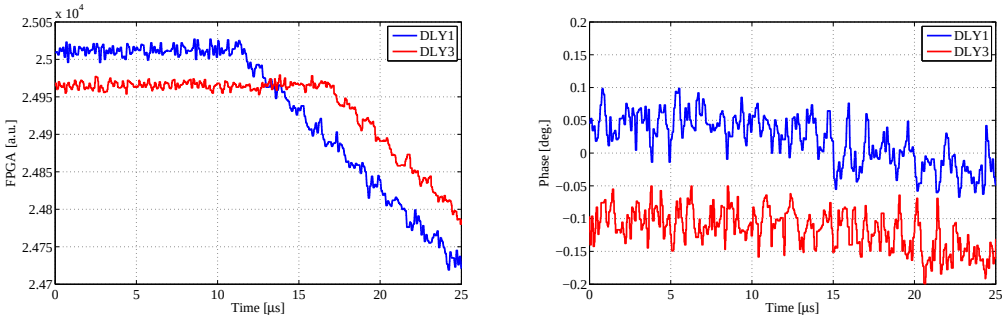
(a) Amplitude (b) Phase

Figure 3.15: Flattop of vector sum of eight cavities operated with only master board.

Furthermore, to make sure that there is no significant effect caused by optical communication link delay, the more additional delay of 800 clk (which corresponds to 4.9 µs) was added to DLY. The interesting part of signal is the end of the signal as shown in Figure 3.16. This result shows that by lengthening the delay, there is no phenomenon such as spike found in amplitude and phase waveform. It can be inferred that even though the delay of a partial vector sum is long enough, the delay does not generate unwanted phenomenon. It can be understood because the delay is less than the response time of superconducting cavity.

Table 3.1: Summary of the amplitude and phase stabilities of different input configurations.

Setup	**Connected Cavity**		**DLY1**	**Stability**	
	Master	**Slave**	**[clock]**	**Amp [% (RMS)]**	**Pha [deg.(RMS)]**
1	1,2,3,4	8,10,11,12	88	0.006	0.027
2	1,2,3,4,8,10,11,12	-	0	0.008	0.027



(a) Amplitude (b) Phase

Figure 3.16: Amplitude and phase waveform at the end of Pf signal from the measurement using the setup in Figure 3.4. Additional delay of 800 clk was added to the DLY3.

3.4 Long Time Performance Evaluation

The motivation for performing this experiment is to determine the RF stability over a long period because in reality, an accelerator facility should provide the required RF stability during long-term operation.

The long-term amplitude and phase stability results are shown in Figures 3.17 and 3.18, respectively. Measurements were conducted by operating eight cavities with vector-sum feedback and feed-forward control in the master–slave configuration. A 30.5 MV/m cavity gradient can be achieved. This is slightly lower than the gradient requirement of the ILC, but it shows that the digital LLRF control system with the master–slave configuration can work well and that the ILC RF stability requirements can be fulfilled.

The amplitude and phase stabilities in long-term measurement are shown in Figures 3.17 and 3.18, respectively. In certain time ranges, data are not available because the system was off. The average phase and amplitude stabilities between 3:00 and 3:40 are 0.014 % (RMS) and 0.015° (RMS), respectively. The

results show that the stability can meet the ILC requirements. The cause of the performance difference between short-term and long-term operation is not yet known. One possible explanation is a difference in the operation environment, such as a difference in the microphonics, between those two experiments. Further investigation is needed.

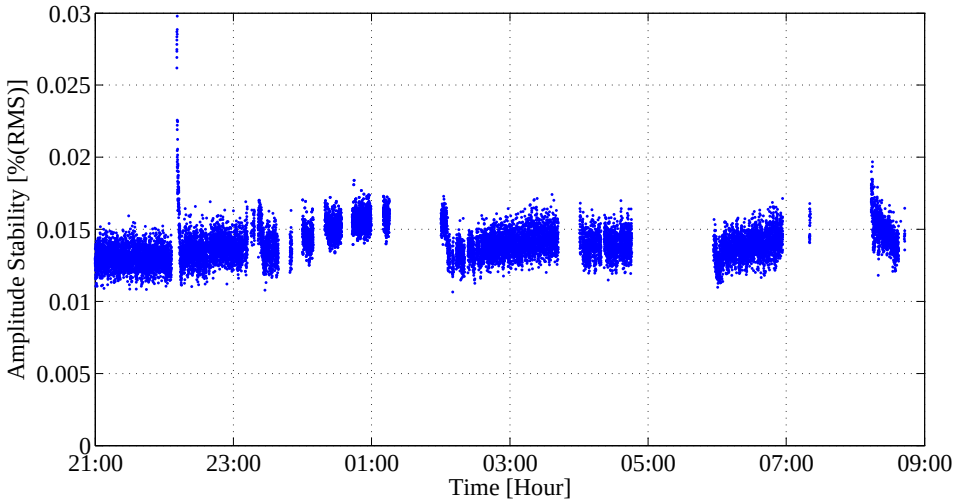


Figure 3.17: Long-term amplitude stability

3.5 Summary

The minimum setup of a digital LLRF using a master–slave configuration for the ILC was constructed. The additional delay introduced by optical link communication does not affect the stability. Amplitude and phase stabilities of 0.006 % (RMS) and 0.027° (RMS), respectively, can be achieved, which meet the ILC requirements. The measurements were conducted without a beam. The master–slave configuration can be implemented for realization of an RF station in the ILC.

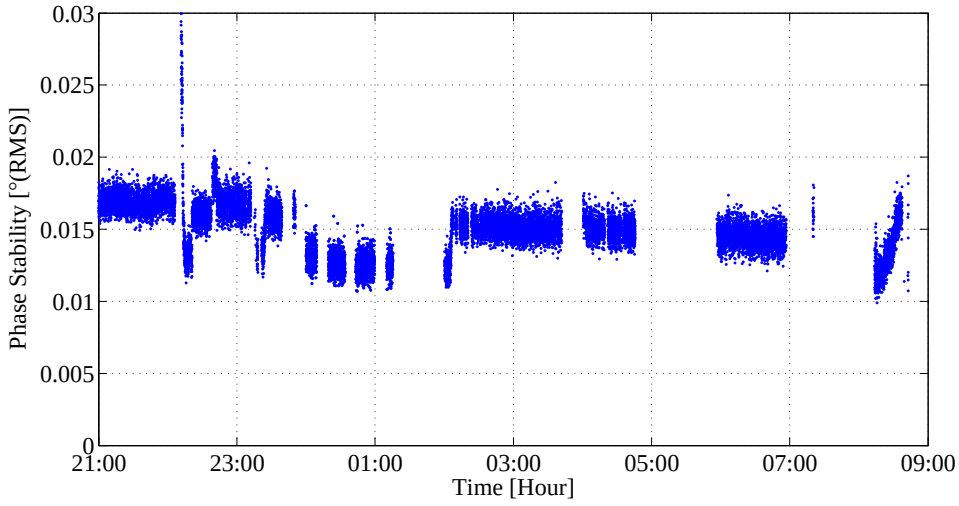


Figure 3.18: Long-term phase stability

Chapter 4

Digital LLRF Control System with IF-Mixture

In this chapter, the first successful digital LLRF control system with an IF-mixture algorithm controlling eight cavities is presented [24]. The motivation for proposing the digital LLRF control system using an IF-mixture technique is to reduce the number of ADCs. This reduction can make fabrication of the digital LLRF control system board less difficult. Furthermore, the number of digital LLRF boards in one RF station can also be reduced.

In the IF-mixture technique, several IFs are combined by a passive power combiner, and its output is connected to one ADC. The front-end for the IF-mixture technique is shown in Figure 4.1. The figure shows that four IFs are combined and fed into only one ADC. In this case, the required number of ADCs can be reduced by factor of four.

When several IF signals are combined and read by one ADC, the bit number used to quantize each IF signal decreases as the number of IF signals to be combined increases. If the number of IF signals is 2^K, the bit number used to quantize each IF decreases by K. In our design, we use a 16-bit ADC. We consider using four different IFs, in which case each IF signal can be quantized by 14 bits. Each IF signal that is quantized by 14 bits is still sufficient to fulfill the ILC stability requirements. The averaging effect in the I/Q converter also helps to reduce the ADC noise caused by the lower number of quantization levels.

A previous successful proof of concept of the IF-mixture technique was also presented at STF-KEK [25–28]. Preliminary studies of digital LLRF control systems with different IF techniques were performed at the STF. The first development of this technique was described in [25]. This paper reported successful implementation of the technique using two different IFs. To demonstrate the proof of concept, an FPGA-based cavity simulator was used. In this develop-

ment, the estimates of I and Q were updated at the least common multiple (LCM) of both signal periods (T_1 and T_2), where T_1 is the period of the first IF, and T_2 is the period of the second IF.

In [26], the technique was demonstrated using four different IFs. The performance was evaluated using four cavities. Only a proportional feedback controller was applied. By using Equations 2.7 and 2.8, the estimated I/Q value of each IF was updated at every L^{th} sampled signal (here, $L = 9$).

In [27], the performance of a system with four different IFs was compared with that of a system with a single IF. The system with four different IFs was similar to the system reported in [26].

In [28], a new feature of the system with four different IFs was that the estimated I/Q value of each IF was updated at every sampled signal, which reduces the latency. Different IFs are also selected in this paper on the basis of the intermodulation product. Furthermore, the LO phase noise was also considered in this paper. The performance was evaluated using one cavity to detect the combined signal of the cavity field, forward, and reflected signals.

The previous works on the IF technique were only proofs of the concept. At this stage, we believe that we can use the concept for the ILC.

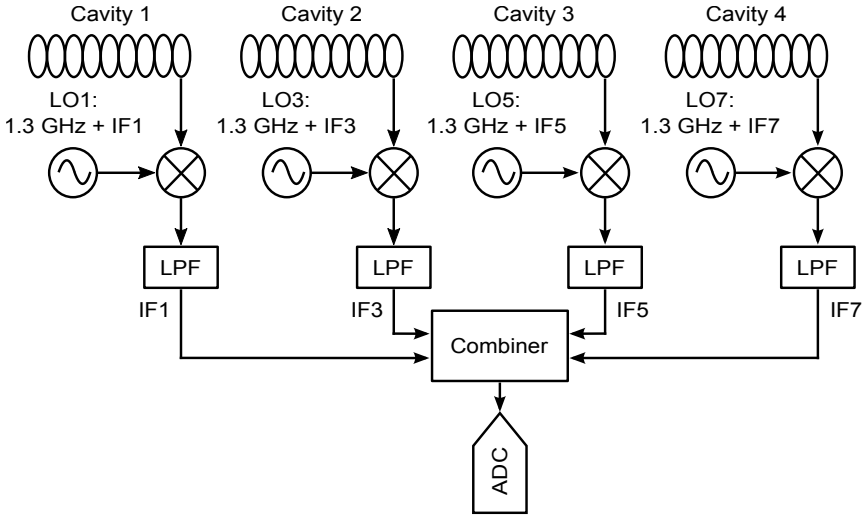


Figure 4.1: Front-end for multi-IF Technique. Each cavity output is mixed with a different LO frequency and filtered by an LPF with the corresponding frequency. Four IFs are combined by a passive power combiner, and its output is connected to one ADC.

4.1 Algorithm

One requirement for combining several signals is to avoid interference among them. To meet this requirement, the signals must be mutually orthogonal. The principle of IF-mixture is described in this section. Each IF signal can be represented as a complex wave:

$$x(t) = A(t)e^{j\omega t+\varphi} \tag{4.1}$$

where A is the amplitude, ω is the angular frequency, and φ is the angle at time $t = 0$ of the signal. The combination of a finite number of signals K can be expressed by a finite Fourier series as follows.

$$x(t) = \sum_{k=1}^{K} c_k e^{j\omega_k t} \tag{4.2}$$

where c_k is the coefficient of the k^{th} IF, and ω_k is the angular frequency of the k^{th} IF. The equation can be given in complex form as follows.

$$x(t) = a_0 + \sum_{k=1}^{K} [a_k \cos(\omega_k t) + b_k \sin(\omega_k t)] \tag{4.3}$$

The coefficient a_0, a_k, and b_k can be obtained:

$$a_0 = \frac{1}{2\pi}\int_{-\pi}^{\pi} x(t)dt \tag{4.4}$$

$$a_k = \frac{1}{\pi}\int_{-\pi}^{\pi} x(t)\cdot\cos(\omega_k t)dt \tag{4.5}$$

$$b_k = \frac{1}{\pi}\int_{-\pi}^{\pi} x(t)\cdot\sin(\omega_k t)dt \tag{4.6}$$

where $\omega_k = 2\pi f_k$ and f_k are defined as $f_k = \dfrac{N_k}{L}$, where $\dfrac{N_k}{L} = \dfrac{f_{\text{IF}_k}}{f_{\text{s}}}$. N_k and L are integers, f_{IF_k} is the k^{th} IF frequency, and f_{s} is the sampling frequency. The in-phase and quadrature components of each IF signal are $I_k = a_k$ and $Q_k = b_k$, respectively. The derivation of the calculation of I and Q is similar to that in subsection 2.2.1. If we assume that there is no DC offset in the combined signal ($a_k = 0$, in Equation 4.3), the signals in a discrete time are governed by the equation

$$\begin{aligned} X[n] &= \sum_{k=1}^{K} x_i[n] \\ &= \sum_{k=1}^{K} \left\{ I_k \cdot \cos\left(\frac{2\pi\cdot N_k}{L}\cdot n\right) - Q_k \cdot \sin\left(\frac{2\pi\cdot N_k}{L}\cdot n\right)\right\} \end{aligned} \tag{4.7}$$

where $X[n]$ is the n^{th} sample of the combined signal, $x_k[n]$ is the n^{th} sample of the k^{th} IF signal, I_k is the I component of the k^{th} IF, Q_k is the Q component of the k^{th} IF, and N_k is the N value of the k^{th} IF. From this combined signal, the I and Q values of each IF can be estimated using an approximation by applying the Reimann sum as explained in subsection 2.2.1.

$$I_k = \frac{2}{L}\sum_{n=0}^{L-1} x[n] \cdot \cos\left(\frac{2\pi \cdot N_k}{L} \cdot n\right) \tag{4.8}$$

$$Q_k = -\frac{2}{L}\sum_{n=0}^{L-1} x[n] \cdot \sin\left(\frac{2\pi \cdot N_k}{L} \cdot n\right) \tag{4.9}$$

These equations are identical to Equations 2.7 and 2.8. The FPGA implementation requires an I/Q converter module for each IF. This implies that more FPGA resources are required.

4.2 IF Selection

The goal of IF selection in the construction of a digital LLRF control system with IF-mixture is to obtain the best combination of IFs without interference among the IFs. In the selection process, the main consideration is the intermodulation product.

When two frequencies are fed to a nonlinear device, the intermodulation product will appear at the output. A typical output spectrum when two frequencies are fed to a nonlinear device is shown in Figure 4.2. Further information about the intermodulation product generated in the nonlinear device is given in [29]. The lower the order of the intermodulation product is, the higher the magnitude will be. In theory, the passive combiner is a linear device. However, a certain level of nonlinearity may exist in practical passive combiners, which may introduce intermodulation distortion among the IFs.

The ADC sampling rate is SR = 81.25 MHz, and $L = 18$. The possible IFs that can be generated using those parameters are listed in Table 4.1. Two possible IF combinations were considered. The first combination is composed of IF_1, IF_2, IF_3, and IF_4. The second combination is composed of IF_1, IF_3, IF_5, and IF_7.

The evaluation was done by providing a two-tone input as illustrated in Figure 4.3. There are two test points in the setup; test point 1 is the analog signal output from the combiner measured by the spectrum analyzer, and test point 2 is the I/Q converter output estimated by an algorithm using Equations 2.7 and

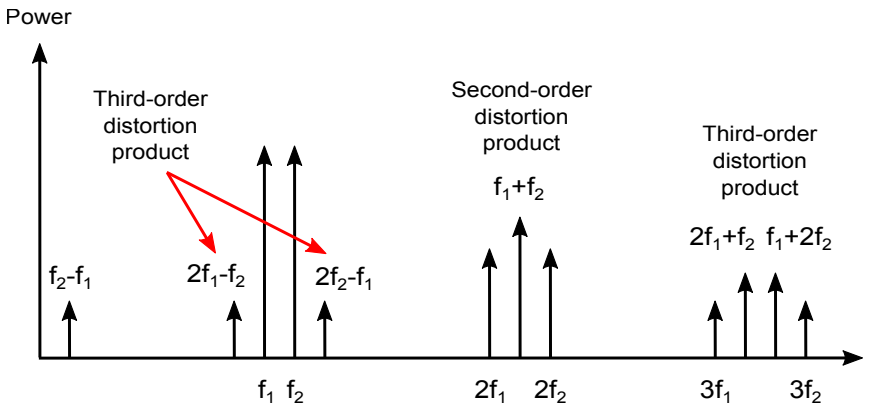


Figure 4.2: Output spectrum of nonlinear device when a two-tone input is provided.

Table 4.1: IFs that were selected with $L = 18$ and ADC sampling rate SR = 81.25 MHz.

IF	**Frequency** [MHz]
$\mathrm{IF}_1 = (1/L) \cdot \mathrm{SR}$	4.5
$\mathrm{IF}_2 = (2/L) \cdot \mathrm{SR}$	9.0
$\mathrm{IF}_3 = (3/L) \cdot \mathrm{SR}$	13.5
$\mathrm{IF}_4 = (4/L) \cdot \mathrm{SR}$	18.0
$\mathrm{IF}_5 = (5/L) \cdot \mathrm{SR}$	22.5
$\mathrm{IF}_6 = (6/L) \cdot \mathrm{SR}$	27.0
$\mathrm{IF}_7 = (7/L) \cdot \mathrm{SR}$	31.5
$\mathrm{IF}_8 = (8/L) \cdot \mathrm{SR}$	36.0

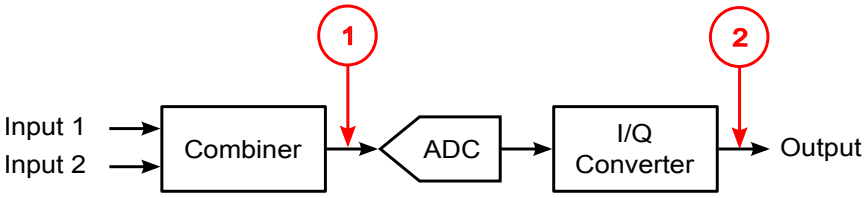


Figure 4.3: Two-tone measurement setup. Test point 1 is the output of the combiner and is measured by a spectrum analyzer. Test point 2 is the output of the I/Q converter and is estimated using Equations 2.7 and 2.8. The magnitude of the I/Q converter output is changed to dBFS.

2.8. The combiner used in the experiment was a ZMSC-4-1 from Mini Circuit, Inc. A photograph of the combiner is shown in Figure 4.4.

Figure 4.4: Photograph of combiner (ZMSC-4-1, Mini-Circuit).

Table 4.2 lists the results for test point 1 in the first IF combination (IF_1, IF_2, IF_3, and IF_4). The highest intermodulation product is approximately 80 dB under the input signals. The I/Q converter output is listed in Table 4.3. The highest intermodulation product is approximately 65 dB under the input signals.

Table 4.4 summarizes the results at test point 1 for the second IF combination (IF_1, IF_3, IF_5, and IF_7). The highest intermodulation product is approximately 80 dB under the input signal. The I/Q converter output is listed in Table 4.5. The highest intermodulation product is approximately 70 dB.

Concerning the intermodulation, the first IF combination (IF_1, IF_2, IF_3, and IF_4) might yield second- and third-order intermodulation products that interfere with other usable IFs. For the second combination (IF_1, IF_3, IF_5, and IF_7), only a third-order intermodulation product is possible. Therefore, the second combination was chosen to minimize the intermodulation products that can interfere with usable IFs.

Table 4.2: Power at combiner output (test point 1) with two-tone input measured by spectrum analyzer. The IFs are IF_1, IF_2, IF_3, and IF_4.

Input [MHz]	**IF Power Level at Output [dBm]**			
	IF_1	**IF_2**	**IF_3**	**IF_4**
	(4.5 MHz)	(9 MHz)	(13.5 MHz)	(18 MHz)
4.5	−6.8	−90.8	−91.0	−91.1
9	−89.9	−7.2	−91.3	−90.8
13.5	−90.2	−90.9	−7.8	−91.4
18	−89.1	−91.4	−91.0	−8.3
4.5 & 9	−7.6	−7.1	−89.7	−90.4
4.5 & 13.5	−7.5	−91.1	−8.2	−89.4
4.5 & 18	−7.3	−90.8	−91.0	−8.4
9 & 13.5	−87.2	−7.1	−7.6	−90.1
9 & 18	−89.8	−7.8	−91.2	−8.5
13.5 & 18	−88.9	−89.5	−7.7	−8.3

Table 4.3: Magnitude of each IF at I/Q converter output (test point 2) with two-tone input estimated by I/Q algorithm. The IFs are IF_1, IF_2, IF_3, and IF_4.

Input [MHz]	**IF Magnitude at Output [dBFS]**			
	IF_1	**IF_2**	**IF_3**	**IF_4**
	(4.5 MHz)	(9 MHz)	(13.5 MHz)	(18 MHz)
No Input	−72.8	−73.9	−75.4	−75.1
4.5	−0.1	−71.8	−74.1	−74.6
9	−72.9	−0.2	−65.9	−72.8
13.5	−73.3	−68.3	−0.5	−68.3
18	−74.6	−75.0	−74.4	−0.9
4.5 & 9	−0.3	−0.4	−65.9	−72.6
4.5 & 13.5	−0.3	−67.9	−0.8	−68.6
4.5 & 18	−0.3	−71.1	−72.8	−0.5
9 & 13.5	−72.1	0.0	−0.5	−67.5
9 & 18	−72.3	−0.3	−65.9	−0.6
18 & 18	−73.0	−67.2	−0.4	−0.4

Table 4.4: Power at combiner output (test point 1) with two-tone input measured by spectrum analyzer. The IFs are IF_1, IF_3, IF_5, and IF_7.

Input [MHz]	**IF Power Level at Output [dBm]**			
	IF_1	**IF_3**	**IF_5**	**IF_7**
	(4.5 MHz)	(13.5 MHz)	(22.5 MHz)	(31.5 MHz)
4.5	−6.8	−91.3	−90.6	−91.2
13.5	−89.9	−7.8	−91.3	−91.0
22.5	−89.3	−91.2	−7.2	−91.5
31.5	−89.8	−91.4	−91.2	−6.7
4.5 & 13.5	−7.6	−8.2	−91.0	−89.8
4.5 & 22.5	−7.3	−90.0	−7.0	−90.8
4.5 & 31.5	−7.3	−91.0	−90.5	−6.4
13.5 & 22.5	−88.0	−7.1	−7.3	−91.2
13.5 & 31.5	−88.5	−7.9	−91.2	−6.4
22.5 & 31.5	−90.1	−91.0	−7.0	−6.5

Table 4.5: Magnitude of each IF at I/Q converter output (test point 2) with two-tone input estimated by I/Q algorithm. The IFs are IF_1, IF_3, IF_5, and IF_7.

Input [MHz]	**IF Magnitude at Output [dBFS]**			
	IF_1	**IF_3**	**IF_5**	**IF_7**
	(4.5 MHz)	(13.5 MHz)	(22.5 MHz)	(31.5 MHz)
No Input	−72.1	−73.1	−75.2	−76.1
4.5	−0.2	−74.0	−74.6	−72.8
13.5	−72.6	−0.5	−73.4	−74.1
22.5	−74.4	−73.0	−0.3	−74.6
31.5	−74.6	−74.1	−71.0	0.0
4.5 & 13.5	−0.3	−0.7	−73.8	−73.3
4.5 & 22.5	−0.3	−72.8	0.0	−71.7
4.5 & 31.5	−0.3	−73.6	−71.2	0.2
13.5 & 22.5	−73.9	−0.4	−0.3	−73.6
13.5 & 31.5	−73.2	−0.5	−70.5	0.3
22.5 & 31.5	−74.8	−73.0	0.1	0.1

In Table 4.4, the measurement at test point 1 shows that the highest intermodulation product is approximately 80 dB. The intermodulation distortion produced by the combiner should not be a significant problem because the noise floor of the ADC output is approximately −70 dBFS, as shown in the first row of Table 4.5, where no input is connected to the combiner. The two-tone measurement results of the selected IFs presented in Table 4.1 indicate that they can be used in the digital LLRF control system with four different IFs.

The effectiveness of the algorithm can be evaluated by feeding one IF input to the ADC and comparing the IF output, as shown in the second to fifth rows of Table 4.5. The magnitude difference between the input IF and the others is about 70 dB, which is similar to the noise floor. This indicates that the algorithm can effectively select the desired frequency without any leakage to other frequencies.

4.3 LO Generation Setup

The goal of generating LOs for IF-mixture is to construct multiple LOs by a simple, low-cost method and synchronize them with the MO.

To distribute the ADC sampling clock and various frequencies for the LOs, a frequency divider (AD9510, Analog Devices, Inc. [30]) is used. Figure 4.5 shows a simplified schematic of LO generation for all the IFs.

In IF-mixture, the number of LOs depends on the number of IF signals used. Each LO is generated from the MO by dividing its frequency by the appropriate number. The first step is to generate the IF signals from the MO. Each IF signal is then mixed with the MO. IF_1 and IF_3 can be generated by directly dividing the MO frequency by 288 and 96, respectively. IF_5 and IF_7 cannot be generated directly by dividing the MO frequency. To generate those IFs, mixing with another frequency is required after division. IF_5 is generated by mixing with IF_2 and IF_3. IF_7 is generated by mixing with IF_3 and IF_4.

Because this LO generation procedure involves several mixers and frequency dividers, filters are necessary to block unwanted frequencies. Both ready-made and customized filters are used in LO generation. Figure 4.6 shows a photograph of a ready-made filter manufactured by Mini-Circuit. Customized narrow bandwidth (BW = 4 MHz) bandpass filters (BPFs) of 1304.5 MHz, 1313.5 MHz, 1322.5 MHz, and 1331.5 MHz (Sogo Electronics, Inc. [31]) are used for LO1, LO3, LO5, and LO7, respectively. Figure 4.7 shows a photograph of a customized filter. The measured bandwidth is approximately 4.2 MHz, which meets the design specification. All the devices for generating the LOs are placed in a 19-in. rack, as shown in Figure 4.8.

The motivation for evaluating LO generation in this section is to examine

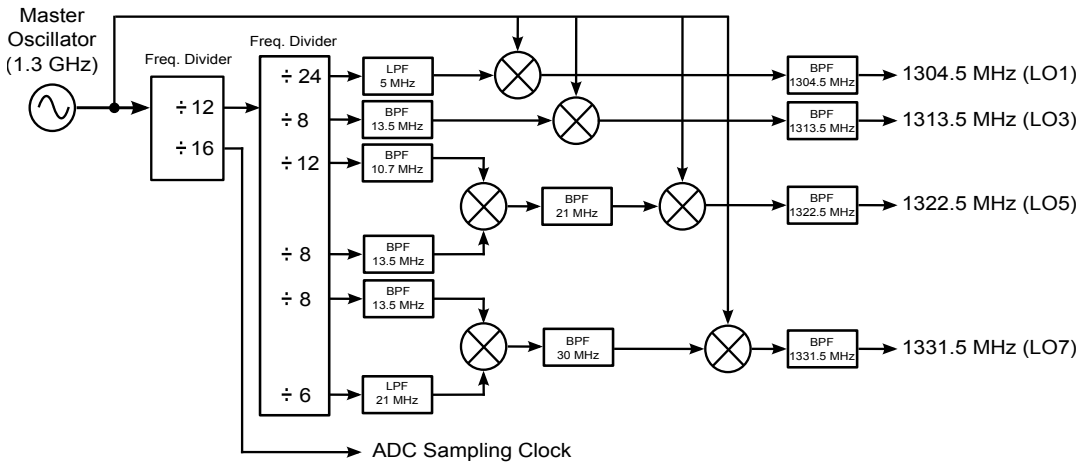


Figure 4.5: LO generation for multi-IF technique.

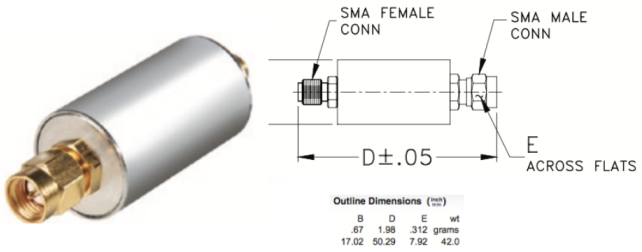


Figure 4.6: Photograph of filter manufactured by Mini-Circuit.

the performance of the LO generation process. A network analyzer is used to investigate the filter performance. The frequency responses of these filters are displayed in Figure 4.9. To increase the roll-off, two filters are cascaded, and the frequency responses are shown in Figure 4.10. The filters' performance meets the design specification. In the implementation, two filters are cascaded.

An important parameter of the LO is the phase noise, which directly affects the IF estimation. The phase noise of the LO for IF-mixture was measured using an Agilent Technology E5052A signal source analyzer, and the result is shown in Figure 4.11. The phase noise was compared with that of the MO. The results are shown in Figure 4.11. Within an offset frequency interval of 10 Hz to 1 MHz, the RMS jitter of each LO does not significantly differ from that of the MO, as listed in Table 4.6. The RMS jitter difference between each LO and the MO is only 1–2 fs, which corresponds to 4.7×10^{-4} deg to 9.6×10^{-4} deg. It can be inferred that the proposed LO generation circuit added little phase noise.

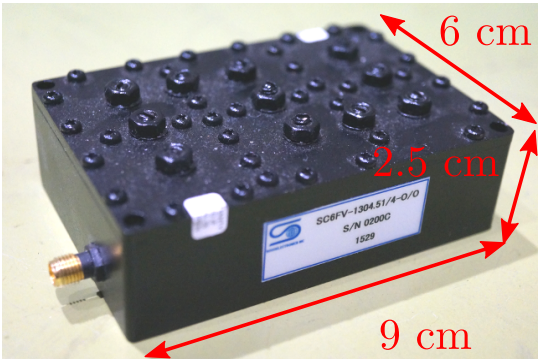


Figure 4.7: Customized 1304.5 MHz filter from Sogo Electronics, Inc. The designed filter bandwidth is 4 MHz.

Table 4.6: RMS jitter and phase of MO and LO within an offset frequency interval of 10 Hz to 1 MHz

Signal	**Frequency** [MHz]	ΔT_{RMS} [fs]	$\Delta\phi_{\mathrm{RMS}}$ [°]
MO	1300.0	56	0.026
LO1	1304.5	57	0.027
LO3	1313.5	57	0.027
LO5	1322.5	57	0.027
LO7	1331.5	58	0.027

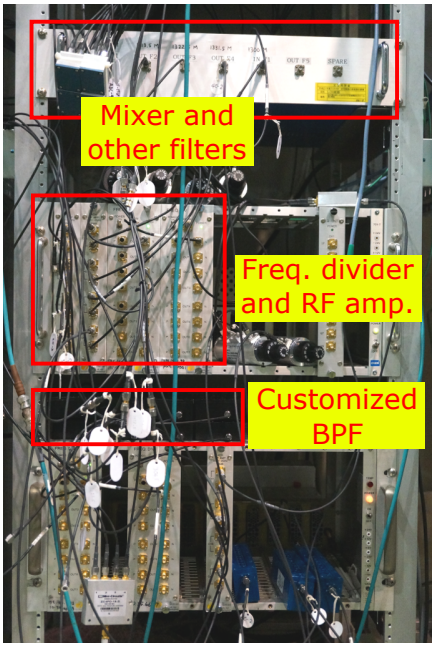


Figure 4.8: Photograph of setup for LO generation for multi-IF technique.

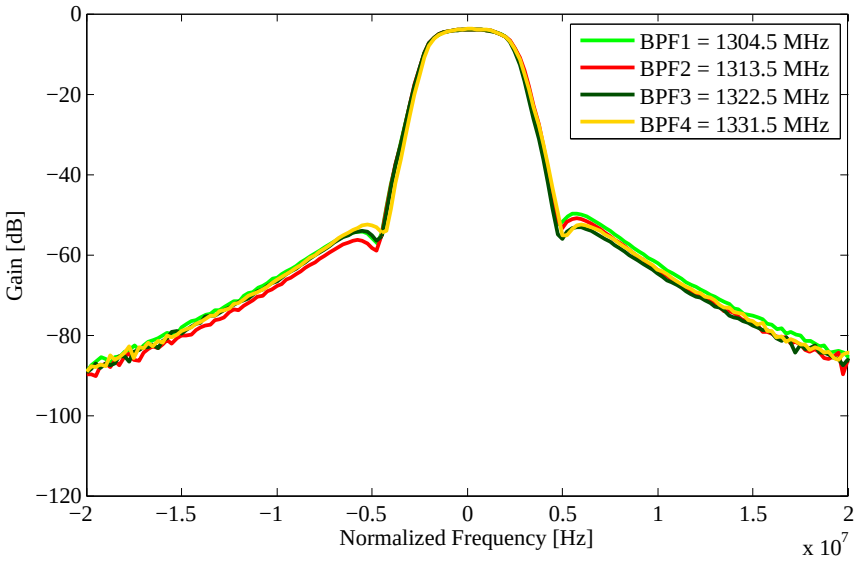


Figure 4.9: Frequency response of single filter. The filter frequencies are normalized.

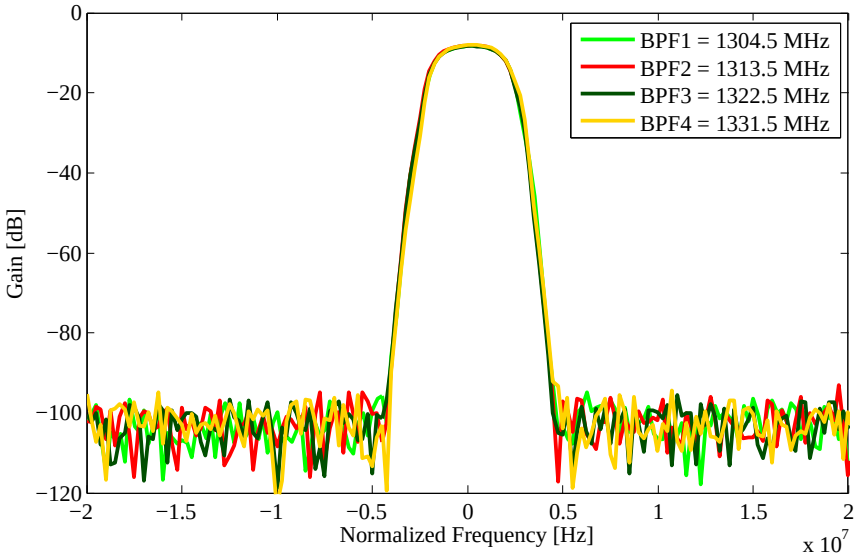


Figure 4.10: Frequency response of two cascaded filter. The filter frequencies are normalized.

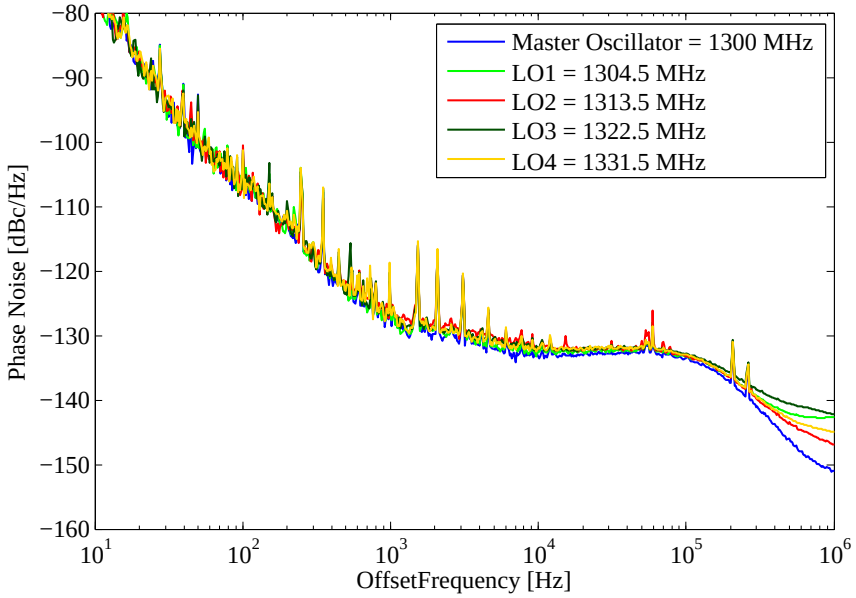


Figure 4.11: MO and LO phase noise. MO = 26.3 mdeg, LO1 = 27.3 mdeg, LO2 = 27.9 mdeg, LO3 = 27.8 mdeg, LO4 = 27.9 mdeg.

4.4 Digital LLRF System Setup

The IF-mixture technique was implemented on an MTCA.0-compliant digital LLRF board. The board features a Virtex XC5FX-70T FPGA (Xilinx, Inc. [32]), four 16-bit ADCs (LT2208, Linear Technology, Inc. [33]), and four 16-bit DACs (AD9783, Analog Device, Inc. [23]). The system clock and ADC sampling frequency are 81.25 MHz. This system was also used in the Quantum Beam project. The performance of this system was evaluated in [34].

Figures 4.12 and 4.13 show a photograph and a block diagram of the board, respectively. In this thesis, implementation of the IF-mixture technique can increase the number of input channels by a factor of four. Thus, this digital LLRF board can accommodate 16 input channels.

Figure 4.12: Digital LLRF board meeting MTCA.0 standard.

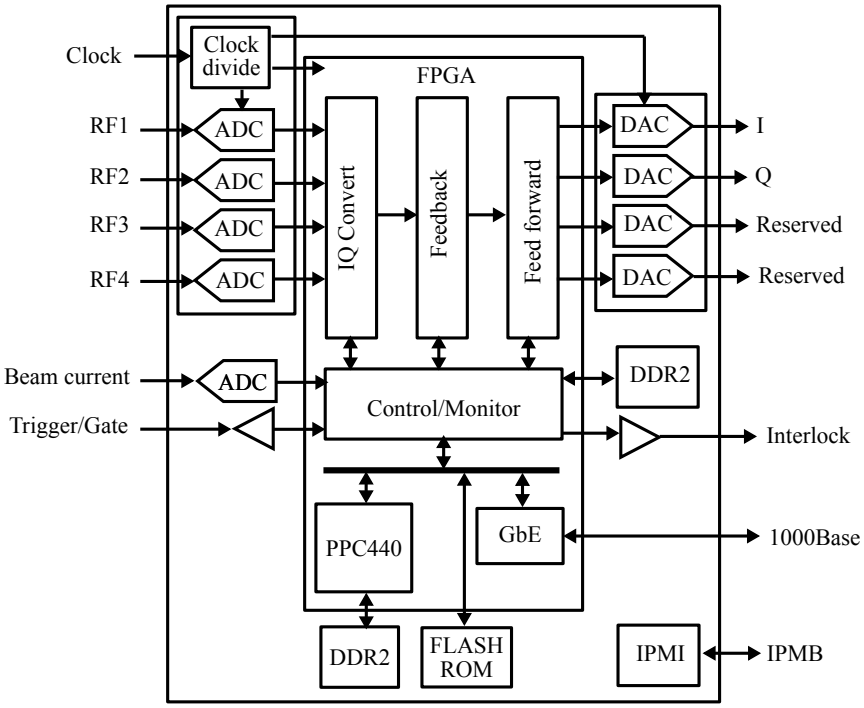


Figure 4.13: Block diagram of digital LLRF board with MTCA.0 configuration. The board is equipped with four ADCs and four DACs.

4.5 Performance Evaluation

The motivation for the performance evaluation is to confirm that the digital LLRF control system using IF-mixture can provide the RF stability required by the ILC.

The performance of the IF-mixture technique was evaluated during cavity conditioning at STF-KEK. The IF-mixture algorithm was implemented on a board that complies with the MTCA.0 standard for hardware. This board uses an 81.25 MHz FPGA sampling clock. The phase noise measurement of this clock is shown in Figure 4.14. The RMS jitter resulting from phase noise between 10 Hz and 1 MHz is 114 fs, which corresponds to 3.3 mdeg. The number of cavities was eight; therefore, two ADCs were used during operation. ADC1 was connected to cavities #1, #2, #3, and #4 through a combiner. ADC2 was connected to cavities #8, #10, #11, and #12 through a combiner.

The waveform amplitude and phase of the eight cavities are shown in Figures 4.15 and 4.16, respectively. The amplitude and phase of the vector sum in the flattop region are shown in Figure 4.17. The stabilities obtained using the IF-mixture technique are 0.006 % (RMS) and 0.046° (RMS), which fulfill

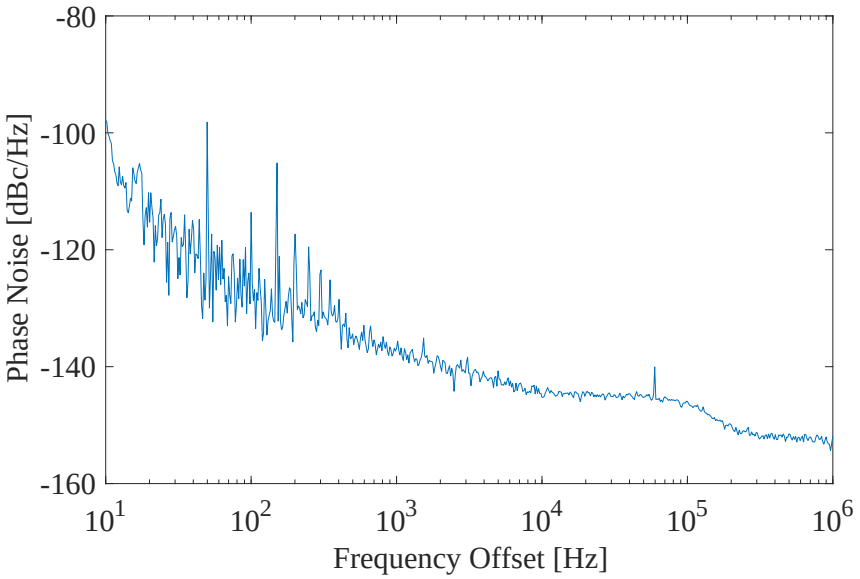


Figure 4.14: Phase noise of 81.25 MHz sampling clock. The RMS jitter from 10 Hz to 1 MHz is 114 fs.

the ILC requirements. The stability was calculated at the flattop from 1100–1650 µs.

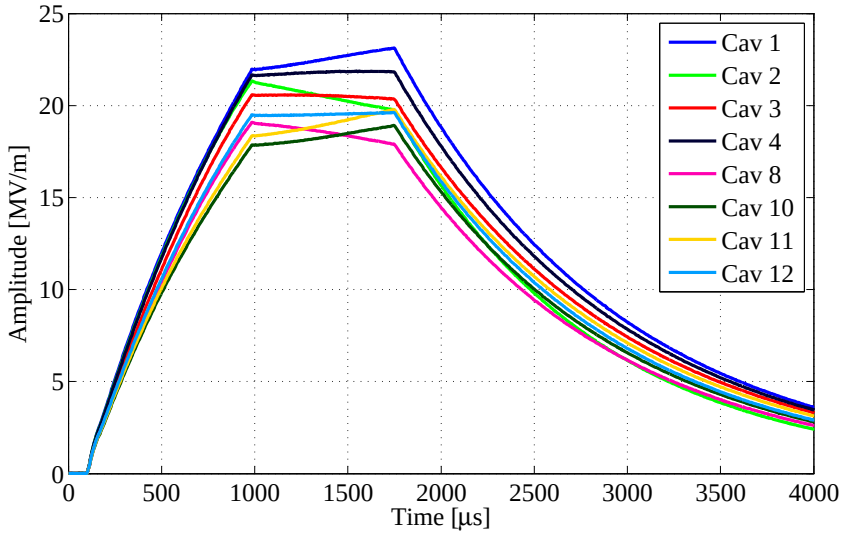


Figure 4.15: Amplitude waveform of eight cavities.

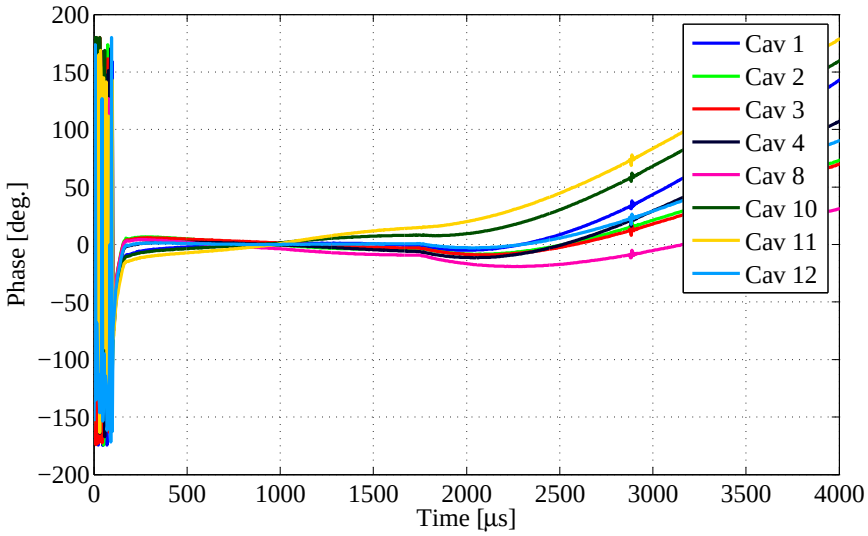


Figure 4.16: Phase waveform of eight cavities.

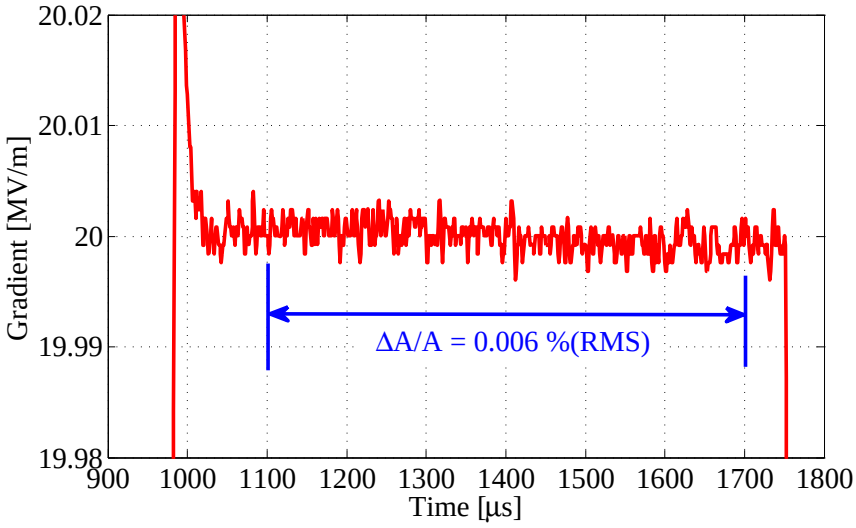


Figure 4.17: Amplitude of vector sum in flattop region.

4.6 Summary

A digital LLRF control system using the IF-mixture technique was constructed. The IFs were selected by considering the intermodulation product. The proposed LOs were generated by a simple, low-cost method and synchro-

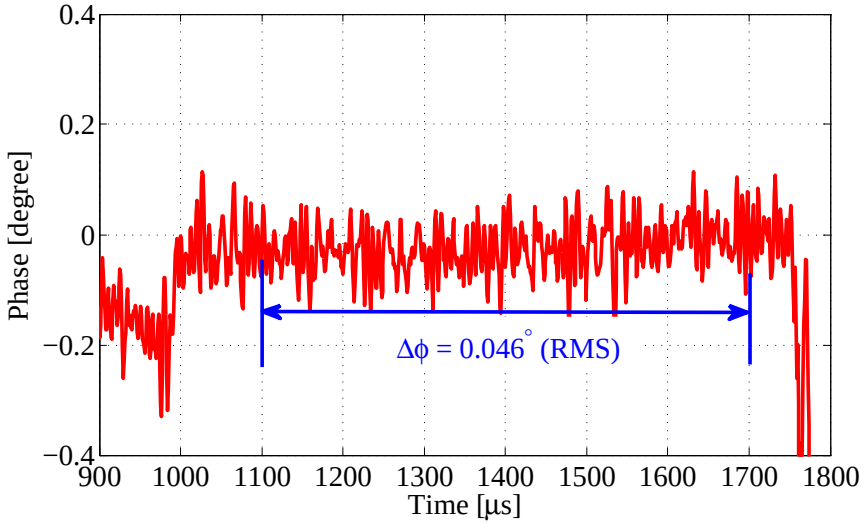


Figure 4.18: Phase of vector sum in flattop region.

nized with the MO. This is adequate for realization of the IF-mixture technique. The achieved amplitude and phase stabilities are 0.006 %(RMS) and 0.046 deg(RMS), respectively. These values fulfill the ILC requirements.

Chapter 5

Direct Sampling

The development of the direct sampling method at the STF began with an evaluation of a fast ADC with a commercial FPGA board, as reported in [35]. This development was continued in [36], which reported the evaluation of different sampling frequencies. The development and evaluation of direct sampling implemented on an MTCA.0-compliant FPGA board was reported in [19].

In a typical digital LLRF control system, the high-frequency signal to be monitored is translated to an IF by a down-converter. The characteristics of the down-converter such as temperature dependence and nonlinearity can add to the error in the detection field. One way to avoid this error is to eliminate the down-converter, which also simplifies the structure of the system.

The motivation for applying the direct sampling technique is to eliminate the down-converter so that the additional error in signal estimation resulting from the down-converter's characteristics can be avoided. Furthermore, the system becomes simpler because the LO is not required. The main issue in the direct sampling technique is the demanding ADC specifications for of the speed, bandwidth, and resolution. ADCs with the necessary speed ($> 400\,\mathrm{MSPS}$), bandwidth ($> 1.3\,\mathrm{GHz}$), and resolution ($> 12\,\mathrm{bits}$) have recently become available [37]. The front-end direct sampling technique is illustrated in Figure 5.1. Another drawback of the direct sampling technique is that the ADC SNR is lower because it is operated at a high-frequency input. The SNR of the ADC is directly related to the input frequency, as shown by the following equation.

$$\mathrm{SNR(dBFS)} = -20 \cdot \log_{10}(2 \cdot \pi \cdot f_{\mathrm{in}} \cdot \sigma_{\mathrm{jitter}}) \tag{5.1}$$

where f_{in} is the input frequency, and σ_{jitter} is the total jitter, which consists of the ADC aperture jitter, sampling clock jitter, and input frequency jitter. To reduce the ADC noise, a digital filter was implemented for direct sampling.

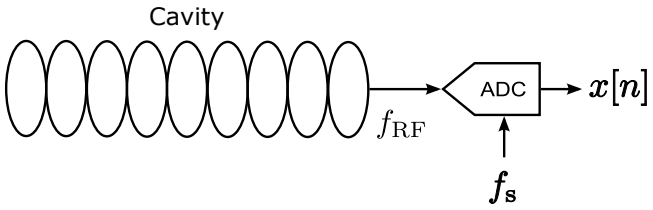


Figure 5.1: Front-end for direct sampling technique. The signal from the cavity is fed directly to the high-speed, wide-bandwidth ADC. f_{RF} is the input signal, f_{s} is the sampling clock, and $x[n]$ is the sampled signal.

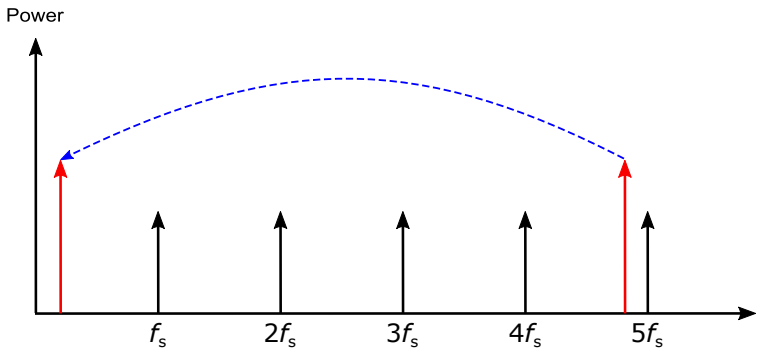


Figure 5.2: Direct sampling technique will translate the sampled signal to the first Nyquist band.

Even though the available ADC can perform sampling at a very high speed, it is still not fast enough to satisfy the Nyquist rate. Therefore, the undersampling technique is used [38].

In the undersampling technique, the frequency of the signal to be sampled is higher than the Nyquist frequency (half the sampling frequency). In terms of the frequency domain, the undersampling process translates the sampled signal to the first Nyquist band, as illustrated in Figure 5.2. For example, an ADC input signal with a frequency of 1300 MHz is sampled at a sampling frequency of 270.83 MHz. The input signal lies in the tenth Nyquist zone (1354.1 MHz). Undersampling translates the sampled signal to the first Nyquist zone (54.1 MHz).

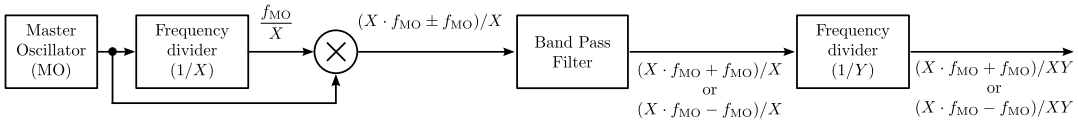


Figure 5.3: Clock generation for direct sampling

5.1 Sampling Frequency

The relationship between the sampling frequency (f_s) and the MO (f_{MO}) is given by

$$f_s = \left(f_{MO} \pm \frac{f_{MO}}{X} \right) \frac{1}{Y} \tag{5.2}$$

where X and Y are the division values of the frequency divider. Clock generation for direct sampling can be implemented as shown in Figure 5.3. The I and Q components of the sampled signal can be estimated using Equations 2.7 and 2.8, respectively.

The direct sampling experiment uses sampling at two frequencies: 172 MHz and 270 MHz. The phase noise at these sampling frequencies was measured, and the result is shown in Figure 5.4. The jitter of the 172 MHz clock is approximately $\Delta T_{RMS} = 68$ fs, which corresponds to 4.3 mdeg. The jitter of the 270 MHz sampling rate is approximately $\Delta T_{RMS} = 70$ fs, which corresponds to 8.4 mdeg. Both jitter estimations were calculated within an offset frequency range of 10 Hz to 1 MHz. According to the result, the additional phase error does not seem to be significant. For direct sampling, the value can be significant because the ADC input frequency is very high (1300 MHz).

The SNR of the ADC limited by jitter can be calculated using Equation 5.1. If the sampling clock jitter is not considered ($\sigma_{clk} = 0$), the maximum SNR limited by the ADC aperture jitter and input jitter is approximately 60.3 dB. The total jitter in the ADC consists of the sampling clock jitter, the aperture jitter of the sample-and-hold switch at the input of the ADC, and the input frequency jitter. The total jitter is written as

$$\sigma_{jitter} = \sqrt{(\sigma_{ADC})^2 + (\sigma_{clk})^2 + (\sigma_{in})^2} \tag{5.3}$$

where σ_{jitter} is the total jitter, σ_{ADC} is the ADC aperture jitter, σ_{clk} is the sampling clock jitter, and σ_{in} is the input frequency jitter. In this experiment, the ADS5474 ADC from Texas Instruments was used [37]. This ADC has an aperture jitter of 103 fs. The SNR of the ADC calculated from the total jitter

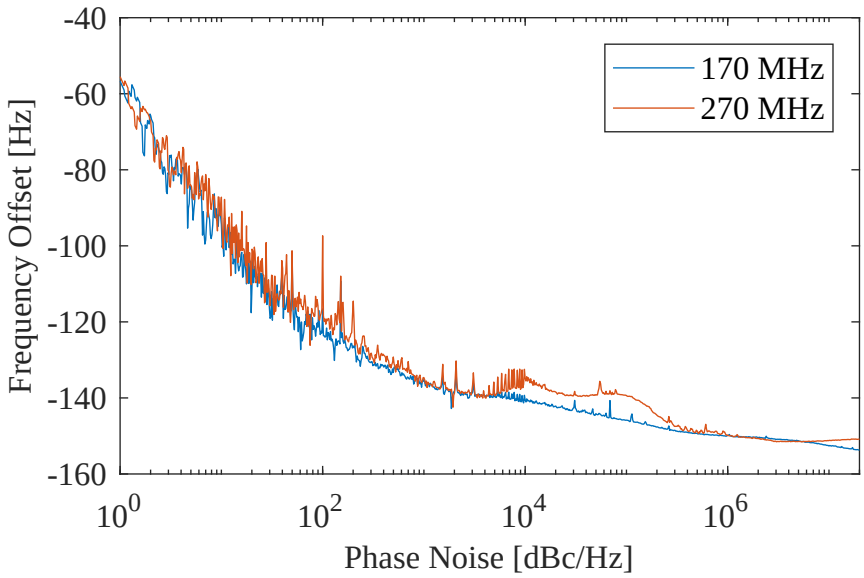


Figure 5.4: Phase noise at sampling frequencies used for direct sampling, 172 MHz and 270 MHz.

is approximately 59.1 dB. This means that the sampling clock jitter reduces the SNR by less than 2 dB. Thus, it can be inferred that the sampling clock is acceptable.

To generate the 270 MHz sampling frequency, a BPF at 1083 MHz is necessary. Figure 5.5 shows a photograph of the BPF. To generate the 172 MHz sampling frequency, a BPF at 1381 MHz is required.

5.2 Digital LLRF System Setup

The digital LLRF system for monitoring by using the direct sampling algorithm was implemented on an MTCA.0-compliant board [18]. This board features a DSP consisting of a Virtex XC5FX-70T FPGA (Xilinx, Inc. [32]) and 2 14-bit ADCs (ADS5474, Texas Instruments, Inc. [37]). This ADC has an input bandwidth of 1.4 GHz and a sampling rate of up to 400 MSPS. Figures 5.6 and 5.7 show a photograph and a block diagram of the board, respectively.

5.3 System Monitoring

Direct sampling is used for monitoring, and feedback is performed by a typical system with MTCA.4-based hardware. The direct sampling boards are

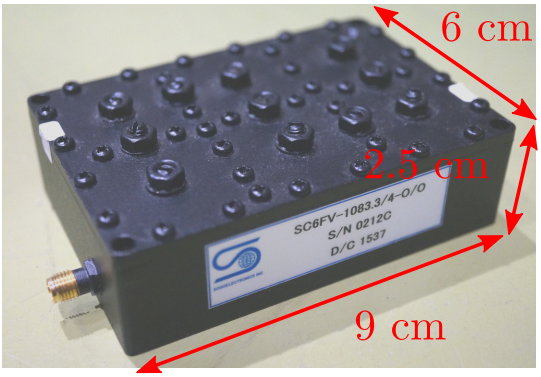


Figure 5.5: Customized 1083 MHz filter from Sogo Electronics, Inc. The designed filter bandwidth is 4 MHz.

Figure 5.6: MTCA.0-compliant digital LLRF board for direct sampling.

equipped with two ADCs; one ADC is connected to cavity #1, and the other is connected to cavity #8. A 4^{th}-order conjugate filter is implemented in the system, and the filter bandwidth is set to 250 kHz.

In this measurement, the MTCA.4-compliant board was compared with the direct sampling board. Cavity #1 was operated with feedback control. For the direct sampling board, both filtered and unfiltered operation were compared. The result is shown in Figure 5.8. The filter implemented on the direct sampling board can effectively reduce the ADC noise, as shown in Figure 5.8(c) and 5.8(d). Amplitude and phase stabilities of 0.021 %(RMS) and 0.17 °(RMS), respectively, can be achieved in the direct sampling system. These values are similar to those of the MTCA.4 board in the typical system. The noise in the

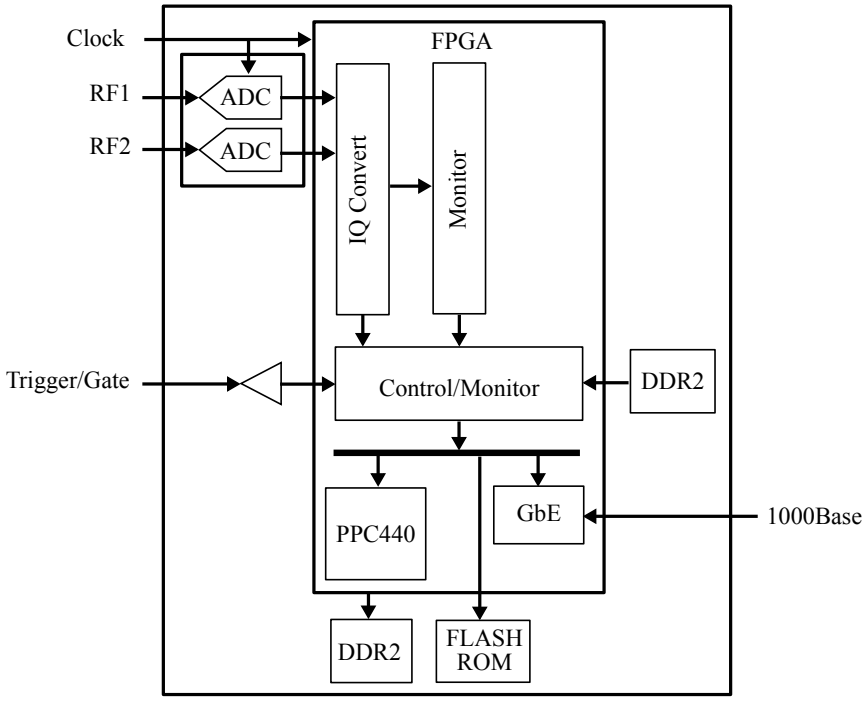
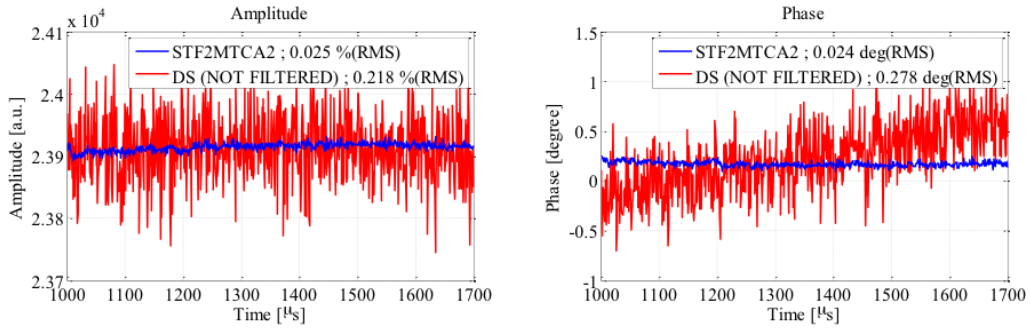


Figure 5.7: Block diagram of MTCA.0-compliant board for direct sampling.

phase can also be reduced effectively by the filter, but there is a tilt. This tilt could be caused by the difference in clock distribution between the feedback controller (MTCA.4) and the monitor system (direct sampling).

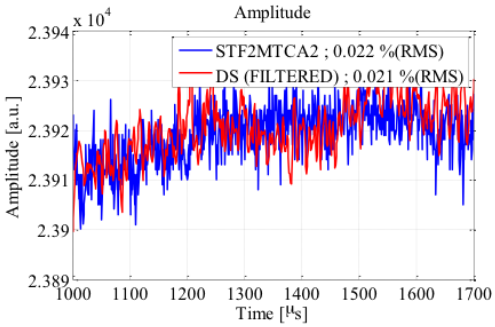
The amplitude stability achieved by the direct sampling method can fulfill the ILC requirement. Even if the phase stability is calculated with the tilt included, it can still fulfill the ILC requirement. However, if the tilt problem is solved, the achieved phase stability will be significantly better. The tilt problem might not arise from the direct sampling board because it also occurred on another board when it was used for monitoring. If the tilt is not considered in the stability calculation, the phase stability is 0.050° (RMS).

Figure 5.9 compares the performance of STF2MTCA2 and direct sampling for cavity #8. The difference in the flattop length between STF2MTCA2 and the direct sampling configuration is caused by the scaling factor in the direct sampling setting.

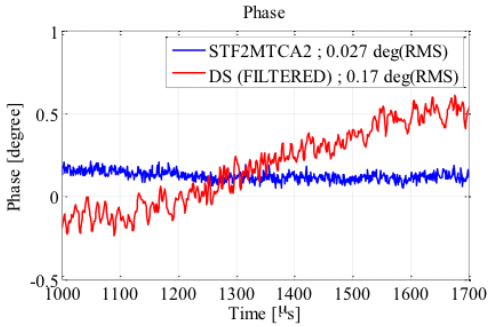


(a) Amplitude

(b) Phase



(c) Amplitude



(d) Phase

Figure 5.8: Comparison of amplitude and phase of STF2MTCA2 and direct sampling for cavity #1 with (a) and (b) the direct sampling filter off and (c) and (d) the direct sampling filter on.

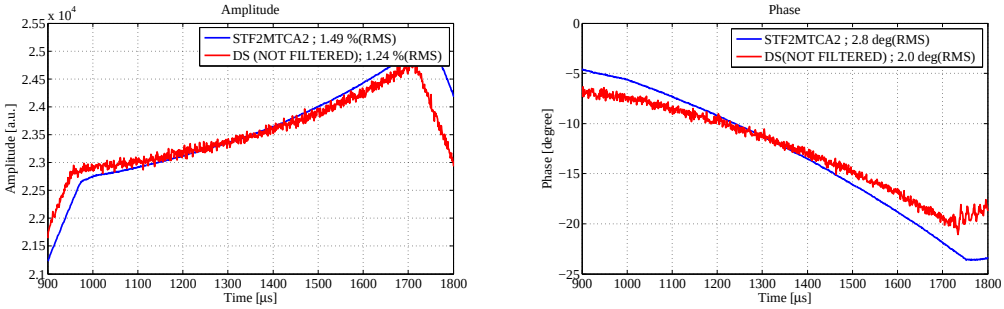
5.4 LO and MO Monitor with Direct Sampling

The signal stability can be evaluated in either the frequency or the time domain. A signal source analyzer is an effective device for observing the stability in the frequency domain for short time periods. Observation of the long-term drift in the time domain is also important. The direct sampling system is useful for long-term monitoring of the MO and LO because it is not affected by the characteristics of the down-converter. This section describes the MO and LO monitoring system with direct sampling at a single sampling frequency.

In the I/Q estimation method, the sampling frequency can be determined as follows.

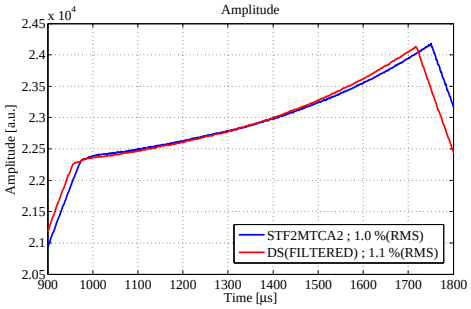
$$f_{\mathrm{s}} = \frac{f_{\mathrm{IN}}}{K + \frac{N}{L}}, \ K = 0, 1, 2, \ldots \tag{5.4}$$

where f_{IN} is the input frequency and f_{s} is sampling frequency. The phase

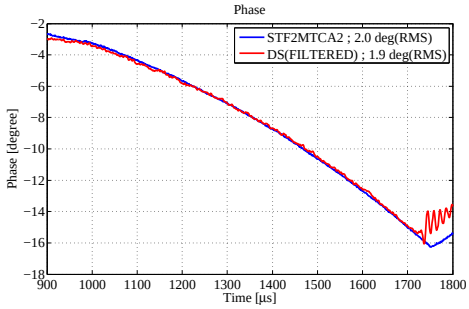


(a) Amplitude

(b) Phase



(c) Amplitude



(d) Phase

Figure 5.9: Comparison of amplitude and phase of STF2MTCA2 and direct sampling for cavity #8 with (a) and (b) the direct sampling filter off and (c) and (d) the direct sampling filter on.

difference between two adjacent samples is defined as

$$\Delta\phi = \left(K + \frac{N}{L}\right) \cdot 2\pi \tag{5.5}$$

We used an f_{LO} value of 1310.16 MHz, which was obtained by mixing the MO and $f_{\mathrm{MO}}/128$. It can be written as $f_{\mathrm{LO}} = 129/128 \times f_{\mathrm{MO}}$. The LO coefficient for I/Q estimation is determined as follows.

$$\frac{f_{\mathrm{LO}}}{f_{\mathrm{s}}} = \frac{129}{128} \cdot f_{\mathrm{MO}} \Bigg/ \frac{f_{\mathrm{MO}}}{K + \frac{N}{L}} = \left(K + \frac{N}{L}\right) \cdot \frac{129}{128} \tag{5.6}$$

Consequently, $(KL + N) = 128$, so the coefficient for the LO is $129/L$, and the coefficient for the MO is $128/L$.

The relationship between the sampling frequency (f_{s}) and the frequency of the MO can be expressed as follows.

$$f_{\mathrm{s}} = \left(f_{\mathrm{MO}} \pm \frac{f_{\mathrm{MO}}}{X}\right) \frac{1}{Y} = \left(\frac{X \pm 1}{XY}\right) \cdot f_{\mathrm{MO}} \tag{5.7}$$

Table 5.1: Possible sampling frequencies for direct sampling.

Operating freq. 1300 MHz					
X		(X ± 1)/X freq. [MHz]	Y	Sampling freq. [MHz]	
32	+	1340.6	4	335.16	×
32	–	1259.4	4	314.84	×
16	+	1381.3	8	172.66	✓
16	–	1218.8	8	152.34	✓
8	+	1462.5	16	91.41	✓
8	–	1137.5	16	71.09	✓
4	+	1625.0	32	50.78	×
4	–	975.0	32	30.47	✓

where X and Y are the parameters of the frequency divider. The realization of Equation 5.7 is shown in Figure 5.3.

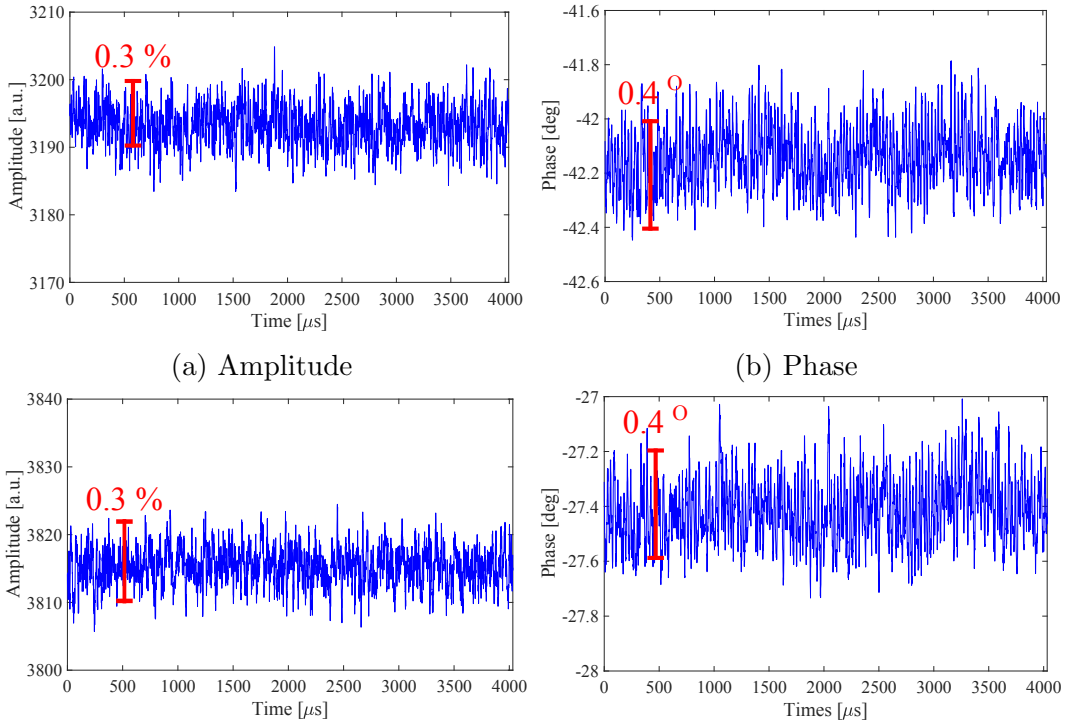
Sampling clock generation can be implemented as follows.

1. The MO frequency is divided by X to obtain f_{MO}/X
2. The frequency of f_{MO} is then mixed with f_{MO}/X to obtain $(X \cdot f_{\mathrm{MO}} \pm f_{\mathrm{MO}})/X$.
3. The output of the mixer is then filtered wby the BPF to choose $(X \cdot f_{\mathrm{MO}} + f_{\mathrm{MO}})/X$ or $(X \cdot f_{\mathrm{MO}} - f_{\mathrm{MO}})/X$.
4. The output of the BPF is then divided by Y. The sampling frequency is either $(X \cdot f_{\mathrm{MO}} + f_{\mathrm{MO}})/XY$ or $(X \cdot f_{\mathrm{MO}} - f_{\mathrm{MO}})/XY$.

From these steps, $XY = KL+N = 128$, and the possible combinations of X and Y used to obtain different sampling frequencies are listed in Table 5.1. Here, the sampling frequencies 335.16 MHz and 314.84 MHz are not chosen because they are close to the maximum sampling frequency of the ADC (ADS5474). The sampling frequency of 50.78 MHz also cannot be used because the maximum input frequency of the divider (AD9510) is 1.6 GHz. Therefore, we chose the highest sampling frequency among the candidates, which is 172.66 MHz ($K = 7, L = 17,$ and $N = 9$).

The MO and LO stability results are shown in Figure 5.10. In this measurement, the digital filter was not implemented. For the MO, the amplitude and phase stabilities are 0.089 % (RMS) and 0.11° (RMS), respectively. For the LO, the amplitude and phase stabilities are 0.068 % (RMS) and 0.097° (RMS),

respectively. These results do not satisfy the ILC stability requirements. To improve them, the digital filter can be used. When a filter with a bandwidth of 250 kHz is used, amplitude stability on the order of 0.02 % (RMS) and phase stability on the order of 0.02° (RMS) are expected.



(a) Amplitude (b) Phase

(c) Amplitude (d) Phase

Figure 5.10: Amplitude and phase of (a) and (b) MO and (c) and (d) LO detected by direct sampling with the same sampling clock.

5.5 Summary

A direct sampling technique for signal monitoring was prepared, and the performance was estimated. Furthermore, direct sampling for MO and LO signal monitoring using a single sampling frequency was also developed, and the performance was estimated.

Chapter 6

Filling on Resonance

The klystron power requirement depends directly on the energy required for beam acceleration. The minimum required klystron power for beam acceleration is determined during beam acceleration (flattop). In the ILC, the klystron will be working near the saturation point to obtain higher efficiency.

The superconducting cavity is operated at the designed cavity gradient. To achieve that gradient, a filling time is necessary. The amount of klystron power during the filling time depends on the length of the filling time, the loaded quality, and the detuning, as shown in Equation 2.80. The best efficiency is achieved when the klystron power during the filling time and the klystron power during the flattop are the same.

The motivation for applying the filling on resonance method is to reduce the klystron power during the filling time in order to avoid exceeding the klystron's saturation level.

When the cavity is detuned, a larger RF power is required during the filling time to fill the cavity to the dedicated voltage. Consequently, the klystron can exceed its saturation level. According to Equation 2.80, the klystron power can be reduced by adjusting the filling time T_{fill}. This adjustment is not possible because in the ILC TDR, the filling time is determined to be 924 ms. The loaded quality Q_{L} can also be adjusted to reduce the klystron power during the filling time. However, this adjustment can affect both the cavity time constant and power coupling factor. In the ILC TDR, Q_L is determined to be 5.5×10^6. The other method of reducing the klystron power during the filling time is to make the cavity in resonance, that is, the so-called filling on resonance method [**?**]. In this chapter, the filling on resonance method is described. Either feed-forward or feedback control was applied during the experiment. The discussion is preceded by sections on the cavity detuning measurement and microphonics evaluation.

6.1 Cavity Detuning

The motivation for the cavity detuning measurement is to understand the cavity detuning pattern, which will be used to apply the filling on resonance method. Before the method is applied, the detuning pattern of the cavities must be known.

The cavity detuning during the pulse can be estimated using Equation 2.74. Figure 6.1 shows the cavity detuning during the pulse of eight cavities. The measurement was made using feed-forward control. The differences in the quality factor among the cavities leads to the differences in the detuning patterns.

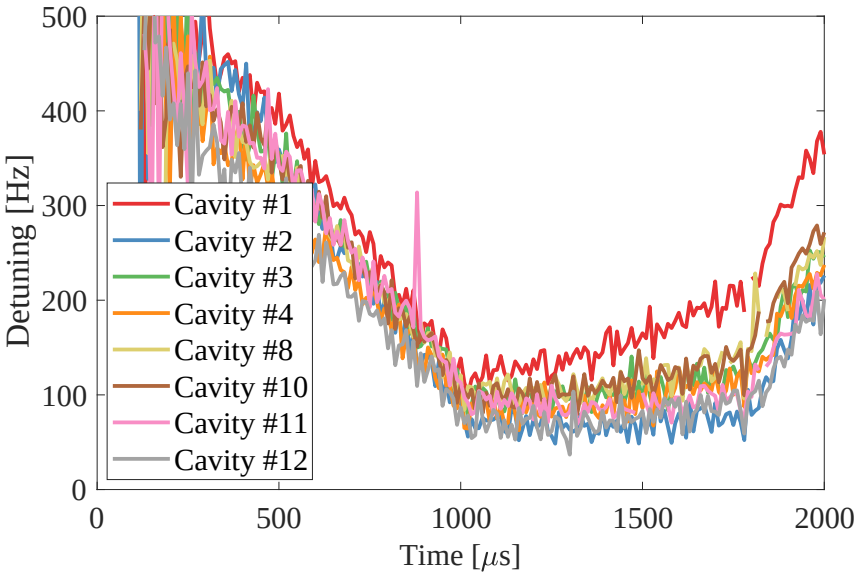


Figure 6.1: Detuning of eight cavity

6.2 Microphonics Evaluation

Microphonics is the modulation of the resonance frequency by external mechanical disturbances. Sources of disturbance include the helium pressure, ground motion, and man-made machinery.

In terms of control, to stabilize the amplitude and phase of the accelerating field in the detuned cavity caused by microphonics or Lorentz force detuning, the controller gives a signal to the klystron to increase its power.

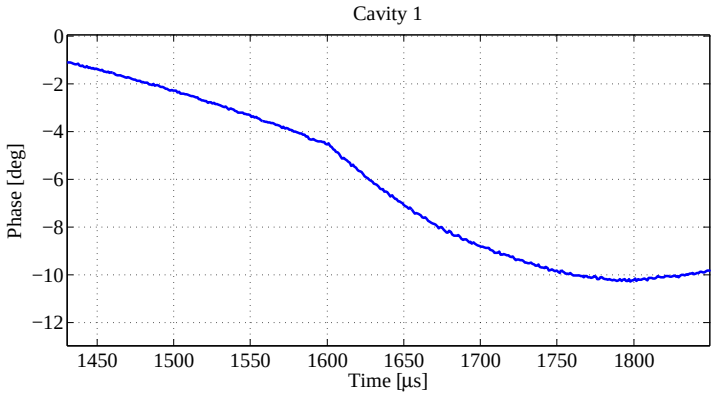


Figure 6.2: The example of phase decay after the RF power is turned off at 1600 µs

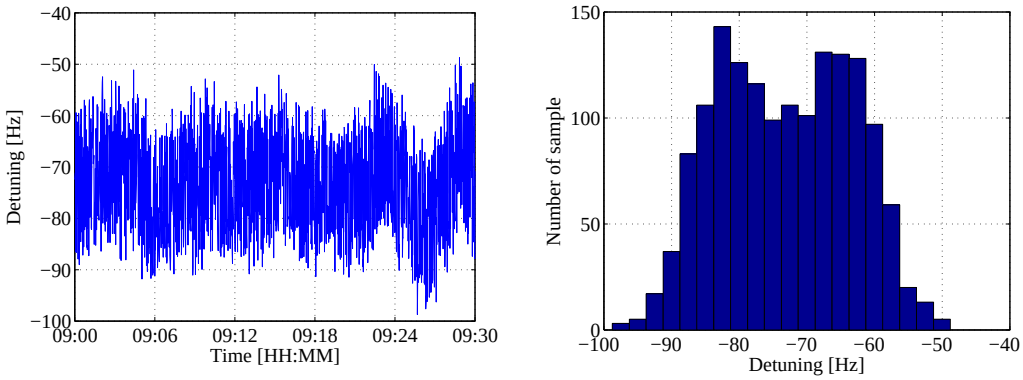
The motivation for the microphonics evaluation is the need to understand the microphonics behavior of each cavity, which is important for constructing a control algorithm to compensate for the microphonics.

To define the cavity wall thickness, several parameters are considered in the cavity design. To make the cavity more rigid, the wall should be as thick as possible. To increase the cooling effectiveness, the wall of the superconducting cavity is made as thin as possible. Furthermore, the superconducting cavity is made of niobium, which is expensive. The TESLA-like cavity for the ILC is constructed of a 2.8 mm Nb sheet [1]. This thickness makes the cavity more susceptible to mechanical disturbances such as external mechanical excitations (microphonics) or Lorentz force detuning. The microphonics has been estimated by measuring the fluctuation of the cavity detuning, which was measured after the RF power was turned off. Because there is no RF signal, Equation 2.74 becomes

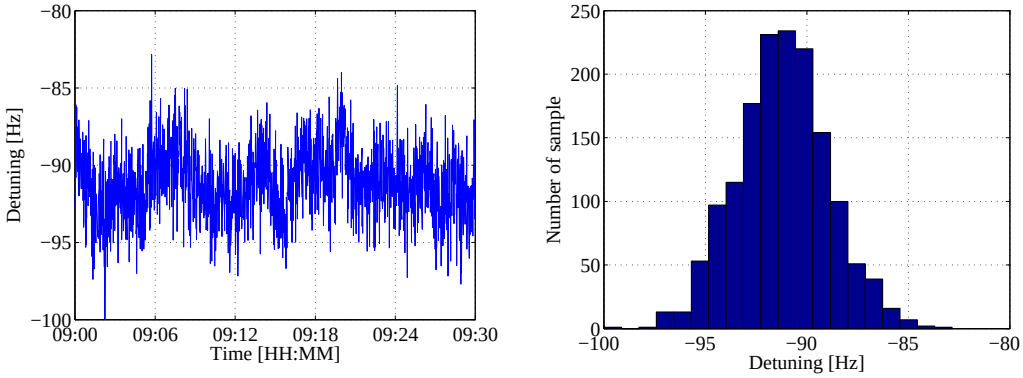
$$\Delta\omega = \frac{\mathrm{d}\theta}{\mathrm{d}t} \tag{6.1}$$

Figure 6.2 shows an example of the phase waveform. In this case, the RF was turned off at 1600 µs.

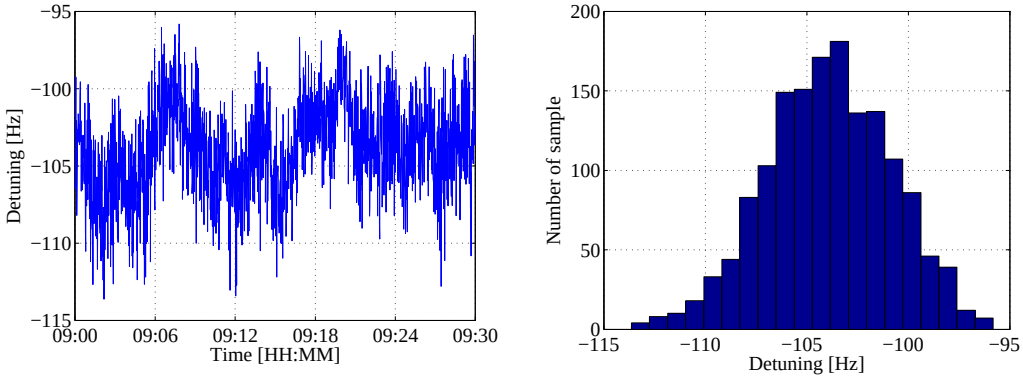
The cavity field phase decay after the RF power is turned off is then fitted. Thirty points are fitted from approximately 1605 µs to 1635 µs. The microphonics of eight cavities were measured for approximately 30 min. The results are shown in Figures 6.3, 6.4, and 6.5. The measured microphonics levels in the cavities are summarized in Tables 6.1 and 6.2. Most of the measurements give a near-Gaussian distribution with RMS values in the range of 2.3–9.9 Hz.



(a) Cavity #1 detuning ($\sigma_{\Delta f} = 9.9\,\mathrm{Hz}$)

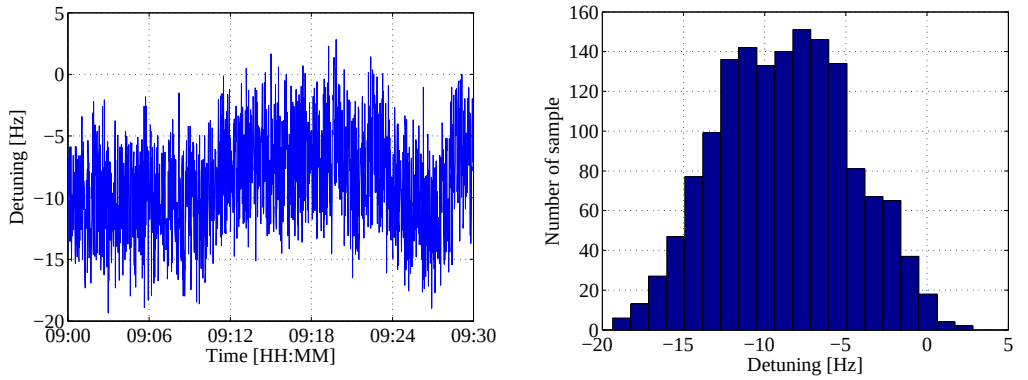


(b) Cavity #2 detuning ($\sigma_{\Delta f} = 2.3\,\mathrm{Hz}$)

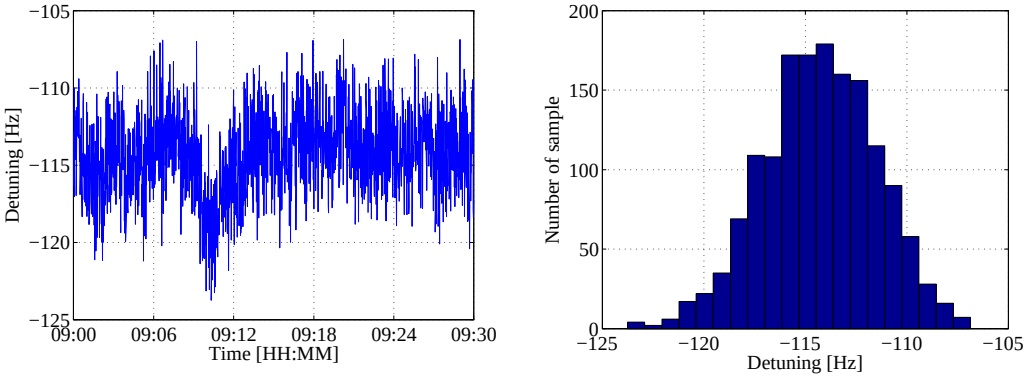


(c) Cavity #3 detuning ($\sigma_{\Delta f} = 3.3\,\mathrm{Hz}$)

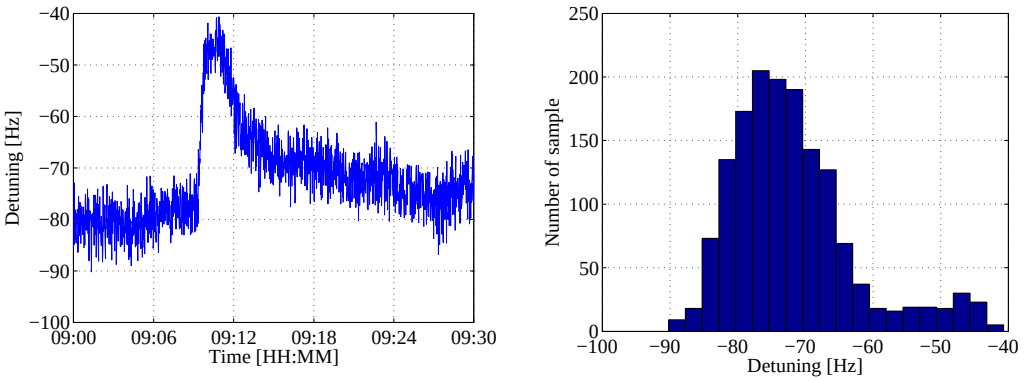
Figure 6.3: Microphonics and histograms of cavities #1, #2, and #3. Data were taken for 30 min, as indicated on the time axis of the detuning plot.



(a) Cavity #4 detuning ($\sigma_{\Delta f} = 4.3\,\mathrm{Hz}$)

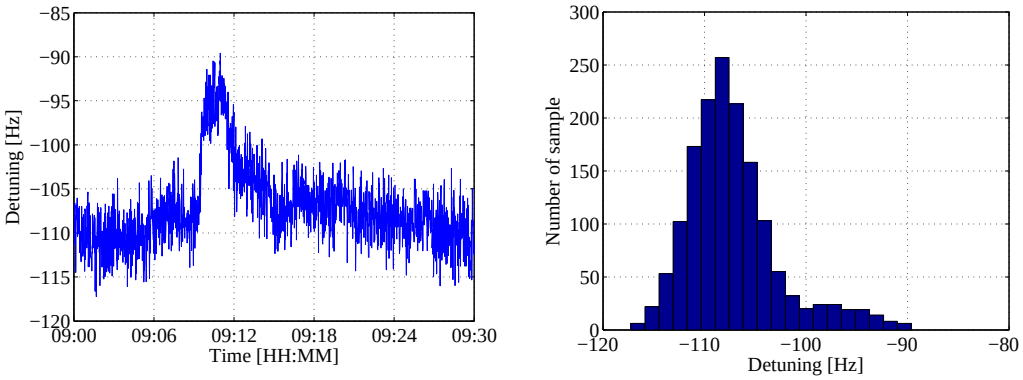


(b) Cavity #8 detuning ($\sigma_{\Delta f} = 2.9\,\mathrm{Hz}$)

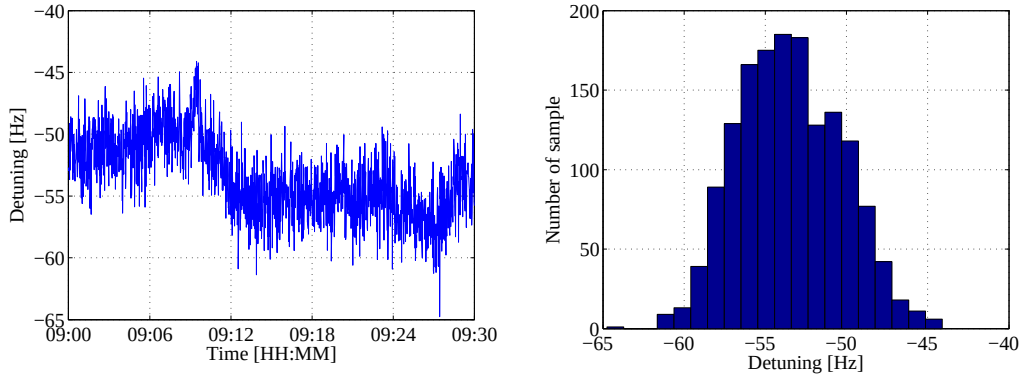


(c) Cavity #10 detuning ($\sigma_{\Delta f} = 5.8\,\mathrm{Hz}$)

Figure 6.4: Microphonics and histograms of cavities #4, #8, and #10. Data were taken for 30 min, as indicated on the time axis of the detuning plot.



(a) Cavity #11 Detuning ($\sigma_{\Delta f} = 3.4\,\mathrm{Hz}$)



(b) Cavity #12 Detuning ($\sigma_{\Delta f} = 2.5\,\mathrm{Hz}$)

Figure 6.5: Microphonics and histograms of cavities #11 and #12. Data were taken for 30 min, as indicated on the time axis of the detuning plot.

Table 6.1: RMS error of the microphonic noise level of the four cavities (#1, #2, #3, #4)

$\sigma_{\Delta f}$(RMS)			
Cavity 1	Cavity 2	Cavity 3	Cavity 4
9.9 Hz	2.3 Hz	3.3 Hz	4.3 Hz

Table 6.2: RMS error of the microphonic noise level of the four cavities (#8, #10, #11, #12)

$\sigma_{\Delta f}$(RMS)			
Cavity 8	Cavity 10	Cavity 11	Cavity 12
2.9 Hz	5.8 Hz	3.4 Hz	2.5 Hz

A long-duration measurement was conducted for 16 h from 00:00 to 16:00. The results are shown in Figures 6.6 and 6.7. Gaps in the graph indicate that the klystron was turned off.

The results show that the highest fluctuation appears in cavity #1 (Figure 6.6(a)). One possible reason is that cavity #1 is close to the cold box (Figure 1.4). The second-highest fluctuation appears in cavity #12. One possible reason is that this cavity is at the end of the cavity string. Consequently, this cavity is less mechanically stable than the other cavities, and thus more susceptible to microphonics.

Fluctuation of the detuning may be caused by factors such as helium pressure variation or mechanical vibration due to the accelerator environment. The highest fluctuation appeared in cavity #1. The lowest fluctuation appeared in cavity #2.

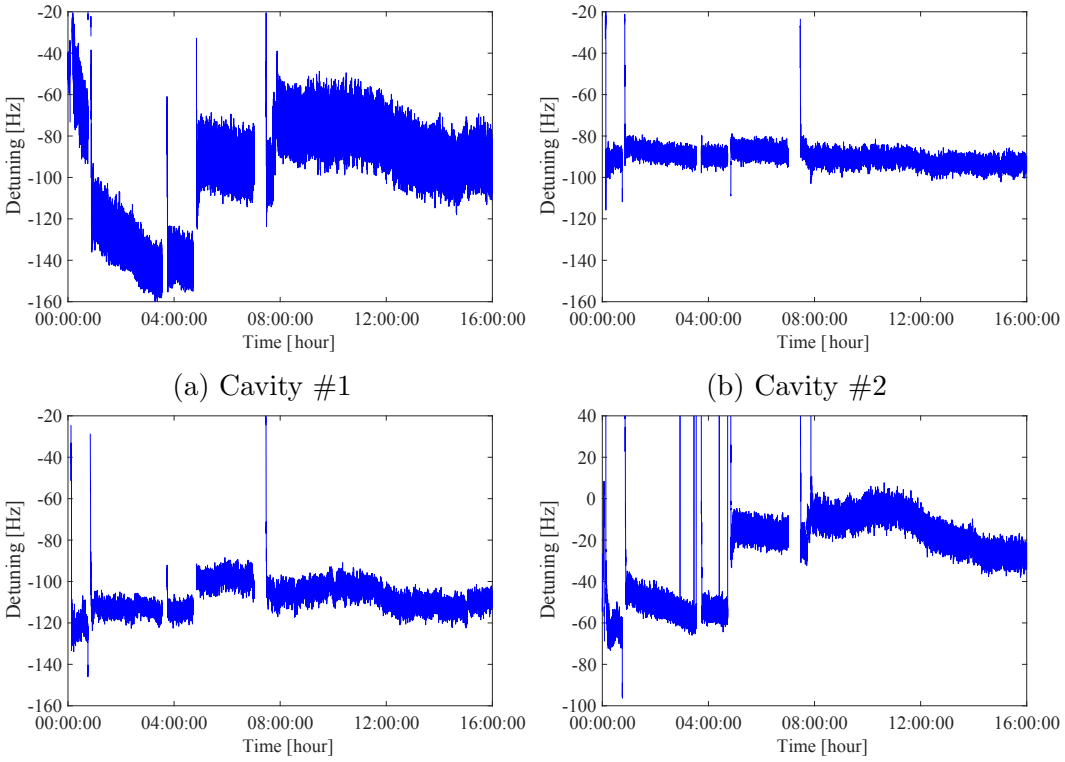
The liquid helium pressure measurement was conducted to understand the relation with microphonics. A trend of the liquid helium pressure is shown in Figure 6.8. The average pressure during the 16 hour operation is 2.999 kPa. The result shows that there is no fluctuation in helium pressure. However, based on the result, the relation between helium pressure and detuning fluctuation is still not clear. As the comparison, the other result from DESY shows that the fluctuation of liquid helium pressure can be observed and the stability requirement is 2 % peak [39].

6.3 Filling on Resonance Method

The filling on resonance method is based on the idea of keeping the cavity always in resonance with the forward signal [40]. It is difficult, if not impossible, to change the frequency of the forward signal to follow the cavity resonance from time to time. Because changes in the frequency over time can be translated to changes in the phase over time, an easier way to maintain the resonance condition during the filling time is to modulate the feed-forward table with the phase according to the cavity detuning.

For simplicity, the detuning pattern during the filling time is approximated. In this case, detuning starts at 500 Hz and decreases linearly to zero at the beginning of the flattop, as illustrated in Figure 6.9(a).

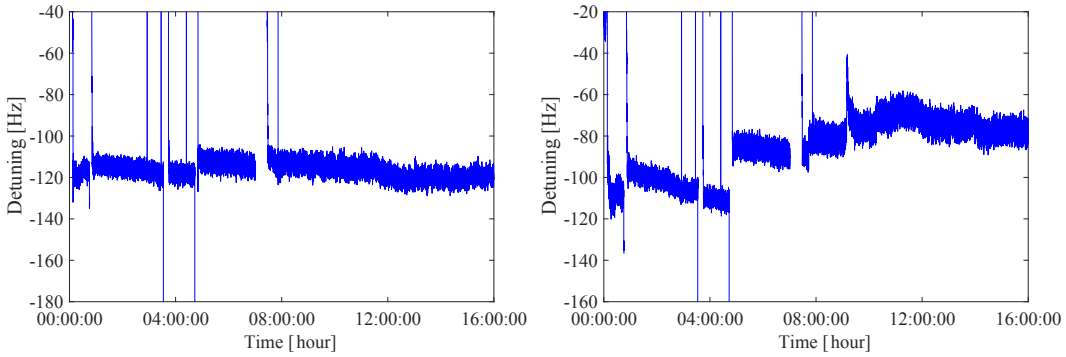
For simplicity, the detuning pattern during the filling time is then approximated. In this case, the detuning is started with 500 Hz and linearly decreases to zero at the beginning of the flattop as illustrated in Figure 6.9(a). The



(a) Cavity #1 (b) Cavity #2

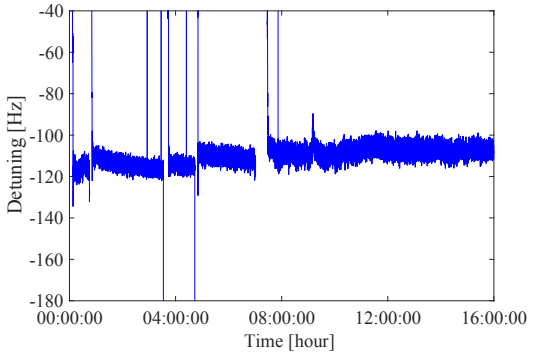
(c) Cavity #3 (d) Cavity #4

Figure 6.6: Detuning of cavities #1, #2, #3, and #4 at the end of the RF pulse. Data were taken for 16 h, as indicated on the time axis of the detuning plot.

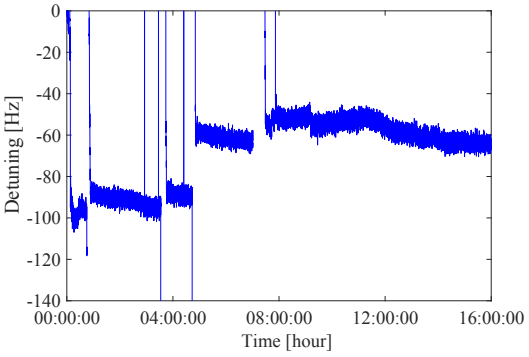


(a) Cavity #8

(b) Cavity #10



(c) Cavity #11



(d) Cavity #12

Figure 6.7: Detuning of cavities #8, #10, #11, and #12 at the end of the RF pulse. Data were taken for 16 h, as indicated on the time axis of the detuning plot.

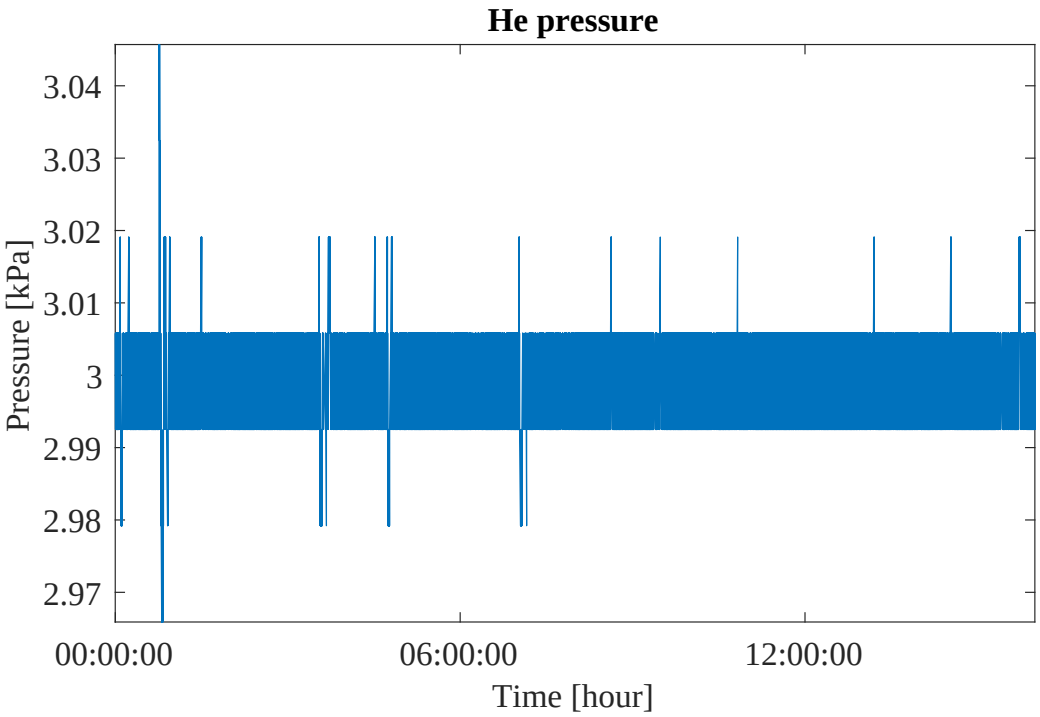
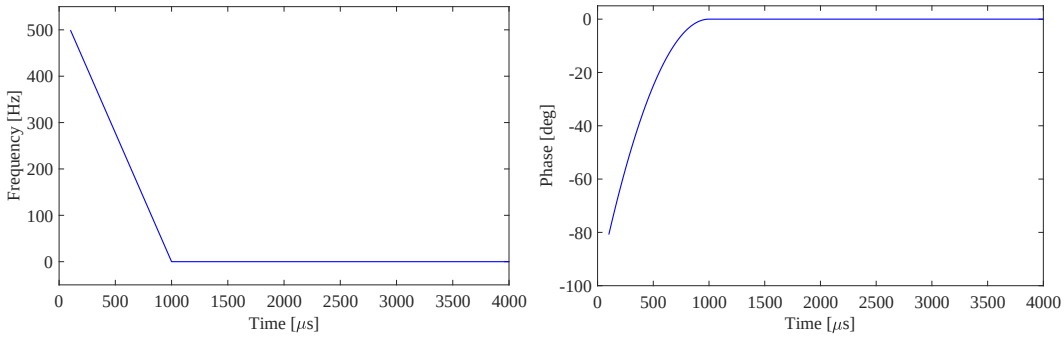


Figure 6.8: Helium pressure during 16 hours operation.



(a) Approximated detuning. (b) The phase pattern.

Figure 6.9: The upper figure is the detuning pattern approximated from a simple linear fitting. Right figure is the phase pattern calculated from approximated detuning using equation 6.2.

approximated detuning pattern is then converted to a phase pattern as follows.

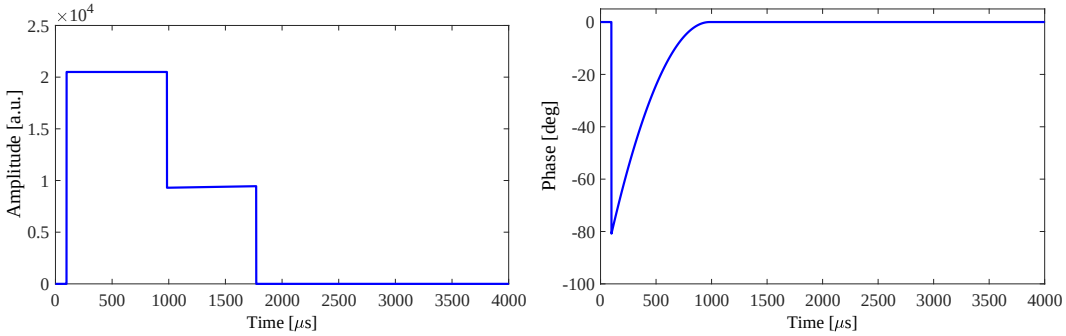
$$\phi(t) = \int_0^t 2\pi\Delta f(\tau)d\tau \tag{6.2}$$

where ϕ is the phase, and Δf is the detuning in Hertz. The converted phase detuning is illustrated in Figure 6.9(b). The phase pattern is then used to modulate the feed-forward table.

Before being modulated by the phase in Figure 6.9(b), the feed-forward phase was set to zero for the entire RF pulse. The feed-forward amplitude and phase after modulation are shown in Figure 6.10(a) and 6.10(b), respectively. The rate of change of the feed-forward phase during the filling time follows the phase of the approximated detuning. In the implementation, the calculation using Equation 6.2 was performed off-line, and the modulated feed-forward table was placed in the FPGA.

6.4 Digital LLRF System Setup

Two digital LLRF boards were used in this experiment. The first board was used to implement the control system. This is the same board as that used in the experiment in Chapter 3. The second board was used for signal monitoring to measure the cavity field, forward, and reflected signals. The monitor board features a Virtex II Pro 30 FPGA [41], 10 16-bit ADCs (LT2208, Linear Technology, Inc. [33]), and 2 14-bit DACs (AD9764, Analog Device, Inc. [42]) [18]. Two boards were used to monitor signals from eight cavities.



(a) Amplitude (b) Phase

Figure 6.10: Figure (c) and (d) are the feedforward amplitude and phase table after being phase modulated. Only the phase is affected.

Figures 6.11 and 6.12 show a photograph and block diagram of the board, respectively.

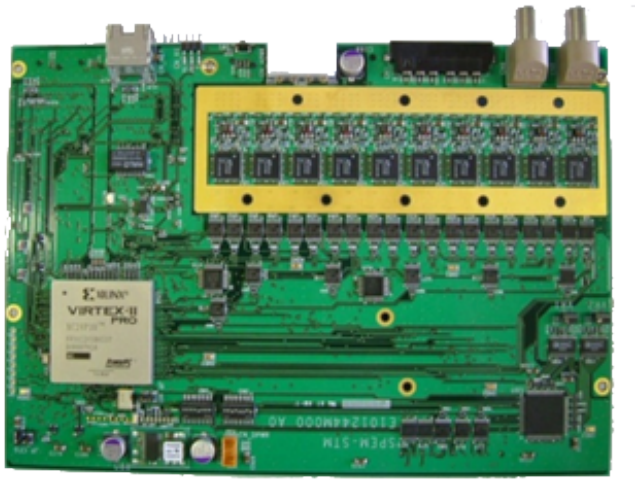


Figure 6.11: cPCI-compliant digital LLRF board.

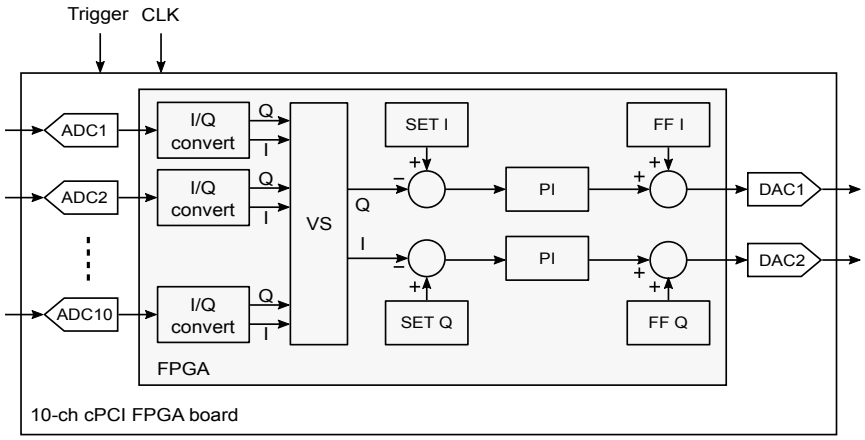


Figure 6.12: Block diagram of cPCI hardware. The board is equipped with 10 ADCs and 2 DACs.

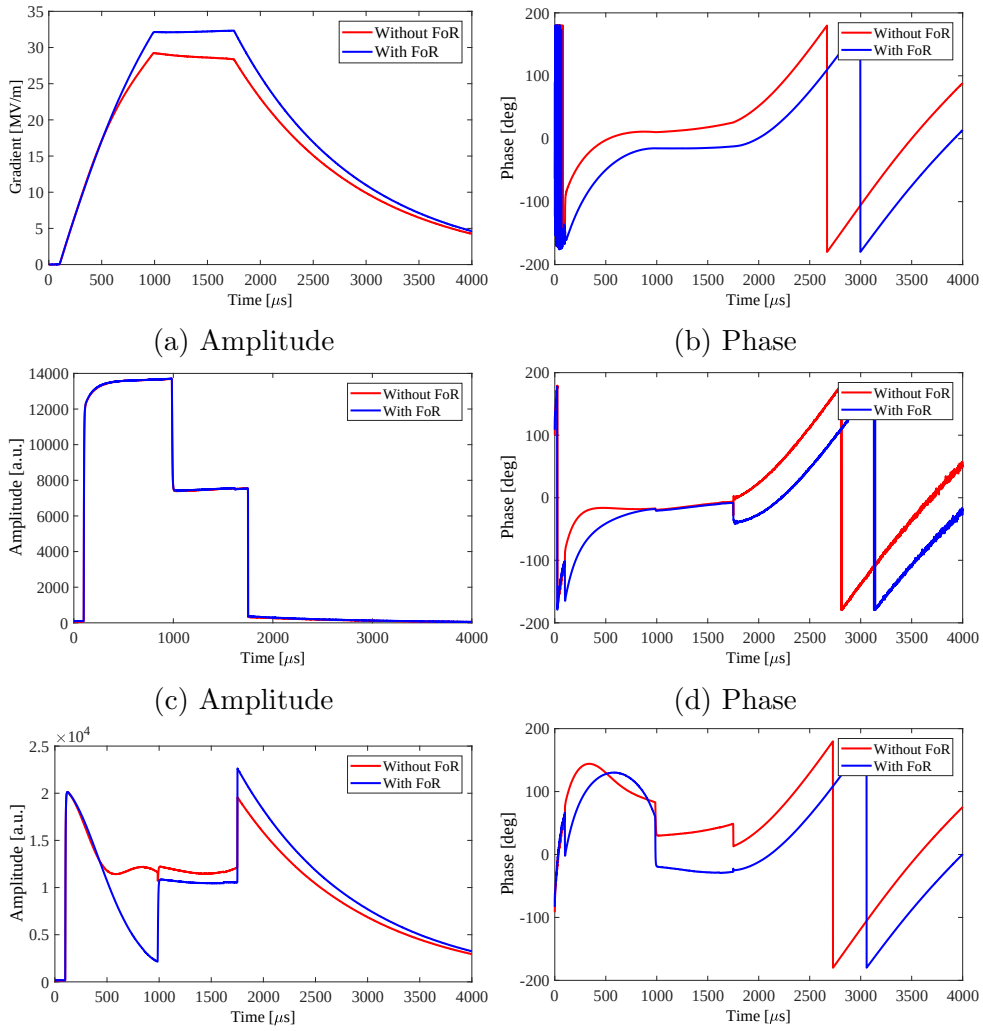
6.5 Feed-Forward Operation

The motivation for the measurement is to understand the effectiveness of filling on resonance implementation for reducing the klystron power in eight-cavity operation with feed-forward control.

In this measurement, only feed-forward control was used, and there was no beam. Detuning compensation began at 500 Hz when the filling time started and decreased to 0 Hz at the leading edge of the flattop. The effect of filling on resonance implementation is shown in Figure 6.13, which shows the forward, cavity pickup, and reflected waveforms with and without the filling on resonance method for cavity #1. Figure 6.13(a) and 6.13(c) show that a higher cavity gradient can be achieved by applying the same forward power. Figure 6.13(e) and 6.13(f) show the reflected amplitude and phase of cavity #1 with and without the filling on resonance method, respectively. When the method is applied, the reflected amplitude during the filling time decreases.

Figure 6.13(c) shows that the edge of the forward amplitude waveform is curved when the RF is on. This curve is caused by the curved edge of the high voltage applied by the klystron, which directly affects the klystron output. The waveform of the klystron applied voltage, klystron current, and klystron RF output are shown in Figure 6.14. The repetition rate is 5 Hz, and the pulse width is 1650 µs.

In the measurement, a klystron modulator with a direct-switched-type design was used. The modulator consists of four switching power supplies, a storage capacitor bank, a series of IGBT switches, a bouncer circuit, and a pulse transformer [43]. A simplified schematic of the modulator is shown in



(a) Amplitude (b) Phase

(c) Amplitude (d) Phase

(e) Amplitude (f) Phase

Figure 6.13: Forward, cavity pickup, and reflected waveforms without and with filling on resonance method.

Figure 6.15. The curve on the edge of the high voltage applied by the klystron is caused by the limited bandwidth of the pulse transformer. Therefore, some high-frequency components in the pulse cannot pass the pulse transformer, resulting in the curved edge on the pulse transformer output.

The waveforms of the cavity field amplitude of all eight cavities are shown in Figure 6.16. The average gradient of the flattop (1100–1700 µs) was calculated. The result shows that the gradients of all the cavities with filling on resonance were higher than those without filling on resonance. The gradient increment varies by approximately 2–12 %, as listed in Table 6.3. The highest gradient

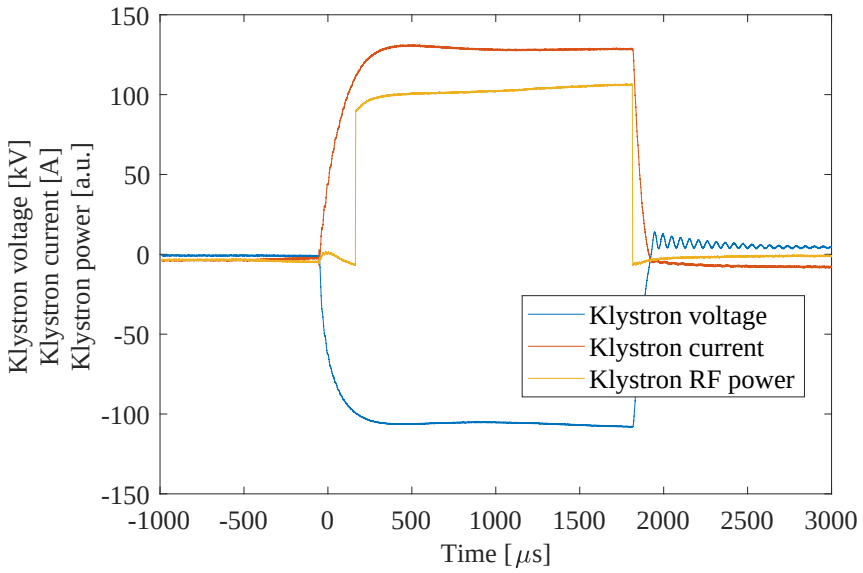


Figure 6.14: Klystron applied high voltage, current, and RF power.

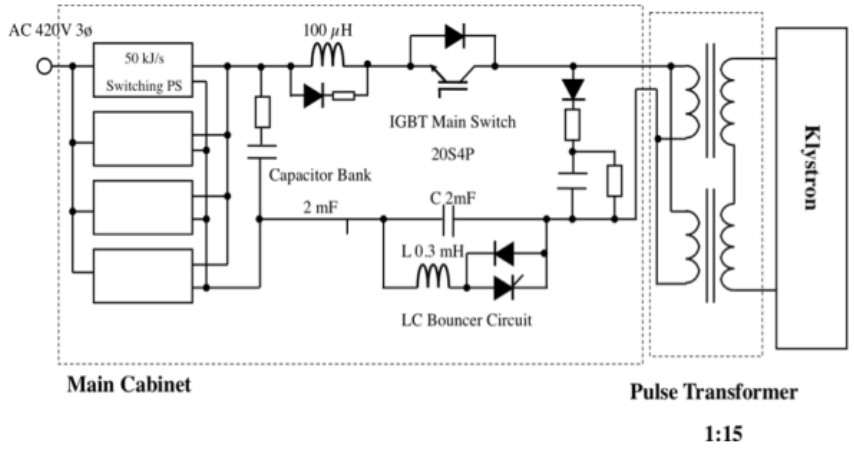
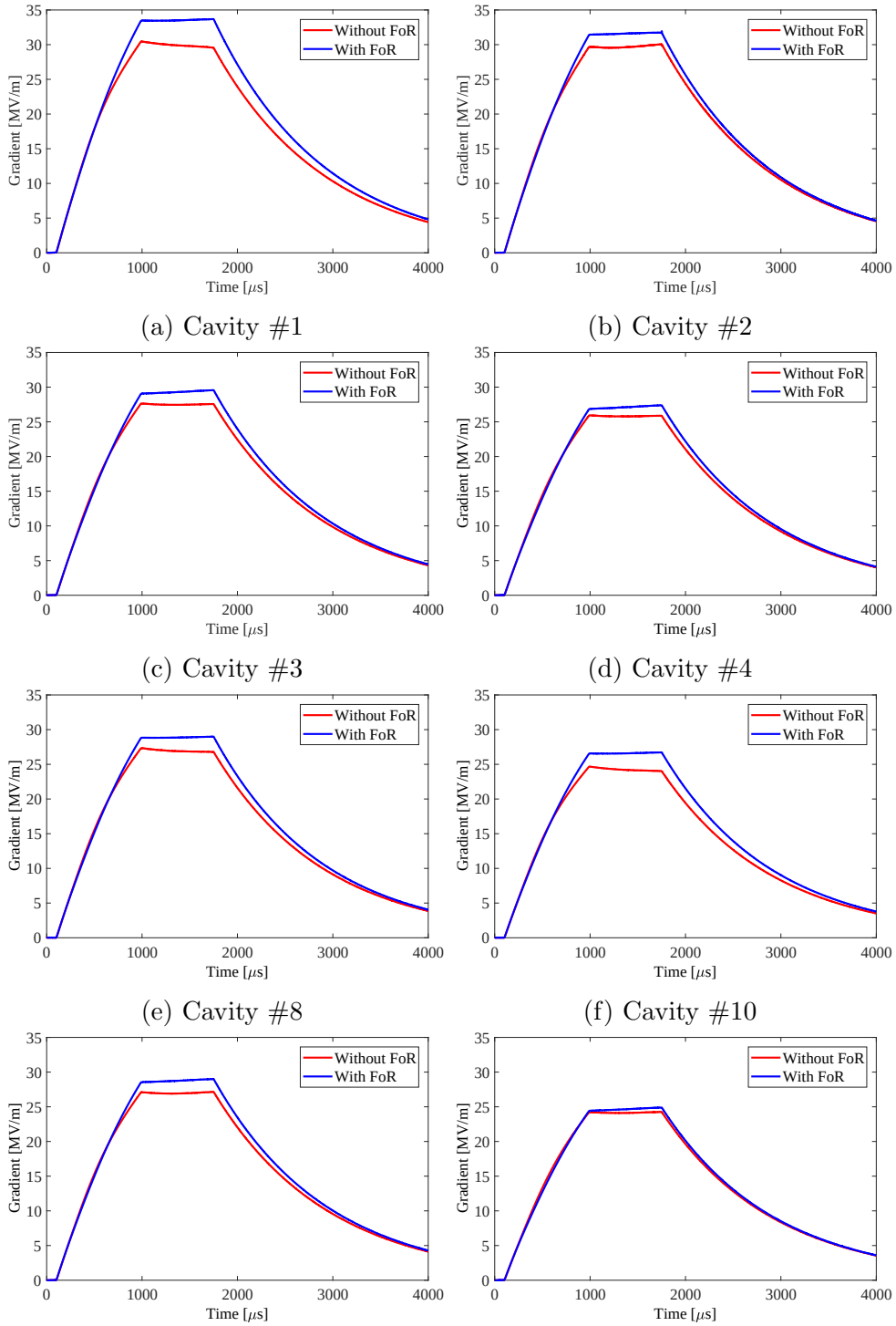


Figure 6.15: Simplified schematic of STF modulator. [43]

improvement is in cavity #1, and the lowest gradient improvement is in cavity #12. The improvement in the vector sum is approximately 7.1 %, indicating that a power savings of approximately 14 % is possible.

Figure 6.17 compares the detuning patterns of all the cavities without and with filling on resonance. The results indicate that the filling on resonance



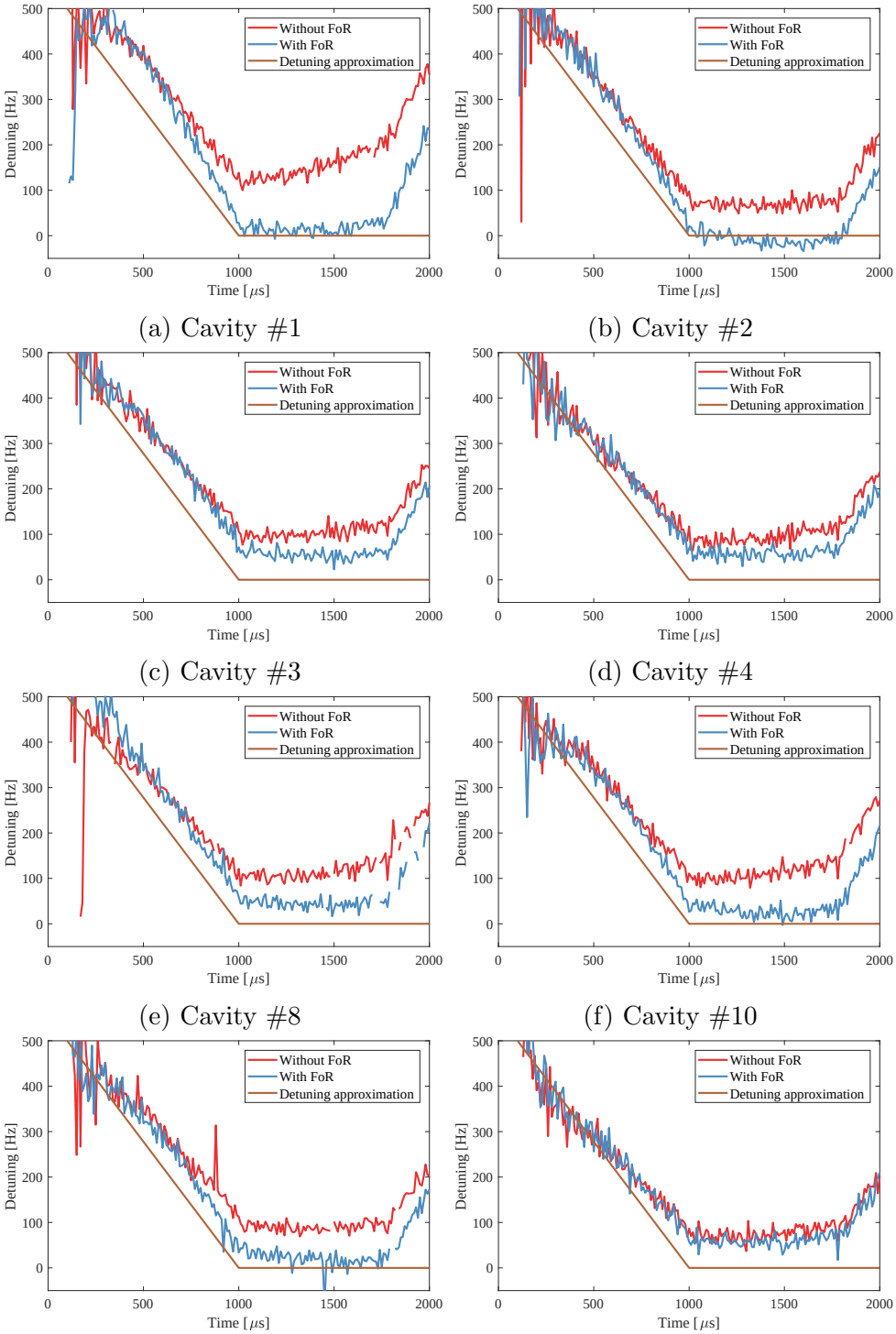
(a) Cavity #1 (b) Cavity #2

(c) Cavity #3 (d) Cavity #4

(e) Cavity #8 (f) Cavity #10

(g) Cavity #11 (h) Cavity #12

Figure 6.16: Cavity gradients of all eight cavities without and with filling on resonance method.



(a) Cavity #1 (b) Cavity #2

(c) Cavity #3 (d) Cavity #4

(e) Cavity #8 (f) Cavity #10

(g) Cavity #11 (h) Cavity #12

Figure 6.17: Detuning patterns of all cavities without and with filling on resonance (FoR).

Table 6.3: Average flattop (1100–1700 µs) of cavity gradient without (w/o FoR) and with (w/FoR) filling on resonance.

Cavity	**w/o FoR** [**MV/m**]	**w/ FoR** [**MV/m**]	**Increment** [%]
Cav #1	29.9	33.5	12.0
Cav #2	29.7	31.6	6.4
Cav #3	27.5	29.9	6.6
Cav #4	25.8	27.1	5.0
Cav #8	26.9	28.9	7.2
Cav #10	24.2	26.6	9.8
Cav #11	27.0	28.8	6.7
Cav #12	24.1	24.7	2.0
Vector Sum	26.7	28.6	7.1

method can effectively increase the cavity gradient.

The detuning patterns during the filling stage of all eight cavities are shown in Figure 6.18. The detuning cavities were fitted with a polynomial. Cavity #1 shows the largest gradient improvement after filling on resonance is implemented because the detuning pattern of this cavity is farthest from the approximated detuning pattern for phase modulation in the feed-forward table. Figure 6.18 shows that the detuning pattern of cavity #12 is the closest to that of cavity #1, so the improvement caused by filling on resonance is the smallest.

The variation in the increment can be understood because the detuning pattern varies from cavity to cavity, but all the cavities were driven by the same driving signal pattern. Therefore, the effectiveness of the filling on resonance method differs from cavity to cavity. It is not possible to obtain the same effectiveness for each cavity. However, the average power reduction of 14 % is suitable for the ILC.

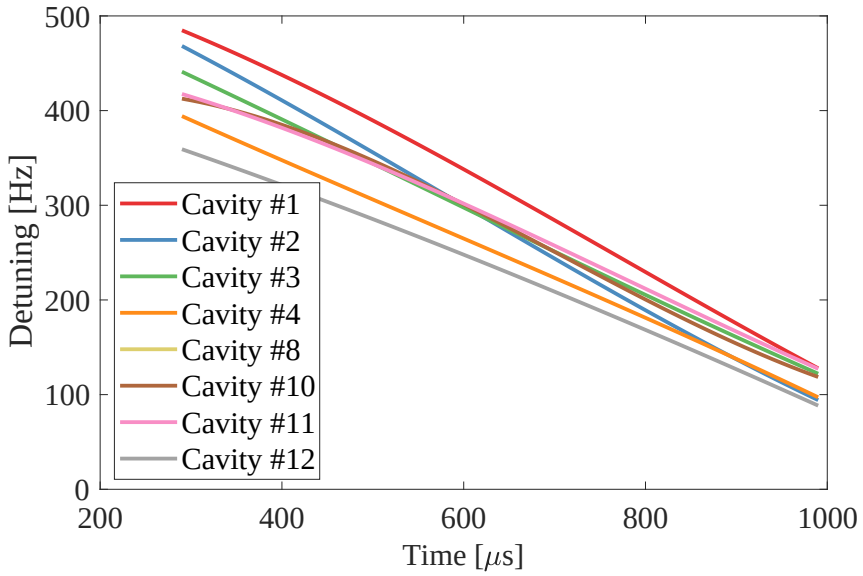


Figure 6.18: Detuning patterns of eight cavities after they were fitted with third-order polynomial fitting during the filling time.

6.6 Feedback Operation

The motivation for the measurement is to understand the behavior of the filling on resonance method during operation in feedback control. This measurement was also conducted with feed-forward control.

The loop delay of the LLRF digital control system causes the overshoot at the beginning of the cavity driving signal if the feedback gain is too high. To minimize this effect, the feedback gain can be started at zero and increased gradually to the desired value at the start time of the beam flattop. This technique is known as gain scheduling.

Two conditions are compared to understand the effect of filling on resonance when it is applied with feedback and also to understand the feedback gain scheduling effect. Figure 6.19 shows the ordinary gain pattern (red-dashed line) and gain scheduling pattern (blue solid line). In the ordinary gain pattern, the gain is equally distributed from the beginning of RF-on to RF-off. In the gain scheduling pattern, the gain is started at zero at 800 µs and increases linearly to the desired gain at the starting point of the flattop. These two gain patterns were applied and evaluated. Feed-forward control was also implemented in this experiment.

Figure 6.20 compares the forward, reflected, and cavity pickup waveforms with and without filling on resonance. The blue lines show the results obtained

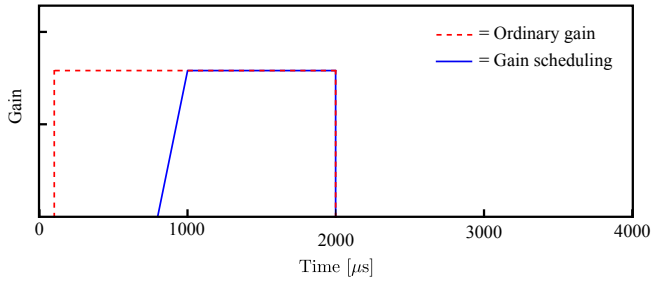


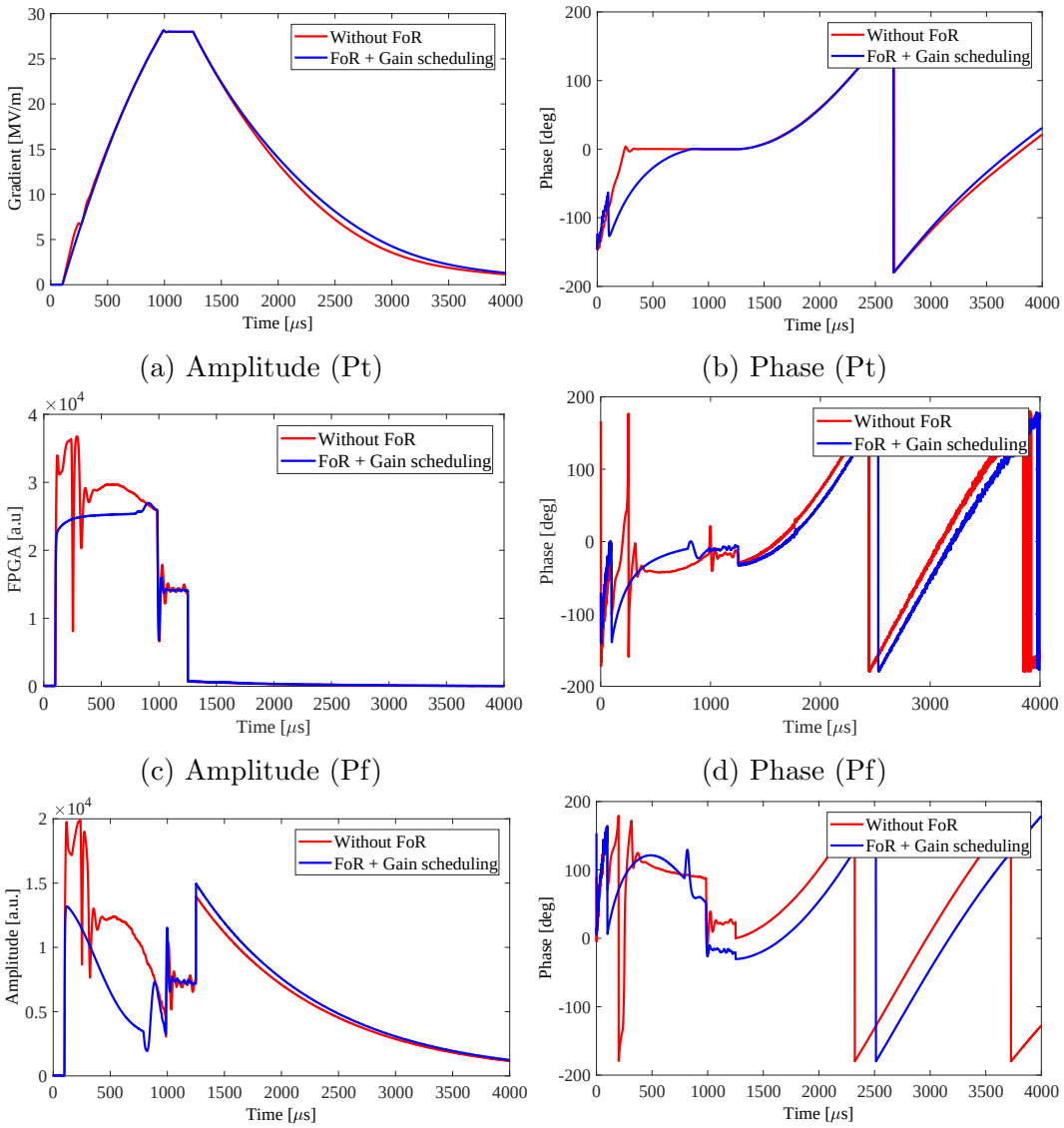
Figure 6.19: Feedback gain pattern

without filling on resonance and with the ordinary feedback gain pattern (red-dashed line in Figure 6.19). The red lines show the results obtained with filling on resonance and the feedback gain scheduling pattern (solid blue line in Figure 6.19).

From Figure 6.20(c) and 6.20(d), we see that the required klystron power during the filling time to obtain the same cavity gradient is smaller with the filling on resonance method than without it. Gain scheduling reduces the oscillation. From Figure 6.20(e) and 6.20(f), we can see that the reflected signal with filling on resonance has a lower power than that without filling on resonance. These results indicate that the filling on resonance method can reduce the required power during the filling time to obtained the designed cavity gradient.

The following conclusions were reached after the filling on resonance method was implemented.

- For the same forward power, a higher cavity field can be achieved with filling on resonance than without it.
- The effectiveness of the filling on resonance method differs from cavity to cavity because the detuning of each cavity is different.
- The measurements confirms that by adopting the filling on resonance method, the klystron power required to achieve a given cavity gradient can be reduced.
- If feedback is applied in the filling on resonance method, the feedback gain should start at a small value and increase to the desired value at the leading edge of the flattop, a process known as gain scheduling.
- To apply feedback in the filling on resonance method, the reference phase table should also be modified according to the detuning. If the phase of



(a) Amplitude (Pt)

(b) Phase (Pt)

(c) Amplitude (Pf)

(d) Phase (Pf)

(e) Amplitude (Pb)

(f) Phase (Pb)

Figure 6.20: Amplitude and phase with gain scheduling

the reference is not rotated, the control system will try to achieve zero phase (it is assumed that zero phase is set for the entire pulse duration) by increasing the klystron output power.

6.7 Summary

A proof of concept for the filling on resonance method was demonstrated. In this method, the feed-forward table is phase-modulated using the translation of the approximated cavity detuning. In feed-forward operation, the klystron power can be reduced by 14 %. The filling on resonance method is also effective in feedback operation. To reduce the overshoot when the RF power is on, feedback gain scheduling can be implemented. Furthermore, the microphonics of each cavity were measured.

Chapter 7

Conclusion and Future Work

Digital LLRF control systems using several techniques were set up and evaluated at STF-KEK to meet the ILC amplitude and phase stability requirements, which are 0.07 % (RMS) and 0.35° (RMS), respectively. The work can be summarized as follows.

- The small scale of the digital LLRF control system for the ILC with a master–slave configuration was demonstrated. Eight cavities with vector sum control were constructed. The amplitude and phase stabilities are 0.006 % (RMS) and 0.027° (RMS), respectively, which fulfill the ILC stability requirements. Without a beam, the delay introduced by the optical communication link does not affect the RF stability.

- A proof of concept of the IF-mixture technique was demonstrated and evaluated. Four different IFs can be combined to reduce the required number of ADCs. Amplitude and phase stabilities of 0.006 % (RMS) and 0.046° (RMS), respectively, can be achieved. These values meet the ILC stability requirements.

- A direct sampling technique for system monitoring was demonstrated and evaluated. Amplitude and phase stabilities of 0.021 % (RMS) and 0.17° (RMS), respectively, can be achieved. However, there was a tilt in the phase that may be caused by the difference in clock distribution between the feedback and monitoring systems. The first successful implementation of monitoring of the MO and LO using sampling at a single frequency by the direct sampling technique was also demonstrated.

- The filling on resonance method was demonstrated and evaluated. It was confirmed that by applying this technique, the required klystron power during the filling time can be reduced.

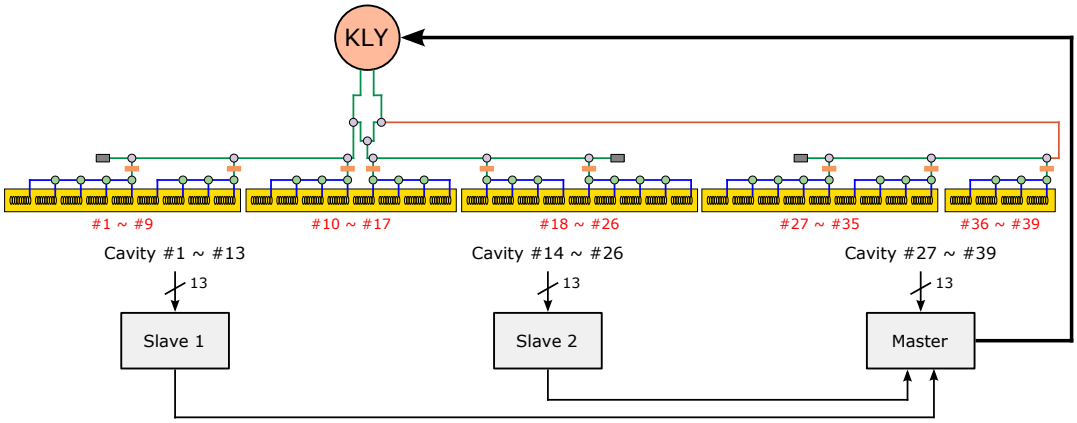


Figure 7.1: Possible configuration of digital LLRF with master–slave configuration for the ILC. Using three boards, 39 signals can be accommodated. However, in this configuration, only cavity field signals can be measured

In future work, the digital LLRF control system with a master–slave configuration and IF-mixture implementation can be used to realize one RF station. The possible configurations are discussed below.

The digital LLRF control system configuration based on the ILC TDR is shown in Figure 2.18. In this configuration, only cavity field signals are considered. A possible configuration for one RF station using an MTCA.4 board is shown in Figure 7.1. Two slave boards and one master board are required.

To ensure stable operation, parameters such as the detuning must be monitored. To estimate the cavity detuning, the forward and reflected signals must also be measured. Consequently, a total of approximately 120 signals must be measured. One MTCA.4 board is equipped with 14 ADCs.

To calculate the cavity detuning, the cavity field, forward, and reflected signals must be retrieved for the same event. To ensure that this occurs, these three signals should be fed to the same board for each cavity. Consequently, one board can accommodate up to four cavities (12 signals). A total of 10 slave boards and 1 master board are required to accommodate one RF station. The configuration for one RF station is depicted in Figure 7.2.

One concern regarding this implementation is the availability of FPGA resources. As explained in Chapter 4, the IF-mixture technique was applied on a digital board with four ADCs. It was implemented in the Virtex 5 XC5VFX70T Xilinx FPGA. The available logic resource in this FPGA is 11.200 slices. One slice in this FPGA consists of four LUTs and four flip-flops [32]. A total of approximately 10,000 FPGA slices was required to implement the technique.

To implement the IF-mixture technique with more ADCs, additional I/Q

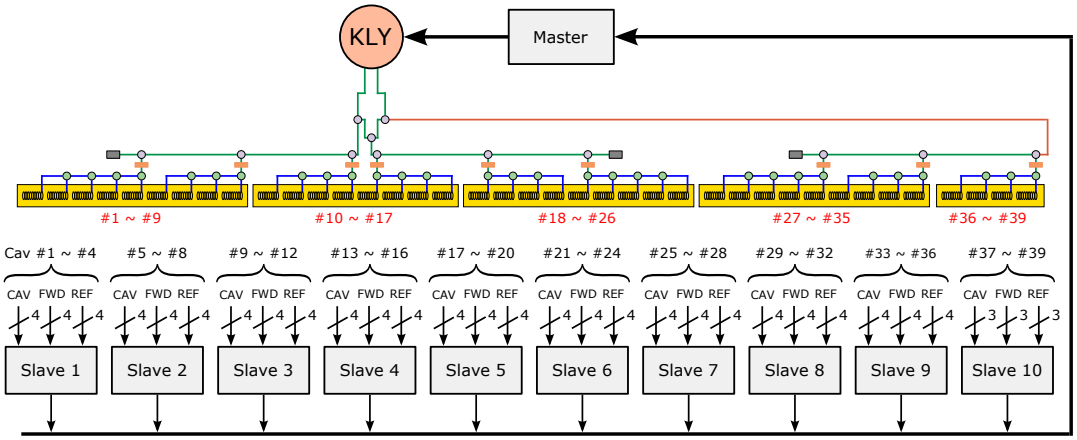


Figure 7.2: Possible configuration of digital LLRF with master–slave configuration for the ILC. Nine slave boards are required to accommodate 117 signals. CAV = cavity field; FWD = forward signal; REF = reflected signal.

calculation modules are necessary. One module requires approximately 100 slices. As shown in Figure, for this board the I/Q calculation is performed in a Spartan 6 XC6SLX150T Xilinx FPGA. The available resource in this FPGA is 23.038 slices. One slice in this FPGA consists of four LUTs and eight flip-flops [44]. This board is equipped with 14 ADCs. Thus, an additional 40 I/Q calculation modules are required. Approximately 4000 additional FPGA slices are necessary. Thus, multi-IF technique implementation on this board is expected to be possible.

To construct one RF station, one master board and two slave boards are required. A total of 168 channel inputs are available. The possible digital LLRF control system for the ILC for one RF station using a master–slave configuration and multi-IF technique is illustrated in Figure 7.3.

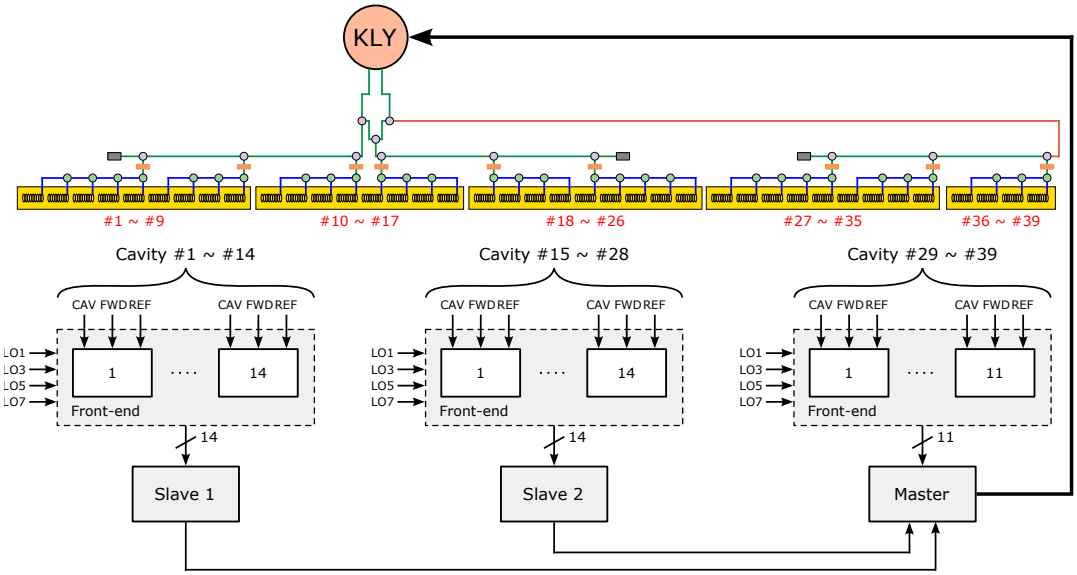


Figure 7.3: Possible digital LLRF control system for the ILC using master–slave configuration and four IFs. The front-end block is illustrated in detail in Figure 4.1. CAV = cavity field; FWD = forward signal; REF = reflected signal.

The placement of the boards must also be considered. There are two possibilities for placing the boards. The first is near the cryomodule to obtain the shortest signal transmission delay, although there is a risk of faster board deterioration caused by high radiation. This risk can be mitigated by covering the board with appropriate shielding. The second possibility is to place the board in the nonradiation area, although there is a risk of a longer signal transmission delay. These two methods need to be further studied to obtain the best trade-off.

Appendix A
Power at Filling Time

The klystron power at the filling time is derived as follows.

$$\vec{V_{\text{cav}}}(t) = \frac{\omega_{1/2} R_{\text{L}} \vec{I}(t)}{\omega_{1/2} - j\Delta\omega}(1 - e^{-(\omega_{1/2} - j\Delta\omega)t}) \tag{A.1}$$

Both sides are then squared to obtain

$$V_{\text{cav}}^2 = \frac{\omega_{1/2}^2 R_{\text{L}}^2 I^2}{(\omega_{1/2} - j\Delta\omega)(\omega_{1/2} + j\Delta\omega)}(1 - e^{-(\omega_{1/2} - j\Delta\omega)t})(1 - e^{-(\omega_{1/2} + j\Delta\omega)t}) \tag{A.2}$$

$$|\vec{I_{\text{g}}}| = 2\sqrt{\frac{2P_{\text{f}}}{R_{\text{L}}}},\ \omega_{1/2} = \frac{\omega_0}{2Q_{\text{L}}},\ R_{\text{L}} = \frac{1}{2}\left(\frac{r}{Q}\right) Q_{\text{L}} \tag{A.3}$$

$$\begin{aligned} P_{\text{f}} &= \frac{1}{8} R_{\text{L}} I_{\text{g}}^2 \\ &= \frac{1}{8} R_{\text{L}} \frac{V_{\text{cav}}^2(\omega_{1/2}^2 + \Delta\omega^2)}{\omega_{1/2}^2 R_{\text{L}}^2 (1 + e^{-2\omega_{1/2}t} - 2e^{-\omega_{1/2}t}\cos(\Delta\omega t))} \\ &= \frac{1}{8} \frac{V_{\text{cav}}^2(\frac{\omega_0^2}{4Q_{\text{L}}^2} + \Delta\omega^2)}{\frac{\omega_0^2}{4Q_L^2}\frac{1}{2}\left(\frac{r}{Q}\right) Q_{\text{L}} \left(1 + e^{-\frac{\omega_0}{Q_{\text{L}}}t} - 2e^{-\frac{\omega_0}{2Q_{\text{L}}}t}\cos(\Delta\omega t)\right)} \\ &= \frac{V_{\text{cav}}^2(\omega_0^2 + 4Q_{\text{L}}^2\Delta\omega^2)}{4\left(\frac{r}{Q}\right) Q_{\text{L}}\omega_0^2 \cdot \left[1 + e^{-\frac{\omega_0 t}{Q_{\text{L}}}} - 2e^{-\frac{\omega_0 t}{2Q_{\text{L}}}}\cos(\Delta\omega t)\right]} \end{aligned} \tag{A.4}$$

The power at the filling time is

$$P_{\text{fill}} = \frac{V_{\text{cav}}^2(\omega_0^2 + 4Q_{\text{L}}^2\Delta\omega^2)}{4\left(\frac{r}{Q}\right) Q_{\text{L}}\omega_0^2 \cdot \left[1 + e^{-\frac{\omega_0 T_{\text{fill}}}{Q_{\text{L}}}} - 2e^{-\frac{\omega_0 T_{\text{fill}}}{2Q_{\text{L}}}}\cos(\Delta\omega T_{\text{fill}})\right]} \tag{A.5}$$

With no detuning ($\Delta\omega = 0$), the power is

$$P_{\text{fill}} = \frac{V_{\text{cav}}^2}{4\left(\frac{r}{Q}\right) Q_L \left[1 - e^{-\frac{T_{\text{fill}}\omega_0}{2Q_L}}\right]^2} \tag{A.6}$$

Abbreviations

ADC	Analog-to-Digital Converter
ARM	Advanced RISC Machines
BPF	Bandpass Filter
BPM	Beam Position Monitor
cPCI	Compact Peripheral Component Interconnect
DAC	Digital-to-Analog Converter
dB	Decibel
dBFS	Decibel Full Scale
dBm	Decibel milliWatt
DC	Direct Current
DFT	Discrete Fourier Transform
DSP	Digital Signal Processor
EPICS	Experimental Physics and Industrial Control System
FB	Feedback
FF	Feedforward
FIR	Finite Impulse Response
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
IF	Intermediate Frequency
IGBT	Insulated Gate Bipolar Transistor
IIR	Infinite Impulse Response
ILC	International Linear Collider
KEK	Ko Enerugi Kasokuki Kenkyu Kiko
LHC	Linear Hadron Collider
Linac	Linear Accelerator
LLRF	Low Level Radio Frequency
LO	Local Oscillator
LPF	Low Pass Filter
LUT	Look Up Table
MO	Master Oscillator
MTCA	Micro Telecommunications Computing Architecture
μTCA	Micro Telecommunications Computing Architecture
RF	Radio Frequency
RMS	Root Mean Square
SCRF	Superconducting Radio-Frequency
SNR	Signal to Noise Ratio
STF	Superconducting RF Test Facility

TESLA	TeV-Energy Superconducting Linear Accelerator
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
XFEL	X-ray Free Electron Laser

Symbol

A	Amplitude
A_{LO}	Amplitude of local oscillator
A_{RF}	Amplitude of radio frequency signal
β	Coupling factor
C	Capacitance
$\Delta\omega$	Detuning of cavity
f_{s}	Sampling frequency
f_{IF}	Intermediate frequency
I	In-phase component
I'	Rotated in-phase component
I_{f}	Forward current
I_{b}	Beam current
L	Inductance, Integer
N	Integer
ω	Angular frequency
$\omega_{1/2}$	Cavity bandwidth
P_{fill}	Required klystron power at filling time
P_{flat}	Required klystron power at flattop
ϕ	Phase
ϕ_{b}	Beam phase
ϕ_{LO}	Phase of local oscillator signal
ϕ_{RF}	Phase of radio frequency signal
Q	Quadrature component
Q'	Rotated quadrature component
Q_0	Unloaded quality factor
Q_{L}	Loaded quality factor
R	Rotation matrix
R_{L}	Loaded shunt impedance
u	Control signal
V_{cav}	Cavity voltage
V_{f}	Forward voltage
Z_{cav}	Cavity impedance
Z_{ext}	External load

List of Figures

List of Tables

Bibliography

[1] ILC. ILC Technical Design Report. *http://www.linearcollider.org/ILC/?pid=1000895*, 2013.

[2] H. Hayano *et al.* Results Achieved by the S1-Global Collaboration for ILC. *in* in Proceeding of Linear Accelerator Conference (LINAC'12), Tel-Aviv, Israel.

[3] H. Shimizu *et al.* X-ray generation by inverse Compton scattering at the superconducting RF test facility. *in* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment.

[4] A. Kuramoto. Alignment Detection Study using Beam Induced HOM at STF. *in* Proceedings of IPAC2013, Shanghai, 2013.

[5] M. Kuriki. RF Processing of L-Band RF Gun for KEK STF. *in* Proceedings of IPAC2011, San Sebastian, 2011.

[6] H. Hayano. Superconducting Accelerator Development at STF for ILC. *in* Proceedings of the 12th Annual Meeting of Particle Accelerator Society of Japan, Tsuruga, Japan, 2015.

[7] H. Shimizu *et al.* Progress of STF Accelerator Development for ILC. *in* Proceedings of the 13th Annual Meeting of Particle Accelerator Society of Japan August 8-10, 2016, Chiba, Japan.

[8] Y. Yamamoto. High Gradient Cavity Performance in STF-2 Cryomodule for the ILC at KEK. *Proceedings of the 2016 International Particle Accelerator Conference, Busan, Korea*, 2016.

[9] S. Fukuda. Status of RF Sources in Superconducting RF Test Facility (STF) at KEK. *Proceeding of Linear Accelerator Conference (LINAC'08), Victoria, Canada*, 2008.

[10] Mini Circuit. 10.7 Low-pass-filter. *https://www.minicircuits.com/pdfs/SLP-10.7+.pdf*.

[11] T. Schilcher. RF Application in Digital Signal Processing. *in* Proceeding of CERN Accelerator School on Digital Signal Processing, CAS2007, page 249, 2007.

[12] M. Grecki, T. Jezynki, A. Brandt. Estimation of IQ Vector Components of RF Field Theory and Implementation. *in* Proceedings of 12th Mixed Design of Integrated Circuits and Systems (MIXDES'05), Cracow, Poland, 2005.

[13] S.N. Simrock *et al.* Considerations for the Choice of the Intermediate Frequency and Sampling Rate for Digital RF Control. *Proceedings of European Particle Accelerator Conference (EPAC'06), Edinburgh, Scotland*, page 1462, 2006.

[14] F.Qiu *et al.* . Digital Filters Used for Digital Feedback System at CERL. *in* Proceeding of LINAC2014, Geneva, Switzerland, 2014.

[15] T. Schilcher. Vector Sum Control of Pulsed Accelerating Fields in Lorentz Force Detuned Superconducting Cavities. *in* PhD Thesis, 1998.

[16] A. Brandt. Development of Finite State Machine for the Automated Operation of the LLRF Control at FLASH. *in* PhD Thesis, University of Hamburg, 2007.

[17] S. Simrock and Z. Geng. Cavity Field Control - Cavity Theory. *in* International Accelerator School for Linear Collider, Turkey, 2013.

[18] S. Michizono et al. Performance of Digital LLRF system for STF in KEK. *LINAC'08, Victoria, Canada*, 2008.

[19] S.B. Wibowo. LLRF System Performance during SC Cavity Conditioning at STF KEK . *Proceedings of the 2016 International Particle Accelerator Conference, Busan, Korea*, 2016.

[20] S.B. Wibowo *et al.* Evaluation of Digital LLRF Control System Performance at STF in KEK. *International Particle Accelerator (IPAC'2017), Copenhagen, Denmark*, 2017.

[21] PICMG. MicroTCA. *https://www.picmg.org/openstandards/microtca/*, 1998.

[22] Analog Device. AD9650. *http://www.analog.com/media/en/technical-documentation/data-sheets/AD9650.pdf*.

[23] Analog Device. AD9783. *http://www.analog.com/media/en/technical-documentation/data-sheets/AD9780_9781_9783.pdf*.

[24] S.B. Wibowo *et al.* Digital LLRF Control System with Four Different Intermediate Frequencies for the International Linear Collider. *Physical Review Accelerator and Beam*, 2017.

[25] T. Matsumoto *et al.* Development of Digital Low-Level RF Control System using Multi-Intermediate Frequencies. *in* Proc. PAC'07*, New Mexico, USA*, 2007.

[26] T. Matsumoto *et al.* Performance of Digital Low-Level RF Control System with Four Intermediate Frequencies. *in* Proc. LINAC'08*, Victoria, Canada*, 2008.

[27] T. Matsumoto *et al.* Digital Low-Level RF Control System with Four Intermediate Frequencies at STF. *in* Proc. PAC'09*, Vancouver, Canada*, 2009.

[28] S.B. Wibowo *et al.* IF-mixture Performance during Cavity Conditioning at STF-KEK. *in* Proc. LINAC'16*, Michigan, USA*, 2016.

[29] P. L. Lui. Passive Intermodulation Interference in Communication Systems. *in* Electronics & Communication Engineering Journal, 1990.

[30] Analog Device. AD9510. *http://www.analog.com/media/en/technical-documentation/data-sheets/AD9510.pdf*.

[31] Sogo Electronics. *http://www.sogoel.co.jp/index.html*.

[32] Xilinx. Virtex-5 Family Overview. *https://www.xilinx.com/support/documentation/data_sheets/ds100.pdf*.

[33] Linear Technology. LTC2208. *http://cds.linear.com/docs/en/datasheet/2208fc.pdf*.

[34] T. Miura *et al.* Performance of the μTCA Digital Feedback Board for DRFS Test at KEK-STF. *in* Proc. IPAC'11*, San Sebastian, Spain*, 2011.

[35] H. Katagiri *et al.* High Speed Data Acquisition System using FPGA for LLRF Measurement and Control. *in* Proceeding of Linear Accelerator Conference (LINAC'2008), Victoria, Canada, (JACoW, Victoria, Canada, 2008).

[36] Y. Okada *et al.* Direct Sampling of RF Signal for 1.3 GHz Cavity. *in* Proceeding of Particle Accelerator Conference (PAC'2009), Vancouver, Canada, (JACoW, Vancouver, Canada, 2009).

[37] Linear Technology. AD5474. *http://www.ti.com/product/ADS5474*.

[38] W. Kester. Mixed-Signal and DSP Design Techniques. 2003.

[39] J. Branlard. First Commissioning Results of the European XFEL . *in* Presentation on Americas Workshop on Linear Colliders 2017, California, USA.

[40] V. Ayvazyan *et al.* Optimization of Filling Procedure for TESLA-Type Cavities for Klystron RF Power Minimization for European XFEL. *in* Proceeding of International Particle Accelerator (IPAC'10), Kyoto, Japan.

[41] Xilinx. Virtex-II Pro Overview. *https://www.xilinx.com/support/documentation/data_sheets/ds083.pdf*.

[42] Linear Technology. AD9764. *http://www.analog.com/media/en/technical-documentation/data-sheets/AD9764.pdf*.

[43] M. Akemoto *et al.* Long-Pulse Modulator Development for the Superconducting RF Test Facility (STF) at KEK. *in* Proceeding of International Particle Accelerator Conference (IPAC'2010), Kyoto, Japan, (JACoW, Kyoto, Japan, 2010).

[44] Xilinx. Spartan-6 Family Overview. *https://www.xilinx.com/support/documentation/data_sheets/ds160.pdf*.

Acknowledgments

I would like to thank my supervisor Prof. Toshihiro Matsumoto for his support and encouragement. I also thank Prof. Shinichiro Michizono for his advice and constant support. Furthermore, I thank Prof. Takako Miura and Dr. Feng Qiu.

I thank all the people at the STF for their great support during the experimental time at the STF.

I would like to express my gratitudes to all the people at KEK who offered me a chance to study at SOKENDAI through a KEK scholarship.

I thank all my colleagues, Emy Mulyani, Hirosawa, Liu Na, and Muhammad Abdurrahman for their support.

Finally, I would like to thank my family for their encouragements, amazing support, and patience.

Sigit Basuki Wibowo

Declaration

I declare that I wrote this preliminary Ph.D.–thesis independently and without any other references and resources than those stated in the bibliography.

Tsukuba, June 2017