# Study of Reliable Timing System at KEK Accelerator Complex

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June 2021

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# Declaration of Authorship

I, Di WANG, declare that this thesis titled, 'Study of Reliable Timing System at KEK Accelerator Complex' and the work presented in it are my own. I confirm that:

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- I have acknowledged all main sources of help.
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Date: June, 2021

**A dissertation submitted to Department of Accelerator Science,**
**School of High Energy Accelerator Science,**
**The Graduate University for Advanced Studies, SOKENDAI,**
**in partial fulfillment of the requirements for the degree of**
**Doctor of Philosophy**

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# *Abstract*

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Doctor of Philosophy

**Study of Reliable Timing System at KEK Accelerator Complex**

by Di WANG

The timing system provides high-precision signals to control a variety of hardware and software in the accelerator complex. At KEK, the timing system at injector linear accelerator (LINAC) is responsible for RF frequency synchronization between two SuperKEKB main rings (MR) and LINAC, trigger delivery, and bucket selection process. The LINAC timing system also provides trigger signals for two light source rings (PF/PF-AR) simultaneously, which demanding the timing system handle the injection procedure for 4 rings at 50 Hz. The beam properties and device control parameters are modulated every pulse through the timing system.

The event-based timing system generates event codes in an event generator (EVG) and distributes these event codes in a scheduled delay time to all local event receivers (EVR). The EVR module equips with the pulse generation circuit with variable pulse delay and width to supply trigger signals for hardware upon receiving the desired event code.

Several constraints from hardware must be considered during the design of the timing system. Some devices, like pulsed magnet power supply, need to be triggered at the same phase of the 50 Hz AC (AC50) power line to maintain a stable operation. Thus, the timing system operates under the AC50-dependent mode. On the other hand, the high-power klystron modulator needs at least 18 ms to accumulate power for klystron which results in a trigger interval restriction for consecutive injection pulse. The bucket selection cycle (BSC) is defined as a period that can select all the RF buckets inside a ring. The BSC for SuperKEKB electron beam injection is 493 $\mu$s which is effortless to synchronize with AC50 in 50 Hz. However, a newly constructed positron damping ring (DR) to lower the positron beam emittance enlarges the bucket selection period for a whole DR-MR cycle. The RF bucket number for DR and MR are 230 and 5120, respectively. The BSC for SuperKEKB positron beam injection becomes 23 times longer

(i.e., 11.34 ms) due to DR operation and the synchronization between BSC and AC50 in every pulse is broken. The AC line always fluctuates due to requirements from the power company. Consequently, a method called "sequence shift" is implemented to synchronize with both AC50 and BSC for positron as well as compensating for the AC line fluctuation. The length of the sequence and how the sequence shift is accomplished are described in detail.

Apart from the triggering function of a timing system, several significant features are also utilized to either meet the hardware requirement or improve the functionality of the timing system. The beam gate system provides a highly flexible way to disable the trigger delivery to specific devices, such as electron guns or DR injection and extraction magnet, without stopping the operation of EVG. The data buffer component contributes to the auxiliary data delivery, like beam mode, pulse ID, or bucket number information, other than normal trigger signal delivery.

Another limit of the numbers of selectable MR RF buckets for the 2-bunch and 2-pulse operation comes from the rising time of the DR kicker magnet field. To overcome this disadvantage, the RF phase in the downstream LINAC is modulated every pulse to increase the coincidence opportunity between DR RF and LINAC RF. The RF phase shift also brings time discrepancy of nanosecond scale between timing trigger and beam trigger. The beam behavior under such discrepancy is investigated to assure that the beam quality variation is acceptable for the SuperKEKB physics run. By means of the pulse-to-pulse RF phase modulation, all MR RF buckets can be selected in one pulse even during 2-bunch and 2-pulse operations.

The effort of establishing a reliable timing system at LINAC and several solutions to improve the system's robustness are presented in this work. During the commissioning of SuperKEKB, the beam error originates from the timing system was observed. This work mainly focuses on the failure mode analysis of the timing system at LINAC. We follow the procedure of failure mode analysis to understand the failure mode, identify the failure cause, and propose solutions. Several log systems for quickly diagnosing the complex system are built and tested. With the help of the log system, two failure modes called "beam mode replacement" and "redundant beam mode" are comprehensively analyzed and their failure causes are identified. The error can be categorized into two parts, the systematic error caused by either software bug or problematic system design, and the unexpected error caused by strong AC50 drift.

Several possibilities for solutions are discussed in this work. One solution is to remove the AC50 trigger dependency. A beam experiment is done by examining the beam quality degradation under the AC50-independent mode. According to the beam experiment, the AC50-independent operation is acceptable for SuperKEKB MR whereas not feasible

for PF injection due to the strong relationship between the power supply of the PF injection kicker magnet and AC50. Partially AC50-dependent operation mode is proposed by switching between the AC50-independent mode and AC50-dependent mode. Consequently, an AC50 regulator module is installed in the timing system to mask the strong AC50 drift and provide signals within 50±0.1 Hz to stabilize the timing system. A detailed analysis of the process logic and performance of the AC50 regulator module is represented in this thesis. Another possibility is to decrease the sequence length to mitigate the AC50 drift effect. The DR storage time becomes significant because both DR injection and extraction timing need to synchronize with AC50. The injection timing and extraction timing are strongly related without downstream LINAC RF phase shift. Thus, either decreasing the DR storage time or decoupling the DR injection and extraction pulse will allow us to shorten the sequence length. An improvement of the sequence shift algorithm is also necessary to handle some extremely strong AC50 drift situations. An example is given to illustrate how the sequence shift with considering recent AC drift value can increase the stability of the timing system.

# *Acknowledgements*

Many talented and amiable people shared their knowledge and helped form my thinking in this thesis. First and foremost, I want to thank my esteemed supervisors, Dr. Kazuro Furukawa and Dr. Masanori Satoh, who patiently gave me advices and recommendations to pursue interesting and significant problems in my area. The classes they taught provide not only invaluable insight of the historical evolution of accelerator control system but also the philosophy of phronesis on practical obstacle.

I am deeply grateful to Dr. Hiroshi Kaji, Dr. Hitoshi Sugimura, Dr. Fusashi Miyahara and Dr. Yoshinori Enomoto for their insightful comments and suggestions at every stage of the research project.

I would like to offer my special thanks to Dr. Tetsuo Shidara, Dr. Hiroyasu Ego, Dr. Takuya Natsui and Dr. Takako Miura for their kindly help on detailed explanation and test bench construction during my klystron experiment.

I have also benefitted from conversations with Mr. Yuichi Iitsuka, Mr. Takuya Kudou, Mr. Shiro Kusano, Mr. Hideki Saotome and many other staffs during the software programming and hardware debugging.

My leisure life in Japan becomes pleasing, satisfactory and cheerful with the help of my colleagues, Dr. Baiting Du, Dr. Na Liu, Dr. M.A. Rehman, Mrs. Min Yang, Mr. Ce Zhang, Mr. Yao Lu and Mr. Yuki Abe.

Last but not least, I want to thank all the open knowledge organizations, such as the Wikimedia Foundation and the Free Software Foundation, whose principles and methodologies are knowledge acquirement is a basic human-rights. What they pursue inspires me to insist on the belief of the existence of common good for all human.

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# Abbreviations

| | |
|---|---|
| **HER** | High Energy Ring |
| **LER** | Low Energy Ring |
| **MR** | Main Ring |
| **DR** | Damping Ring |
| **RF** | Radio frequency |
| **FC** | Flux Concentrator |
| **EPICS** | Experimental Ehysics and Industrial Control System |
| **OPI** | Operator Interface |
| **IOC** | Input/Output Controller |
| **CA** | Channel Access |
| **DB** | Database |
| **BRR** | Beam Repetition Rate |
| **EBTS** | Event-based Timing System |
| **TBTS** | Timestamp-based timing system |
| **MRF** | Micro-Research Finland |
| **EVG** | Event Generator |
| **EVR** | Event Receiver |
| **DBus** | Distrubuted Bus |
| **WR** | White Rabbit |
| **TDC** | Time-to-Digital Converter |
| **MTG** | Master Trigger Generator |
| **RFM** | reflective Memory |
| **MTS** | Main Timing Station |
| **MO** | Master Oscillator |
| **MMO** | Main Master Oscillator |

| | |
|---|---|
| **SHB** | Subharmonic Buncher |
| **BSC** | Bucket Selection Cycle |
| **BCE** | Bunch Current Equalizer |
| **BCM** | Bunch Current Monitor |
| **CCB** | Central Control Building |
| **PPM** | Pulse-to-pulse Modulation |
| **IP-GEN** | Injection Pattern Generator |

# Chapter 1

# Introduction

## 1.1 Accelerator Complex at KEK

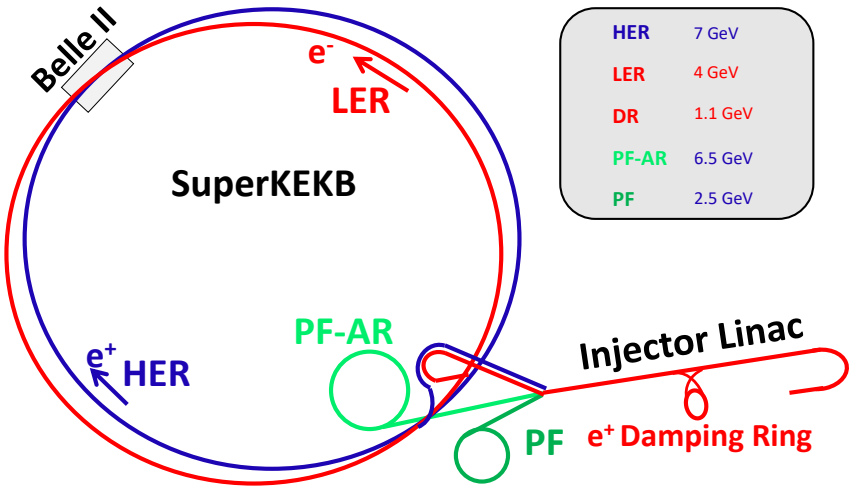


FIGURE 1.1: Overview of the LINAC, SuperKEKB and PF/PF-AR.

The accelerator complex at KEK consists of an injector linear accelerator (LINAC), an electron/positron double-ring collider SuperKEKB, and two synchrotron light source facilities (PF and PF-AR). The SuperKEKB is an upgrade project of KEKB which operated at KEK from 1998 to 2010 and achieved the world-highest peak luminosity of $2.018 \times 10^{34} cm^{-2} s^{-1}$. SuperKEKB is designed to aim at peak luminosity of $8 \times$

$10^{35} cm^{-2} s^{-1}$ which is 40 times higher than the KEKB [4]. The beams which are stored in two main rings (MRs), a 7 GeV high energy electron ring (HER) and a 4 GeV low energy positron ring (LER), collide at the interaction point and are detected by the Belle II detector. The physics goal of the Belle II experiment is to search for new physics in the flavor sector at the luminosity frontier. A low-emittance beam is indispensable to implement the nano-beam scheme for higher SuperKEKB collision efficiency. Apart from supplying beams for the SuperKEKB collider the LINAC also provides beams for two light source facilities, 2.5 GeV Photon Factory (PF) and 6.5 GeV Photon Factory Advanced Ring (PF-AR) [5, 6]. The schematic view of the accelerator complex is shown in Fig. 1.1.

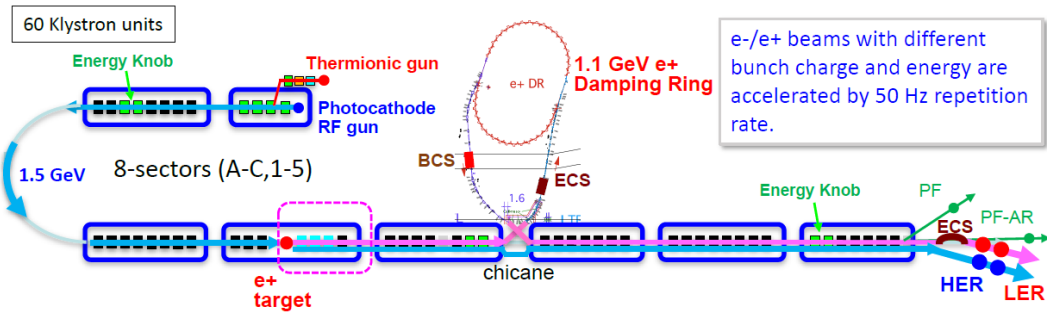


FIGURE 1.2: Schematic layout of 600-m injector LINAC.

A schematic layout of LINAC is shown in Fig. 1.2. The 600-m LINAC is composed of 60 high-power radio frequency (RF) accelerating units distributed at eight sectors (sector A-C and 1-5). The requirements for the LINAC are full energy injection into the SuperKEKB rings with an energy spread of 0.1%. A photo-cathode high-current RF gun generates a high-charge electron bunch (up to 4 nC) into the SuperKEKB high energy ring (HER) while the thermionic gun is adopted for generating electron beams for PF, PF-AR, as well as for positron beam generation. The low-emittance and high-current positron beam is generated by a positron target located between sector "2" and sector "3". After a flux concentrator (FC) and large-aperture accelerating structures, the beam is then transferred by a beam switchyard and damped to low emittance through a damping ring (DR). Finally, the positron beam re-enters LINAC and is accelerated up to 4 GeV.

The LINAC RF system converts the high voltage pulses from the modulator into pulsed RF power and sends them to the accelerating units to set up an electric field which is used for charged particle acceleration. The bunches inside MRs perform a longitudinal

synchrotron oscillation and are contained inside a stable area called an RF bucket. The number of MR RF buckets is determined by the RF frequency and circumference of MR. The bunch will gradually become lost if the injection timing cannot match the synchronous phase between the LINAC and MR. To equalize the bunch distribution inside the ring as well as avoid strong coupled-bunch instabilities, the injection RF bucket should be selected based on the timing system. This procedure is called bucket selection. The bucket selection is one of the main tasks of the accelerator timing system. In addition, the timing system controls the injection by synchronizing all the relevant components to operate at a scheduled sequence. For example, the timing system provides trigger signals for the low-level and high-power RF systems, pulsed magnets, electron guns, injection systems, and beam instrumentation at LINAC. A precise RF synchronization should be provided to allow particles to pass between accelerators. To satisfy the flexibility requirements of series accelerators, a strategy called pulse-to-pulse modulation (PPM) was proposed at CERN to achieve the control of a time-shared injection [7]. As a multi-accelerator facility, the PPM is imperative to avoid accelerator dead-time and this method is also implemented at the KEK accelerator complex to modulate the beam properties for SuperKEKB, PF, and PF-AR. The modulated items include the beam mode, bucket number, RF phase in LINAC, and many other control parameters.

## 1.2 EPICS

The operation of particle accelerators requires high-performance electronics for beam diagnostics, data acquisition, and machine control. These electronics should integrate with several control subsystems to consist of a common architecture. Consequently, the **E**xperimental **P**hysics and **I**ndustrial **C**ontrol **S**ystem (EPICS) is employed as a de-facto standard in the community of accelerator control system. EPICS is a general-purpose control system framework that is maintained by an international joint development project called EPICS collaboration. Before the 1990s, the accelerator control system is usually accelerator-specific. Many home-grown controllers, cables as well as various data transmission protocols are utilized at different institutes. Thus, it is difficult to share common-used components among institutes via collaboration. To increase the high availability, scalability, and flexibility, EPICS was initially developed by Los Alamos National Laboratory (LANL) and Argonne National Laboratory (ANL) for the

construction of control systems in 1987 [8]. Owing to its high-reliable, powerful, and distributed attributes, EPICS now is chosen at many institutes all over the world, such as SLAC, BNL, FNAL, DESY, PSI, and KEK [9].

The basic components of EPICS consist of Operator Interface (OPI), Input/Output Controller (IOC), and LAN (Local Area Network). EPICS is based on the multi-layer architecture, in which the lower layer is responsible for the I/O with different pieces of hardware, and the upper layer is designed to provide hardware-independent services to the OPI layer. EPICS uses Client/Server techniques to communicate between OPI and IOC through an Ethernet-based network. From a software architecture perspective, EPICS IOC consists of the followings:

- **EPICS base**, the core software of EPICS which includes the application programming interface (API), EPICS database access, standard EPICS record support and device support, several tools for building EPICS application and EPICS extensions. The **base** is normally provided by EPICS collaboration.
- **EPICS application**, which usually includes EPICS IOC, a user-defined EPICS database to control the hardware components, a Channel Access (CA) server which provides remote control through TCP/IP network. The **application** is used to control dedicated hardware.
- **EPICS extension**, which includes function-enhancement applications not included in EPICS base, such as the EPICS sequencer, AutoSave, and procServer. The **extensions** are developed by worldwide institutes and shared via collaboration.

Accelerator components such as magnet, vacuum, are controlled by IOC database (DB), which is unlike a relational database. IOC DBs are instances of different data structures called EPICS records and each record type has one or more associated sets of record support routines. Each record has its record type and dedicated behavior. The field of the record is the basic unit for EPICS DB. One of the most important fields is the "VAL" field, which typically holds the data for device input/output or some intermediate calculation results. Records can communicate with each other through a reference link called DB link or through CA link [10]. For example, when writing a value to the "VAL" field of analog output ("**ao**") record, it performs the engineering unit convert and then

calls the correspondent device-specific support routine to perform the I/O with the device. Then it can trigger the process of another analog input ("**ai**") record to set the readback value into the "VAL" field to check whether the command is executed.

A channel-based data exchange protocol called CA serves as the communication protocol between IOC and OPI. One channel corresponds to a combination of record name and field name like "record_name.field_name". The IOC DB information is published to clients using the CA network protocol. The basic actions of CA are "Get", "Put", and "Monitor", which allow the client to read, write and monitor the data inside one IOC.

## 1.3 Reliability Engineering

Several conceptions should be clarified and defined before further discussion on a reliable timing system. From the perspective of reliability engineering, *reliability* is the ability of a system or component to perform as designed, which means without failure, in an operational environment for a specified period [11]. The term "perform as designed" means the system is supposed to meet *system requirements*. The system requirements can be derived from different subjects,

- *Function requirements* care about what a system is supposed to do.
- *Performance requirements* concern the efficiency (i.e., time consumed) of a system.
- *Physical requirements* relate to the physical entity such as size and weight of the devices as well mechanical and electrical characteristics.
- *Safety requirements* focus on the protection of human life and machine while the system is under operational.

The reliability of a timing system mainly concerns function requirements and performance requirements while physical requirements and safety requirements are implicit in the personnel protection system (PPS) and machine protection system (MPS) [12]. The functional requirements of a timing system regulate whether the timing system realizes three basic functionalities which include RF synchronization, trigger delivery, and bucket selection. The performance requirements examine the precision and accuracy of trigger signals as well as the response delay of the system.

According to the definition of reliability, the reliability requirements are distinct from the system requirements which not only refer to the system requirements but also care about the operating conditions and period during normal operation. The reliability requirements do not force the system to operate under any circumstance or function well forever. On the contrary, the reliability requirements only need to satisfy certain conditions and in a fixed period. For example, the timing system at KEK LINAC does not guarantee a stable operation when an earthquake occurs. Owing to two times yearly maintenance, the timing system is required to work 24 hours a day, 7 days a week, constantly for 6 months. The reliability requirements can be evaluated through several factors which include,

- frequency of failures,
- how long do outages last,
- costs,
- impact of failures.

The *failure* is defined as the violation of one or more system requirements and *outage* is the period following a failure. The occurrence of a failure represents the start of an outage, and the outage persists until the recovery is done. The failure can be further divided into "hard failures" and "soft failures" based on the severity of consequence. For example, in an accelerator timing system, there is often a trigger precision requirement, for example, a jitter of less than 30 ps (r.m.s) for SuperKEKB MR [1, 13, 14]) is required. The violation of the jitter requirement in a single pulse may not cease the operation of the timing system or beam operation if the beam quality is acceptable for the ring. On the other hand, the suspending of delivery of event timing signals caused by wrong programming logic stops the timing system as well as beam operation. The former can be regarded as a "soft failure" while the latter is a "hard failure".

The words *failure mode*, *failure mechanism* and *failure cause* are used to describe the attribute of failure. For instance, the pause of event codes delivery in an event-based timing system is a failure mode. The vibration of the event generator module, CPU module, and transmission cable is a failure mechanism. The failure cause is used to describe the root reason, e.g., earthquake. By analyzing the failure mode, the deduced

failure mechanisms are a chain of causes, and the root cause becomes the failure cause. The failure is corrected by applying suitable countermeasures based on the failure cause.

While it is a fundamental goal to meet the reliability requirements in reliability engineering, maintainability and supportability also play a significant role in reliability. Many factors involved in prompting system reliability are listed below.

- Failure location diagnostics,
- Technical documentation and message sharing,
- Workflow management,
- Data and information acquisition,
- Failure monitoring and report
- Software review and audit,
- Spare parts stocking and inventory management,

A universal procedure for reliability analysis starts from the system requirements analysis. After what the system does and how the system responds are thoroughly comprehended, the maintainability and supportability methods, such as failure location identification and failure data monitoring, are deployed to contribute to the failure mode analysis. The reliability requirements evaluation is also reported based on failure data. These steps are discussed in Section 6 as an example for reliability analysis of the timing system at LINAC.

## 1.4 Motivation of this study

The goal of this thesis is to give an insight into the reliability of an accelerator timing system and stabilize the timing system for SuperKEKB injector LINAC. Apart from the normal implementation of an accelerator timing system, several specific requirements demand the architecture of the timing system at KEK. These requirements and corresponding solutions are discussed in this work. During the operation, the failure of the timing system significantly affects the physics run. A thorough analysis of the

failure effects and causes becomes urgent to increase the beam operation time and thus contributing to the luminosity goal of the SuperKEKB collider.

Firstly, the event codes and timestamps should be recorded as these data are basic evidence to identify the timing system error. To construct an event code log system, the driver for the event timing module (i.e., EVR) is modified. The logging speed must be carefully considered since the event clock is 144.24 MHz. After the trial of an EPICS-based event code log system, a relatively low-level log system is tested and successfully saves the event codes without data loss. The AC50 arrival timing log is also developed since the arrival timing of AC50 is a significant fiducial point during sequence shift. Finally, we found that most of the timing failure is caused by strong AC50 drift by identifying the failure mode and analyzing the failure mechanisms. The degree of AC50 fluctuation is measured and provides a quantitative assessment of failure frequency.

Several solutions by decreasing the length of sequence are proposed to solve the AC50 drift problem. An AC50 regulator is used to mask the strong AC50 drift. This method degrades the beam quality and prohibits the injection of PF. Though it stabilizes the timing system, the possibility of a fully functional timing system is discussed. The method is to shorten sequence length by examining the possibility of removing the dependency between DR injection and extraction either through decreasing maximum DR storage time or through shifting the downstream LINAC RF phase. The beam energy deviation and operation stability of some hardware are tested. By shortening the sequence length and improving the sequence shift algorithm, the newer timing system can handle extremely strong AC50 drift. Finally, the timing system should be stable enough to provide trigger signals for accelerator devices and serves as a reliable component of the accelerator control system.

## 1.5 Structure of Thesis

The thesis consists of eight chapters. The basic structure of this thesis is given as follows:

- **Chapter 2** gives the overview of the accelerator timing system and introduce different classifications of timing system which mainly include event-based timing system and timestamp-based timing system.

- **Chapter 3** introduces the basic blocks of the timing system at the KEK accelerator complex. Some major hardware and basic parameters of the timing system are introduced.

- **Chapter 4** discusses the main requirements of the timing system at KEK LINAC. These requirements come from either the hardware, such as klystron and pulsed kicker magnet, or the systematic structure, such as DR operation and pulse-to-pulse modulation process.

- **Chapter 5** talks about the detailed implementation of the timing system at KEK LINAC which includes the reason for the sequence shift scheme and sequence shift algorithm. The core part of the LINAC timing system, i.e., the main timing station, is also analyzed and the control logic is displayed. The solution of bucket selection limit caused by 2-bunch and 2-pulse DR operation is evaluated using LINAC RF phase shift.

- **Chapter 6** shows the failure modes during the timing system operation and failure causes are discussed. The failure mechanism about how the timing system is affected by strong AC50 drift is demonstrated and further analysis of AC50 drift is done in this chapter.

- **Chapter 7** illustrates the attempt to stabilize the timing system and propose the possible timing system upgrade.

- **Chapter 8** summarizes the thesis.

# Chapter 2

# Accelerator Timing System

## 2.1 RF Synchronization and Bucket Selection

For a larger experimental physics accelerator, the basic idea of a timing system is to broadcast a timing clock and a master trigger signal. The timing clock can be thought of as a sinuous wave that decides the timing system resolution. The master trigger which usually originates from external stimulus is synchronized with the timing clock by a counter counting ticks of the clock from a fiducial point. A typical timing system consists of three parts, generation, transmission, and receiving:

- The main timing station with a master oscillator for RF clock synchronization and master trigger signal generation.
- A long-distance signal transmission network with low loss and good phase stability.
- A local timing station with receiver modules and delay modules where the trigger signal is detected and delayed device-dependent pulsed timing is outputted to the instruments.

A representative scenario of an accelerator timing system starts with the trigger of a pulsed magnet power supply to maintain a stable flat top magnetic field, the gun is

then fired to generate the particles while the RF system must follow a proper phase relation with the beam to achieve the desired accelerating effect. In addition, the bunch injection timing needs to be sufficiently precise to meet the storage ring requirement and the diagnostic devices, such as beam feedback systems and beam monitors, which must match its measurement window with the beam arrival timing.

One should keep in mind that a constant time deviation, for example, the beam traveling time in a beam transport line, is insignificant if this time interval is known and simply compensated through programmable delay generator modules. The fixed transmission delay value is usually calculated by physics simulation and observation of the real beam arrival time. The fixed transmission delay is neglected in later descriptions for simplicity. However, the variable transmission delay caused by the thermal effect of cable is non-negligible for jitter consideration.

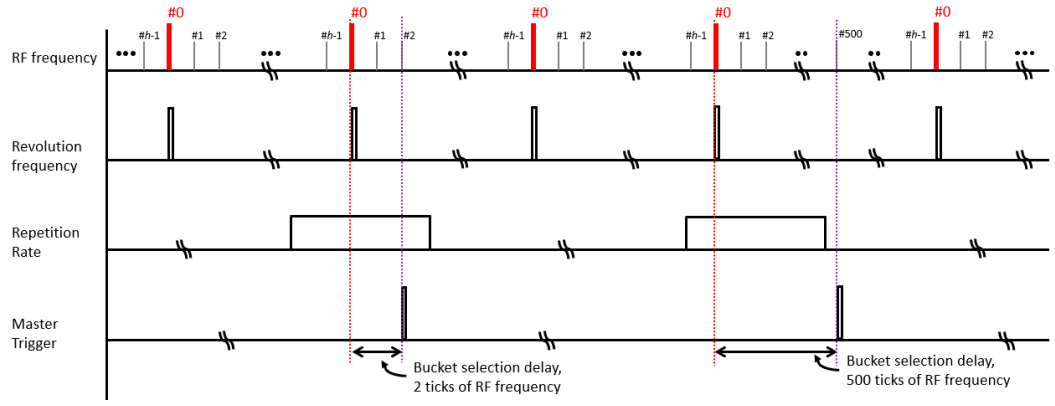


FIGURE 2.1: Timing sequence.

High precision RF synchronization can be accomplished through stable master oscillators, phase-locked loops (PLLs) and frequency synthesizers which includes integer-N and fractional-N type. Apart from the distribution of RF signals, one major task of the accelerator timing system is to calculate the bucket selection delay. Bucket selection is important for top-up injection to equate bunch current and maximize the usage of RF power. To ensure that the circulated particles always see an accelerating RF field, the ring RF frequency must be an integer multiple of the ring revolution frequency. The relation is expressed in Eq. 2.1.

$$f_{rf} = h * f_{rev} \tag{2.1}$$

The symbol $h$ is known as the harmonic number, which also represents total RF bucket numbers inside a storage ring. The revolution frequency $f_{rev}$ is determined by the speed of the particle and the circumference of the ring. $f_{rev}$ can be acquired by dividing the accelerating RF frequency $f_{rf}$ by harmonic number $h$. The obtained clock also assigns one out of the $h$ RF buckets, which can be defined as bucket "#0". As Fig. 2.1 shows, if injection is performing under $f_{rev}$, bucket "#0" is injected every time. By shifting ticks of $f_{rf}$, another RF bucket can be defined as "#0" and this technique is useful during the collision point tuning for double rings. After bucket "#0" is defined, an arbitrary RF bucket can be selected by delaying proper pulses of the ring RF clock period. The frequency during which all the RF buckets can be filled once is defined as a bucket selection cycle (BSC), denoted as $f_{BS}$. Also, note that $f_{BS}$ should be integrally related with $f_{rev}$ if there is no phase shift either in the ring or LINAC. For example, the coefficient between $f_{BS}$ and $f_{ref}$ in Fig. 2.1 is "1", which means $f_{BS} = f_{rev}$.

For a better illustration of the RF synchronization and bucket selection scheme, let us consider a virtual electron accelerator complex that has a linear accelerator (LI), a damping ring (DR), and the main storage ring (MR). The RF frequencies are expressed as $f_{LI-RF}$, $f_{DR-RF}$ and $f_{MR-RF}$ respectively. $f_{DR-REV}$ and $f_{MR-REV}$ stand for the revolution frequency of DR and MR. $h_{DR}$ and $h_{MR}$ are the harmonic number of DR and MR.

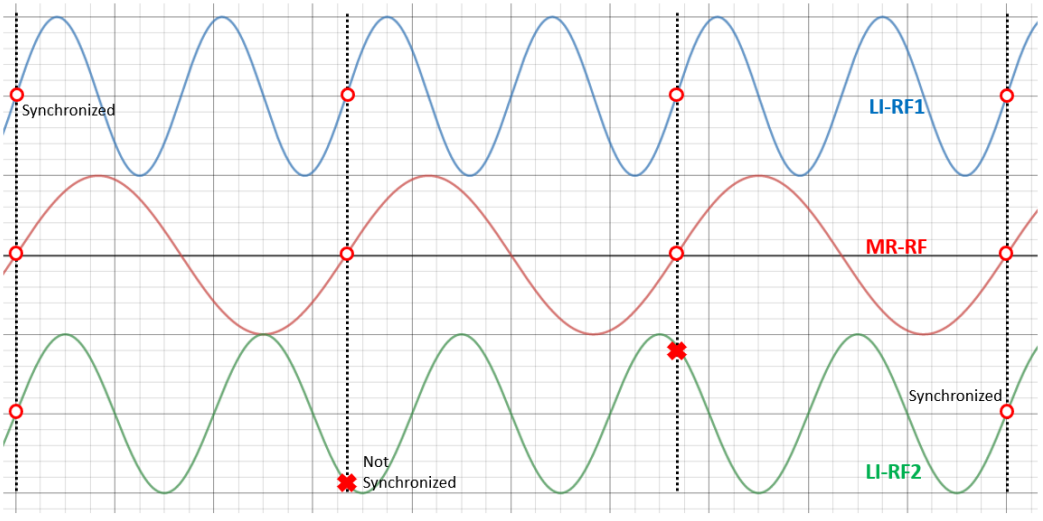


FIGURE 2.2: The injection opportunity is decided by $f_{LI-RF}$ and $f_{MR-RF}$.

First, let us omit the DR and consider the beam injection between LI and MR. The beam should sit at the same accelerating RF phase both in the LI accelerating structure

and MR. As Fig. 2.2 shows, if $f_{LI-RF}$ is an integer multiple of $f_{MR-RF}$, the injection opportunity appears every tick of $f_{MR-RF}$. Otherwise, if $f_{LI-RF}$ and $f_{MR-RF}$ satisfy the relation,

$$f_{LI-RF} * m = f_{MR-RF} * n \tag{2.2}$$

where two integers $m$ and $n$ are mutually prime. The injection opportunity appears in the greatest common frequency of $f_{LI-RF}$ and $f_{MR-RF}$. This injection frequency is described as $f_{LI-MR-CF}$. The common frequency may be referred as other names, such as coincidence frequency or intermediate frequency. The value of $f_{LI-MR-CF}$ can be calculated from,

$$f_{LI-MR-CF} = \frac{f_{MR-RF}}{m} = \frac{f_{LI-RF}}{n} \tag{2.3}$$

Thus, from Eq. 2.3, the BSC for MR ($f_{LI-MR-BS}$) is derived as,

$$f_{LI-MR-BS} = \frac{f_{LI-MR-CF}}{h_{MR}} = \frac{f_{MR-RF}}{m * h_{MR}} \tag{2.4}$$

The bucket "#0" can be filled if the injection is performing based on $f_{LI-MR-BS}$. Then a delay may be added to select a bucket in the MR. The delay value should be an integer multiple of $f_{LI-MR-CF}$.

Next, let us omit the LI and consider the synchronization between DR extraction and MR injection. Similarly, to transfer the beam from DR to MR, the common frequency $f_{DR-MR-CF}$ between revolution frequencies of two rings should be used,

$$f_{DR-MR-CF} = \frac{f_{DR-REV}}{p} = \frac{f_{MR-REV}}{q} \tag{2.5}$$

where $p$ and $q$ are integers. For lepton accelerators, the RF frequencies for DR and MR are usually the same. Thus, according to Eq. 2.1, $p/q$ is the ratio of MR and DR harmonic number. The BSC for DR and MR $f_{DR-MR-BS}$ is the same as $f_{DR-MR-CF}$.

Finally, considering LI, DR and MR together, the overall BSC for DR and MR $f_{LI-DR-MR-BS}$ is derived as,

$$f_{LI-DR-MR-BS} = \frac{f_{DR-MR-CF}}{m} = \frac{f_{MR-RF}}{q * m * h_{MR}} \tag{2.6}$$

For our virtual accelerator, to synchronize the beam injection of LI, DR, and MR, $f_{LI-DR-MR-BS}$ or any integer multiple of it should be used. The Eq. 2.6 is applicable

for most electron colliders and synchrotron light sources. However, there exist several exceptions, for example, the phase shift of accelerators, particle type changing at transfer line, or hadron accelerators with slow beam velocity which induces an "inconstant" ring RF frequency, to break this rule. These restrictions are typically accelerator-dependent, and examples can be found at CERN accelerators [15].

## 2.2 Classification of Timing System

### 2.2.1 Fast Timing and Slow Timing

Based on different criteria, the timing system can be categorized into different groups. One of the most intuitive aspects is the timescale. Several dividing lines exist as the reference and separates the timing system as "fast timing" and "slow timing". The timescale in a normal accelerator is listed in descending order.

1. Beam repetition rate
2. Storage ring revolution frequency
3. Single bunch monitoring
4. RF accelerating phase

The beam repetition rate (BRR), which is limited by pulsed devices, like modulators of high-power RF system, should usually follow the AC power grid line, such as 60 Hz in USA and Canada, 50 Hz in European and Eastern Japan, to stabilize the klystron beam current heated by AC power line on consecutive triggers. The storage ring revolution frequency is of great importance to the beam current measurement as well as the injection matching between the injector linear accelerator and storage ring. The bunch control usually lies at the nanosecond timescale. A fine adjustment of the RF accelerating phase should achieve a precision of femtoseconds. Often for colliders and synchrotron light source facilities, the boundary between "fast timing" and "slow timing" is usually that the "slow timing" handles timing signals slower than one storage revolution frequency while the "fast timing" is responsible for a single bunch level.

A representative example of this classification is the timing system of **T**ransposable **R**ing **I**ntersecting **ST**orage **A**ccelerator in **N**ippon (TRISTAN) project, which is the former project before KEKB accelerator. The "fast timing" supplies timing signals for beam monitors and beam feedback systems. The timing resolution is 1.5 ns for a 508 MHz main ring and RF bucket matching precision between the accumulation ring and the main ring can achieve within ±6 ps through RF synthesizers and PLL circuit. The "slow timing" for TRISTAN is relaxed to 100 Hz for controlling operation mode or RF accelerating voltage. It is achieved using a serial bus using Manchester II code, based on the standard MIL/STD-1553B [16–18].

Now, the dividing line between "fast timing" and "slow timing" is vaguer with the evolution of high-precision electronics. For example, at KEK LINAC, the BRR is 50 Hz, the SuperKEKB MR revolution period is around 10 $\mu$s, the bunch spacing inside the MR is about 2 ns, and the timing jitter of injection should be less than 30 ps. All these trigger signals can be provided by an event-based timing system.

### 2.2.2 Analogue Timing and Digital Timing

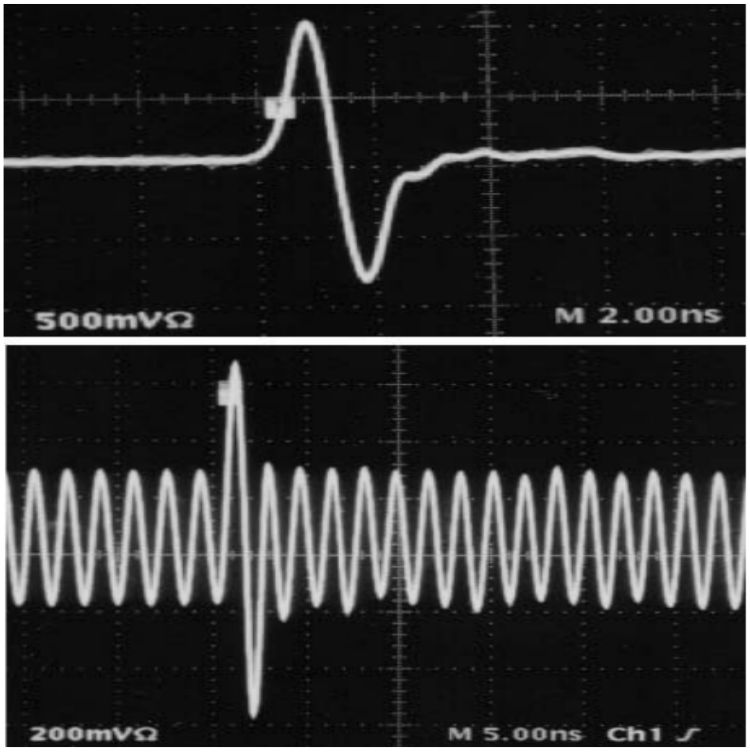


FIGURE 2.3: The 50 Hz timing trigger signal (up) and 571.2 MHz clock signal (down) were generated at the LINAC main timing station and distributed to the remote stations through coaxial cable in the KEKB project era [1].

The transmission method of timing signal also leads to another classification method of the timing system. As Fig. 2.3 shows, by combining the RF clock signal and master timing trigger, the analog signal transmission timing system is utilized. The RF frequency that is served as a carrier wave and a timing trigger signal is overlaid in a transmitter module and distributed to the facility through a coaxial cable. The RF frequency is then regenerated through a bandpass filter in the local receiver module while the master trigger signal is detected by a voltage discriminator circuit. The master trigger signal is used for a start pulse of a delay module which is driven by a recovered RF clock. This method can achieve very high precision and is wildly used for accelerator facilities before the 1990s [1]. However, there exists several drawbacks of analog timing transmission. One of the problems is the signal attenuation of coaxial cable during long-distance transmission. Thus, many cascaded fanout modules, receivers, as well as cabling are required to maintain a satisfactory signal accuracy which results in a high cost [19]. Another disadvantage is the difficulty of diagnosing the timing system since no extra information such as timestamp, beam mode, and beam properties, are provided to the device. Lack of flexibility is also a troublesome issue for operation. For example, it is difficult to switch the device seamlessly if machine study and beam operation are performed continuously.

By encoding the trigger messages onto a synchronized RF carrier clock, the digital transmission is used to broadcast the data stream called timing events from one master station to all the local stations. The transmitter is responsible for modulating the numeric codes while the receiver performs demodulation. Due to the stability of the digital signal, a good quality twisted pair cabling or optical fiber can replace the coaxing cable to construct the timing network. The main advantages of the digital transmission compared with the analog transmission are,

- The flexibility of device control is extended for future upgrades.
- Increase the stability of long-distance (km range) transmission through optical-fiber-based timing network.
- The field wiring is simplified and the cost is reduced.
- Communication standards can be agreed to maintain a universal solution and shared among scientific facilities.

- Encoded digital data through line code technology enhances the error detection ability.
- Timestamp information for diagnosis can be encoded and sent from the master to slave nodes.

Note that it is difficult to achieve RF synchronization and low-level RF (LLRF) control by adding digital delay to the electronics because of the strict RF phase stability requirement. The analog timing and digital timing approaches are combined for nowadays accelerators.

### 2.2.3 Event-based Timing and Timestamp-based Timing

Imagine somebody wants many pulsed magnets to trigger all at midday exactly in a sub-nanosecond timescale. One solution, called event-based timing system (EBTS), is to distribute event messages through Fan-Out units that are generated at a master event generator module, to which the event receiver modules would respond to the messages by producing pulses with carefully calculated delay to drive the pulsed magnets. The event generator module is also responsible for clock synchronization and encoding of event codes. The event receiver module is responsible for decoding the optical signal and producing output signals.

Another common and straightforward strategy, called timestamp-based timing system (TBTS), which is quite like the event-based timing system, works by transmitting the timestamp information over the timing network using techniques that we will describe later, to synchronize the internal notion of time typing in a nanosecond resolution. After the receiver modules are all time-locked, the instruction for firing the pulsed magnets at midday is broadcasted before midday. Then, the receiver modules generate output pulses to the devices when the local timestamp matches the timing decoded from the instruction.

## 2.3 EBTS

Though many accelerators started to distribute timing events using digital transmission, such as the **L**arge **E**lectron–**P**ositron Collider (LEP) project at CERN and the TRISTAN project at KEK, the attempt of designing a modularized EBTS was implemented for the Tevatron project at Fermilab [17, 20]. The highly integrated Fermilab event receiver modules can decode the events using modified Manchester encoding, recover the global event clock, generate programmable VME interrupts, save the event codes into an event FIFO memory together with a high-resolution timestamp, and output pulse to the device. The event system developed by Frank R. Lenkszus and Robert Laird at the **A**dvanced **P**hoton **S**ource (APS) in 1994 is another elegant example [21]. As shown in Fig. 2.4, the APS EBTS consists of a VME event generator card that receives hardware and software trigger inputs and converts them to 8-bit event codes using 8b/10b encoding [22]. The event codes are stored at two sequence RAM and sent sequentially under the external clock rate. The receiver card has several outputs which include 14 fixed-delay outputs, 7 set-reset flipflop outputs, and 4 delayed-pulse outputs. Other features include the heartbeat event code transmission, event code priority encoder for collision avoiding, event and timestamp FIFO for buffering, EPICS environment integration, and timestamp synchronization. The APS EBTS design was also selected for the **S**wiss **L**ight **S**ource (SLS) with several important feature upgrades like the "distributed bus (DBus)" transmission function.

With the practice of these projects, a generic toolkit of EBTS evolves gradually based on worldwide collaboration. One of the most popular and representative EBTS implementations is developed by Micro-Research Finland (MRF) company which focuses on timing systems for particle accelerators. The MRF EBTS consists of a family of products for different event generators (EVGs) and event receivers (EVRs) like VME, CompactPCI, and MicroTCA. The topology of the MRF event timing network is shown in Fig. 2.5. We will briefly illustrate the key features of MRF EVG and EVR and the detailed specification can be referred from the official manuals. Note that several new features like delay compensation are brought into the newly released products, the discussion in this section mainly focuses on the VME-EVG-230 and VME-EVR-230, which are currently used at KEK LINAC.

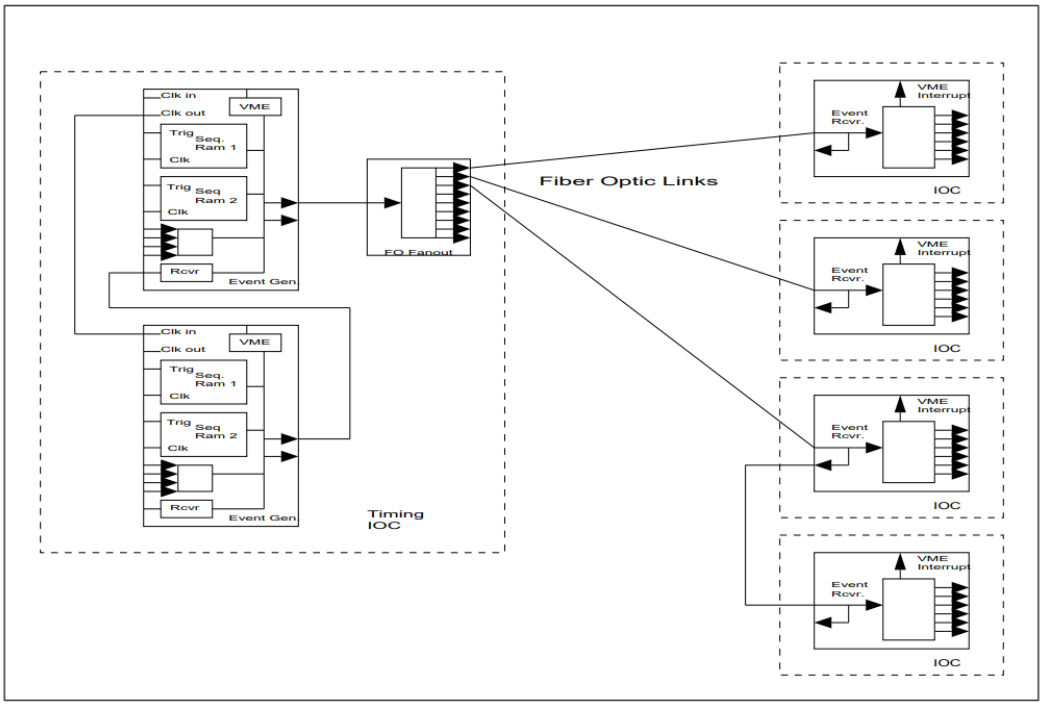


FIGURE 2.4: EBTS for APS. Two event generators are cascaded and transmit event codes as well as periodic timestamp events to an array of event receivers through fiber optic links.

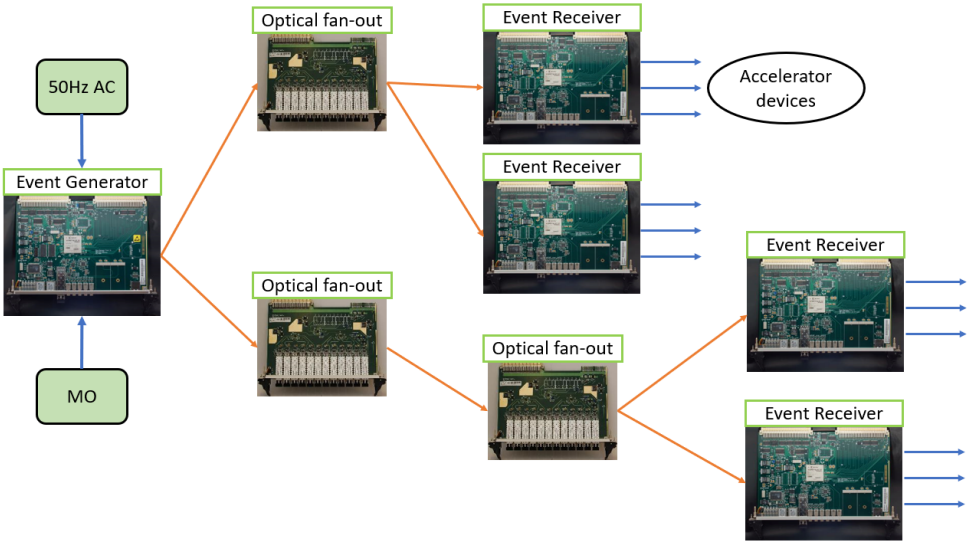


FIGURE 2.5: A typical layout of event timing system.

### 2.3.1 RF Clock and Event Clock

All operations on EVG and EVR are synchronized to the event clock which ranges between 50 MHz and 125 MHz. The event codes are transferred through optical fiber under the event clock which is regenerated on local EVRs. The event clock is derived from

either an external RF clock or from an onboard fractional synthesizer. The maximum RF frequency is limited by the internal circuit at 1.6 GHz.

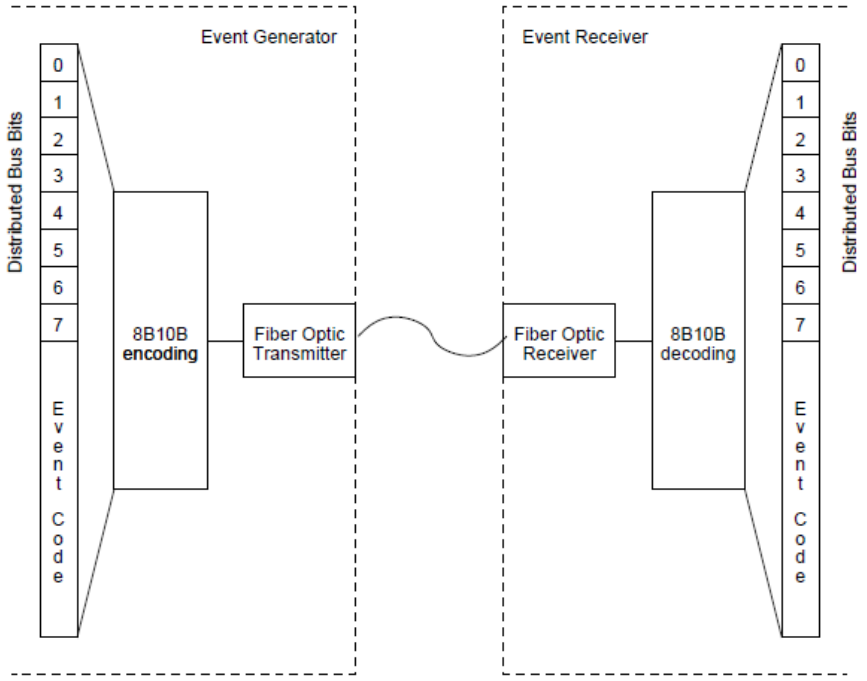


FIGURE 2.6: The event stream consist of a combination of 8-bit event codes and data sent out at the event clock.

### 2.3.2 Event Stream

The limitation of the APS EBTS is that only one event can be transmitted at one event clock period. To overcome this, as shown in Fig. 2.6, MRF EBTS uses a 16-bit frame (called an event stream) to send the data together with the 8-bit event codes. The 8-bit data can be taken from either the DBus or from an optional 2 kB dual-port memory called Data Buffer. Eight DBus data are transmitted simultaneously either with the event clock time resolution or half which depends on whether Data Buffer is enabled. The 8B10B protocol is used for parallel/serial conversion, in that the serial clock is 20 times of event clock.

### 2.3.3 AC Trigger

It is usually necessary to synchronize the timing trigger with the AC power line to keep many devices operate at a constant AC phase, e.g., at the zero-crossing point. Normally

a repetition rate generator module should be developed to provide the trigger signal. Thus, the EVG module provides the functionality of synchronization between the AC power line and the event clock. The synchronized signal can be used to trigger the sequence RAM (see Section 2.3.6) or a trigger event.

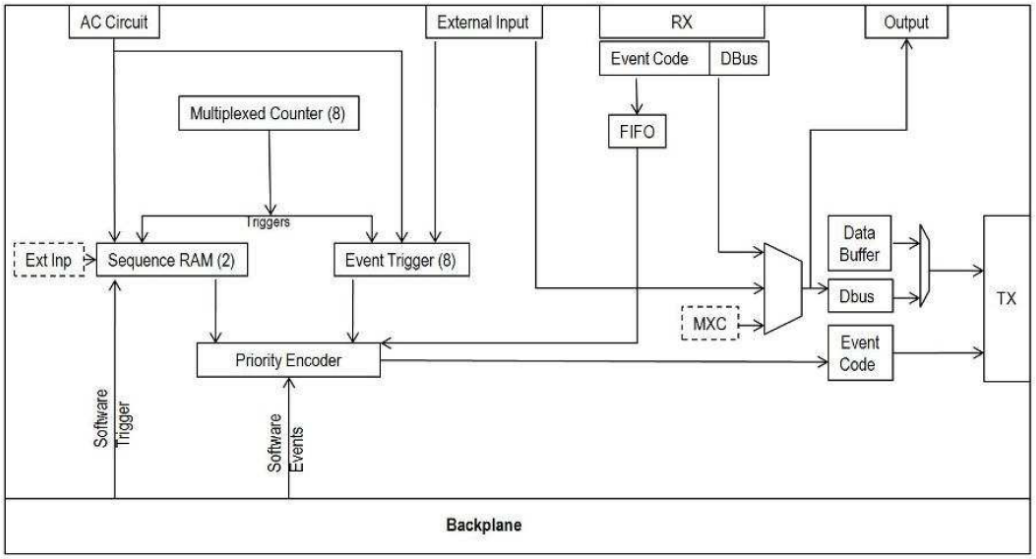


FIGURE 2.7: Sub-components inside the MRF EVG.

### 2.3.4 Event Codes Generation

As Fig. 2.7 shows, 256 event codes originate from several sources are sorted at a priority encoder to avoid the collision. 8 trigger events are sent out on a stimulus from a multiplexed counter, an external TTL level signal, or the AC power line synchronization logic output signal. Two sequence RAMs also provide a method of easily transmitting or playback a set of event codes. We will discuss this part later in Section 2.3.6. Most of the event codes can be defined by the user. However, several special event codes are already occupied by the system. The predefined event codes are list in Table 2.1.

### 2.3.5 Timestamp Synchronization

As shown in Fig. 2.8, the implementation of timestamp synchronization by the MRF hardware consists of a 32-bit seconds register (SecReg) and a 32-bit timestamp register (TsReg). EVG receives the time source either from an external GPS or from a Network Time Protocol (NTP) server. The value of SecReg is changed with 32 special codes

| Code | Meaning |
|---|---|
| 0x00 | Idle, or null, event. Send when nothing happens. |
| 0x70 | Shift 0 into EVR timestamp shift register |
| 0x71 | Shift 1 into EVR timestamp shift register |
| 0x7A | Reset EVR heartbeat timeout counter |
| 0x7B | Reset all EVR dividers. Synchronize global phase |
| 0x7C | Increment EVR timestamp counter (depending on mode) |
| 0x7D | Reset timestamp counter |
| 0x7F | End of sequence (not transmitted). |

TABLE 2.1: Special event codes for MRF EBTS.

(either event "0x70" or event "0x71") sent from the EVG while the TsReg is maintained by each EVR and incremented at an integer divisor of the event clock rate or the special event code "0x7C".

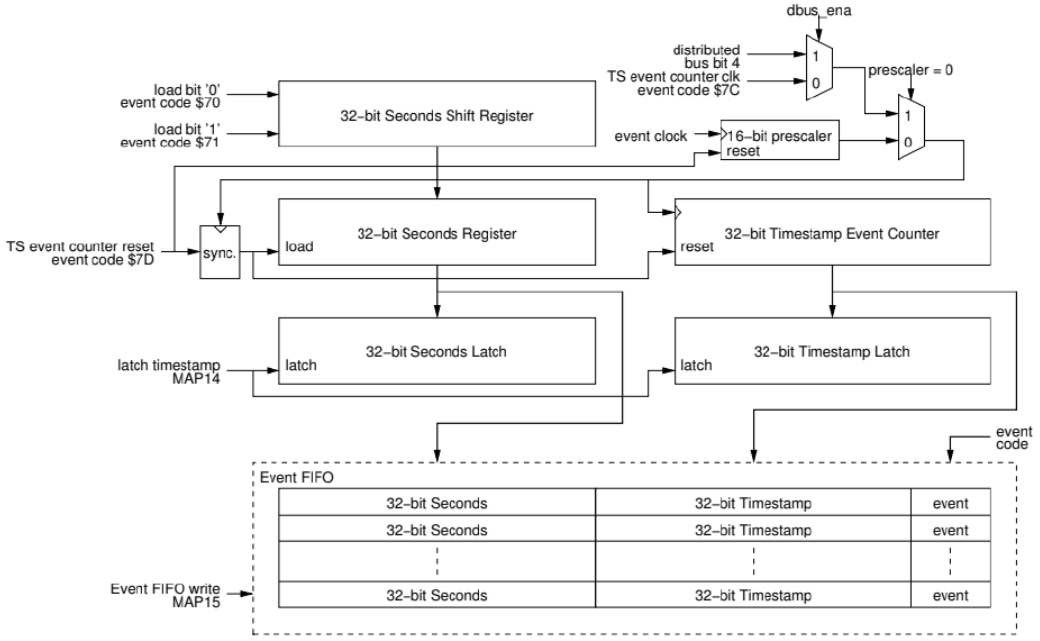


FIGURE 2.8: Timestamp synchronization logic.

Note that the timestamps for receiver modules with a long-distance, e.g., 10 km, may differ in a microsecond scale due to the delay caused by the transmission medium. This problem can be palliated either by newer hardware with a delay compensation function like MRF EVM-300 module or by TBTS (see Section 2.4).

### 2.3.6 Event Sequencer

The sequencer holds up to 2048 pairs of event code and timestamps. The contents of a sequencer can be altered via VME access. The sequencer may be triggered from several sources including external TTL input, software triggering by VME access, AC power line logic, or a multiplexed counter output. When the sequencer is triggered, an internal counter starts on a sequencer clock rate which can be down-converted from the event clock with a prescaler. When the timestamp matches the counter value, the attached event code is sent out.

## 2.4 TBTS

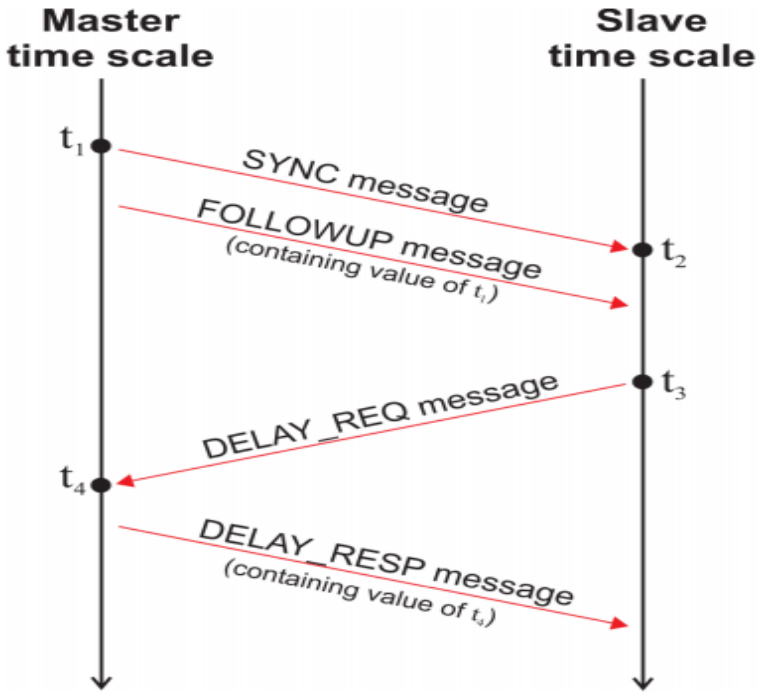


FIGURE 2.9: IEEE 1588 synchronisation mechanism and delay calculation.

Unlike the EBTS that needs an external stimulus to trigger, the TBTS broadcasts an instruction message with an action and correspondent timestamp after a common notion of time is reached through the timing network. The microsecond timing synchronization can be achieved by the Precision Time Protocol (PTP, IEEE1588) [23].

As depicted in Fig. 2.9, to synchronize the timestamp between master and slave, by assuming that the link is symmetric, the delay $\delta$ can be calculated with the time tags $t_1$, $t_2$, $t_3$ and $t_4$ through,

$$\delta = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} \tag{2.7}$$

One example of such implementation is the White Rabbit (WR) project designed by CERN, GSI, and others. Two main technologies are used at WR,

- **Synchronous Ethernet**, all network devices can have the same clock, recovered from the timing master. The clock is encoded in the Ethernet package and recovered by the PLL of the Ethernet physical layer to alleviate the clock skew effect.
- **WR PTP**, the WR PTP detects the phase offset between local clocks and master clock and compensates for the delays introduced by the link.

However, two non-deterministic factors, thermal change of transmission medium and asymmetric link delays limit the WR accuracy of around 1 ns, which is basically at the same scale of EBTS.

## 2.5 Examples of Accelerator Timing system

### 2.5.1 BEPC II

The Beijing Electron Positron Collider II (BEPC II) is a double-ring electron-positron collider with a 202 m long LINAC. It can either serves as a collider or a light source facility with its outer ring for a storage ring [24]. The key timing system parameters of the BEPC II collider mode are shown in Table 2.2.

Since the beam is directly injected into the main ring from LINAC, the RF frequencies of LINAC and MR should match relation of,

$$2856 * 7 = 499.8 * 40 \tag{2.8}$$

| Parameter | Value |
|---|---|
| LINAC RF | 2856 MHz |
| MR RF | 499.8 MHz |
| MR harmonic number | 396 |
| MR circumference | 237.5 m |
| MR revolution frequency | 1.26 MHz |
| Common frequency for LINAC and MR | 71.4 MHz |

TABLE 2.2: Timing system parameters of BEPC II

The greatest common frequency for BEPC II bucket selection is 71.4 MHz which can be obtained through a divide-by-7 divider of MR RF according to Eq. 2.3. However, the frequency divider factor of the old version of the MRF EVG 200 module only supports 4, 5, 6, 8, and 10 [25]. Given this context, $f_{MR-RF}/5$ is first selected as the event clock inside the EVG and then the common frequency of $f_{MR-RF}/35$ for BEPC II BSC is generated through the multiplexed counter component inside the EVG. Though the period for selection of all RF buckets becomes 5 times longer, this period is still acceptable while comparing to the 50 Hz BRR.

### 2.5.2 SLS Timing System

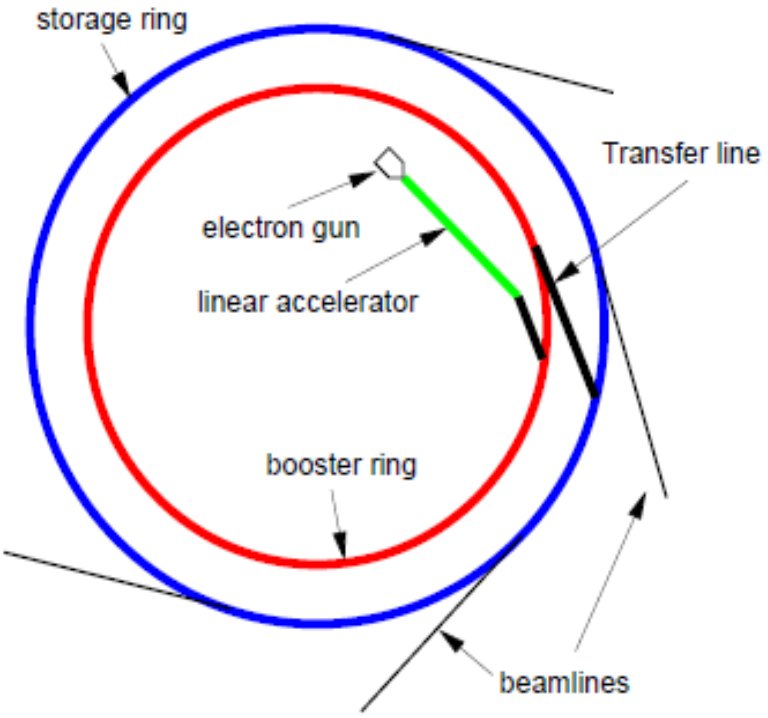


FIGURE 2.10: Layout of SLS.

Like other third-generation light source facilities, the SLS projects consist of an injector LINAC, a Booster, and a storage ring (SR), as Fig. 2.10 shows. The EBTS at SLS is responsible for synchronizing the RF clock and AC power line, distributing event codes, and control the machine operation sequencing. The injection cycle is 320 ms (3.125 Hz) which comes from the synchronization of AC power line (50 Hz) and common frequency [26]. The timing system parameters of the SLS are listed in Table 2.3.

| **Parameter** | **Value** |
|---|---|
| LINAC RF | 2997.6 MHz |
| Booster RF | 499.6 MHz |
| Booster harmonic number | 450 |
| Booster circumference | 270 m |
| Booster revolution frequency | 1.11 MHz |
| SR RF | 499.6 MHz |
| SR harmonic number | 480 |
| SR circumference | 288 m |
| SR revolution frequency | 1.04 MHz |
| Common frequency for booster and SR | 69.44 kHz |

TABLE 2.3: Timing system parameters of the Swiss Light Source.

The RF frequency for SLS LINAC is exactly six times of SR RF frequency at SLS, which means the parameters $m$ and $n$ in Eq. 2.3 are "1" and "6", respectively. Consequently, consideration should only be given into synchronization between Booster and SR. The ratio of Booster harmonic and SR harmonic, i.e., $p/q$ in Eq. 2.5, is 16/15, which means if having had "#0" bucket in alignment, "#0" bucket will be in alignment again every 16 Booster revolution cycles or 15 SR revolution cycles [27]. Thus, the common frequency can be derived according to Eq. 2.6.

Since the Booster revolution frequency is used to trigger the EVG sequence RAM. By moving the event one position later in the sequence RAM, the injection bucket to SR shifts by 30 buckets. That means the "#0" bucket bunch in Booster is injected into "#450" in SR.

# Chapter 3

# Overview of Timing System at KEK LINAC

## 3.1 Hardware and Software

The timing system at KEK LINAC consists of much hardware. Some of them are inherited from the timing system at the KEKB era while some are newly installed to improve the stability and extend the functionality [28, 29]. For example, the event generator module (VME-EVG-230) and event receiver module (VME-EVR-230RF) produced by MRF company still serves as the core timing system part during the past ten years. On the other hand, several new modules, such as time-to-digital converter (TDC), reflective memory (RFM), and master trigger generator (MTG), are introduced to meet new requirements for SuperKEKB as well as extending the system functionality.

A schematic view of the event timing system currently used at LINAC is shown in Fig. 3.1. The timing station which generates the master trigger event signal is called Main Timing Station (MTS). Three MRF-VME-EVG230 modules and an MVME6100 CPU module are installed at MTS [30]. The main timing station delivers events to 20 local EVR stations at KEK LINAC. Besides MTS, many sub-timing stations with

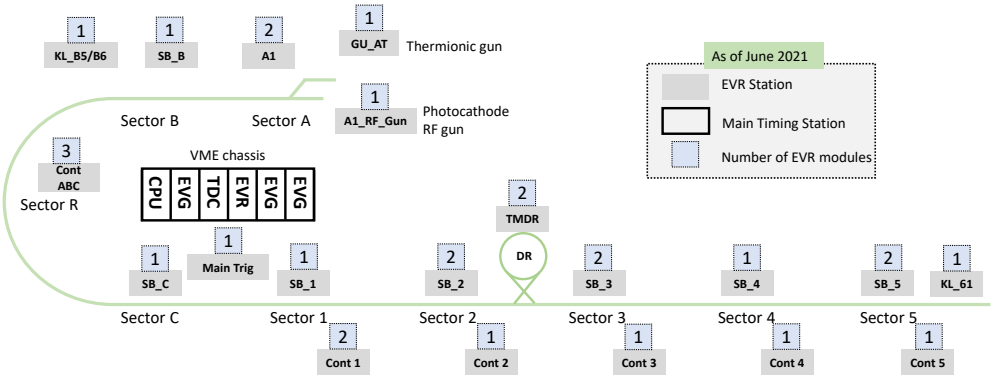


FIGURE 3.1: Layout of timing stations at LINAC [2].

EVRs mounted in the VME64x subrack are connected to the EVG with fiber-optic links in a star-like topology. The EVR can receive an event stream from the EVG at a speed of 57.12 MB/s. There are six local EVR stations installed at sub-control rooms, eight stations located at sub-booster stations, and other local timing stations, which are distributed along the LINAC beamline. Two of the most important sub-timing stations are the MR Sub-timing Station (MR-STS) and DR Sub-timing Station (DR-STS).

EPICS is selected as the control system framework of KEK LINAC, and the timing system modules also integrate with the EPICS environment through some device support and driver support libraries. In addition, the event stream of 8b/10b encoding can also be decoded by user-defined field-programmable gate array (FPGA) board [31]. The RF monitor system is a good illustration of event stream recognition, which integrates the EVR function inside the Virtex-6 FPGA to acquire the beam mode, RF phase, and other necessary data are sent from EVG.

### 3.1.1 Event Modules

As Fig. 3.2 show, MTS IOC consists of three VME-EVG-230 modules, one TDC module, one VME-EVR-230RF module and one RFM module [2, 32–34]. These modules, which are in a VME64x subrack with MVME6100 CPU, collaborate to generate synchronized timing signals from 50 Hz AC power line (AC50) and BSC. Then, these signals are distributed to event receiver stations. The receiver station is composed of an MVME5500 CPU, because of the relatively relaxed CPU load, VME-EVR-230RF module, and several I/O modules [35]. MTS IOC uses VxWorks 6.8.3 as a real-time operating system and runs EPICS version 3.14.12.

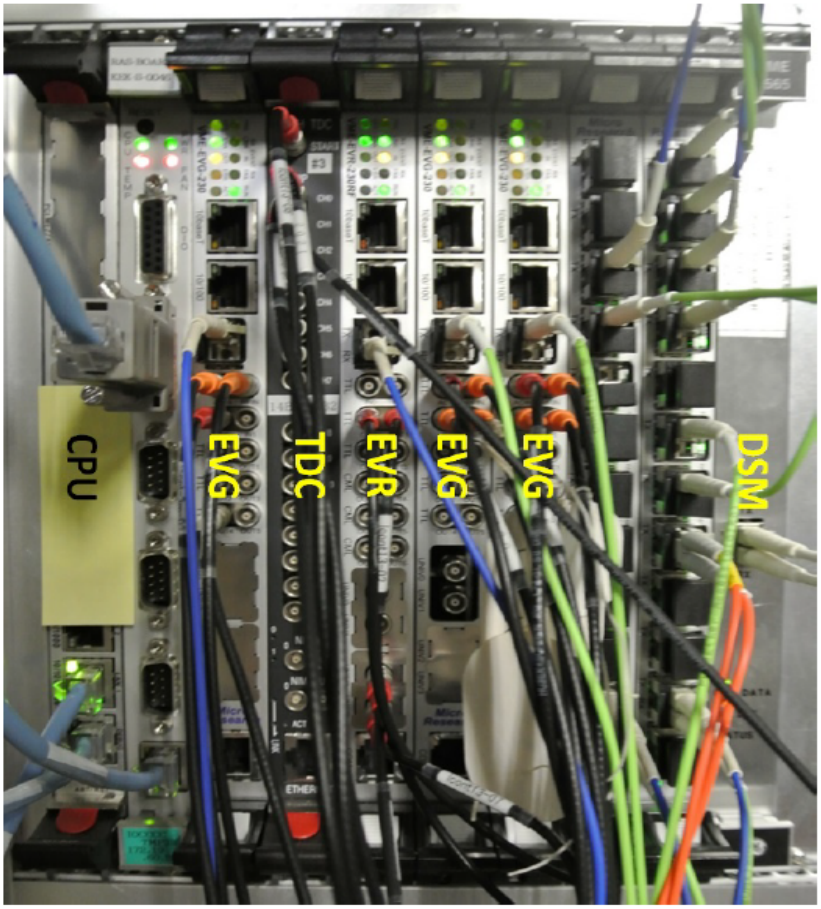


FIGURE 3.2: Event modules installed at MTS.

Besides the MRF event modules, Shanghai Institute of Applied Physics (SINAP) event modules are also used. The specifications of MRF event modules and SINAP event modules are summarized in Table 3.1. The trigger signals for MR BPMs are required to synchronize with the MR revolution frequency which cannot be acquired directly from MTS. Consequently, an extra module is necessary to supply the trigger signal. SINAP event modules mainly include VME-EVO and VME-EVE. The VME-EVO can be configured as EVG, EVR, or FANOUT by software while VME-EVE could only be used as EVR [36]. The VME-EVO module is compatible with the MRF module and provides the functionality to synchronize with another RF input. Thus, with the help of SINAP modules, it is convenient to both receive the data from MRF-EVG and supply MR-synchronized signals for BPMs. The connection between MRF modules and SINAP modules is shown in Fig. 3.3. MRF-VME-EVG located at MTS sends event codes to both MRF-VME-EVR and SINAP-VME-EVO. SINAP-VME-EVO also receives the input of MR RF frequency and sends event codes to SINAP-VME-EVE [37, 38]. Therefore, all outputs from SINAP-VME-EVE are synchronized with the MR RF clock with a jitter

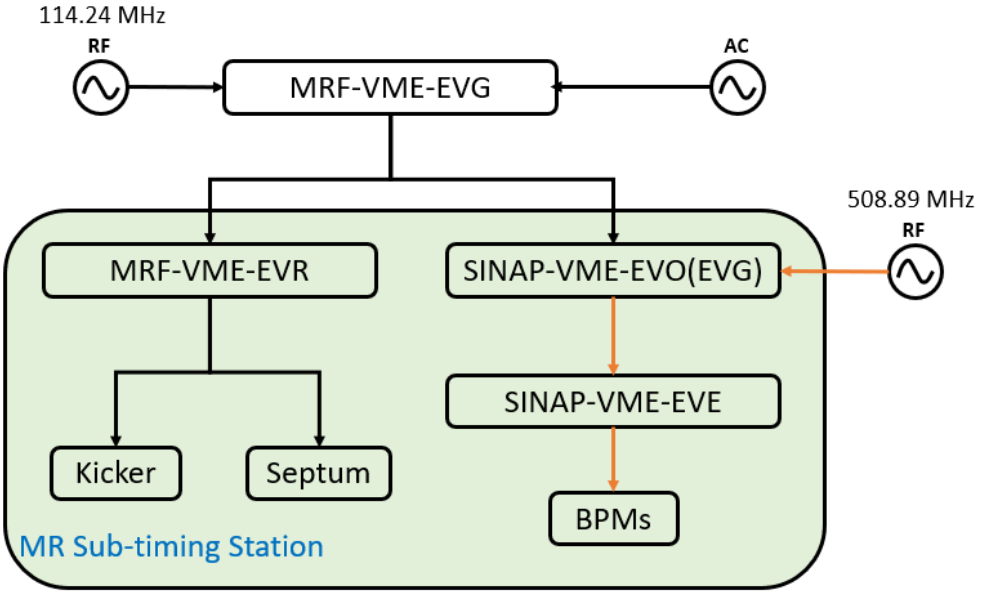


FIGURE 3.3: Schematic view of MR Sub-timing Station.

of about 10 ps.

| | **MRF** | | **SINAP** | |
|---|---|---|---|---|
| | EVG-230 | EVR-230RF | EVO | EVE |
| Event Clock | 114.24 MHz | | 99.39 kHz | |
| Trigger | AC | Up-link event | Up-link event | Up-link event |
| Resolution | Event Clock | Event Clock/40 | Event Clock | Event Clock/20 |
| Jitter | - | ∼30 ps | - | ∼10 ps |

TABLE 3.1: Specifications of MRF and SINAP VME event modules used for MR-STS.

An EPICS driver for VME and PCI cards from MRF for event timing systems called mrfioc2 is used to integrate the device control with EPICS environment [39]. For SINAP devices, a dedicated EPICS driver is also developed. Consequently, the timing adjustment can be controlled based on EPICS. Two standard "waveform" records are used to manage event codes and correspondent delays. The value of these records is loaded into the sequencer RAM of EVG and delivered to EVRs. The timing system control logic, such as the beam mode switch, is also implemented inside the MTS IOC through EPICS records.

### 3.1.2 MTG

The MTG module is responsible for generating a master trigger signal at the same phase of the AC power line to keep the stability of some power-sensibility devices, such

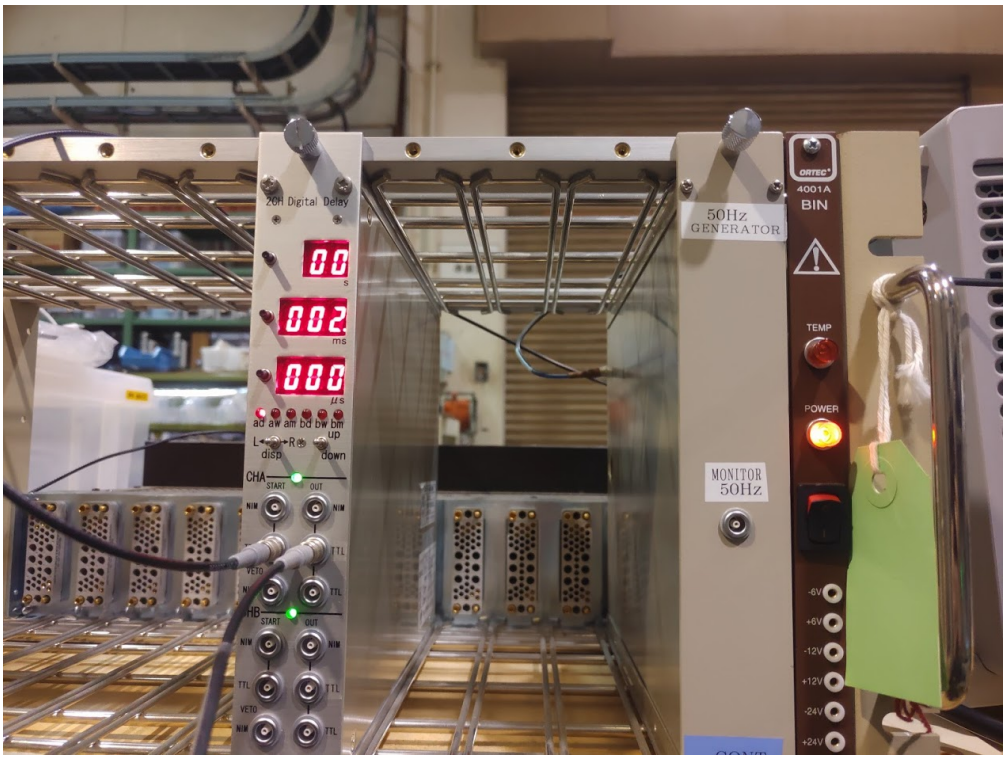


FIGURE 3.4: MTG module (right) in a NIM crate.

as pulsed magnets for MR injection. The AC power used at KEK LINAC is provided by Tokyo Electric Power Company. This commercial frequency will fluctuate at around 50±0.2 Hz.

The implementation logic of the MTG module is intuitive. Basic circuits of the MTG module consist of an AC-DC converter, a voltage comparator, and a monostable multivibrator to generate the 50 Hz TTL type output signal. Fig. 3.4 shows the MTG module installed in the NIM crate.

### 3.1.3 TDC

To quantify the time duration of several trigger signals, a 16-channel FPGA-based TDC has been developed on a Xilinx Spartan-6 FPGA equipped on a VME board with a resolution of 1 ns [2]. The TDC module developed at KEK LINAC is shown in Fig. 3.5. It serves as the major hardware to measure the AC50 arrival time, which is crucial since LINAC needs to operate on the same phase of AC50. It can also be used for measuring the output from EVR. Since the event clock resolution is 8.75 ns, a resolution of 1 ns and

a dynamic range greater than 20 ms are required for the time-duration measurements in the TDC.

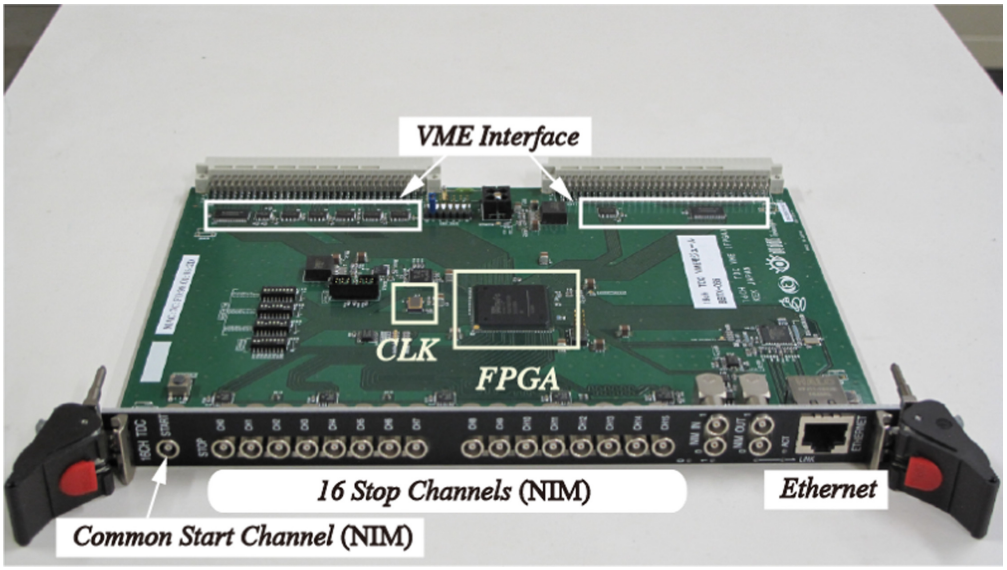


FIGURE 3.5: TDC module.

The VME-based TDC has a common start channel and 16 stop channels. The input signal is based on a Nuclear Instrumentation Module (NIM) standard with a 50-Ω input impedance [40]. The reference signal is fed into the common start channel, and the delayed trigger pulses are fed into the stop channels. Thus, the time duration between the start channel and stop channel can be measured with 32-bit counters with a resolution of 1 ns. Therefore, the maximal measurement range is 4.3 s. The accuracies of the time-duration measurements are less than 1 ns and 2.6 ns within dynamic ranges of 7.5 ms and 20 ms, respectively [2]. Every channel supports the multi-stop function which provides the ability to measure delay timings of up to 4 successive trigger pulses. This is an important specification required for the two-bunch operation mode at LINAC, in which the time duration between two bunches is exactly 96.3 ns. The 1000Base-T Ethernet connection also enables fault diagnosis and data acquisition for the TDC without the interfere of VME CPUs.

The EPICS driver of the TDC module is developed to read the content of the buffer data in the FPGA via an A32/D32 VME64x interface. The measured data is saved in an EPICS "waveform" record with 64 elements and can be accessed remotely through the EPICS CA protocol.

### 3.1.4 RFM

The reflective memory (RFM) module (Also known as "Shared Memory") is a real-time fiber-optic network product that is mainly used to share data regardless of architectures and operating systems. The VME-5565 module provides a method of fast communication among VME computers. The data stored in the local RFM will be automatically broadcasted over a 2 Giga Baud high-speed and low latency link to other RFM nodes, and this process is software transparent. The RFM network supports up to 256 nodes and connection distance can reach up to 300 m with multimode fiber and up to 10 km with single-mode fiber, respectively. The dynamic packet size, 4 to 64 bytes of data, achieves a network transfer rate of 43 Mbytes/s to 170 Mbytes/s [34].

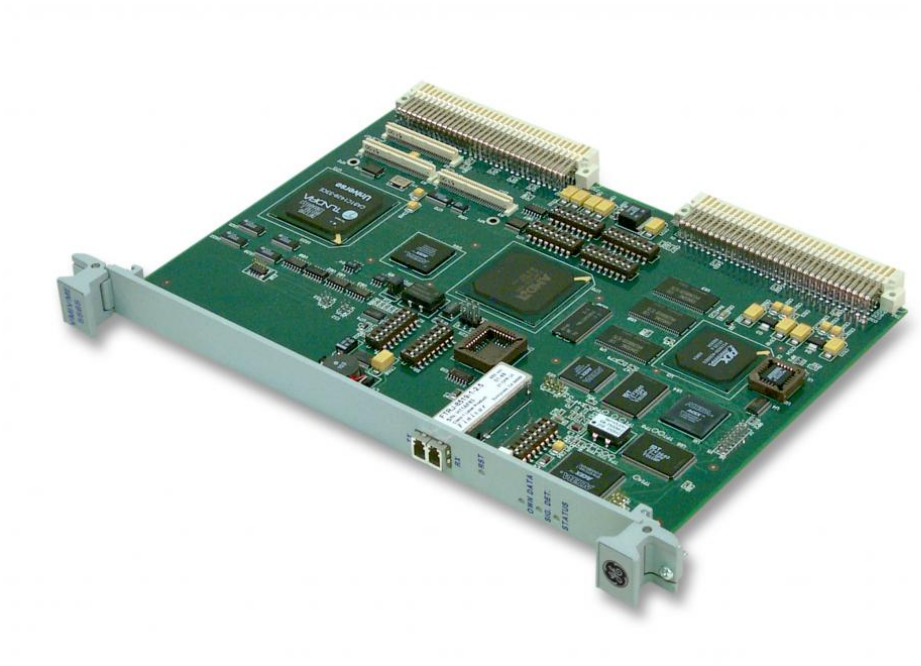

FIGURE 3.6: Reflective memory module (VME-5565).

Another useful functionality is network interruption transmission. Four general-purpose network interrupts with 32 bits of data each can be directed to a specific node or broadcast globally to all nodes on the network. Any of the four possible network interrupts can also generate a host VMEbus interrupt at each receiving node.

Two kinds of network topology are supported for the RFM module. By simply connecting every module as a ring, it is easy to construct a light-weighted network that avoids the complexities of queuing and checking data packets. On the other hand, with the help of a fiber-optic hub, a star topology enhances the network availability and system robustness

since the network will continue to operate even if one module fails. The ACC-5595 RFM hub has 8 ports, and each port regenerates the serial optical signal, eliminating cable attenuation problems as well as reducing jitter [41].


FIGURE 3.7: ACC-5595 Reflective Memory Hub.

The RFM 5565 module and ACC-5595 RFM hub used at SuperKEKB bucket selection system are shown in Fig. 3.6 and Fig. 3.7.

## 3.2 RF Synchronization at LINAC

Fig. 3.8 shows the RF frequency synchronization of the LINAC timing system which equips several frequency multipliers/dividers and phase shifters. "Rev" indicates the revolution frequency, "BS" indicates the bucket selection, "E/O" indicates the electrical/optical converter and vice-versa, and "Acc." indicates the accelerator structure. The LINAC master oscillator (LINAC-MO) is synchronized to the MR master oscillator (MR-MO) and DR master oscillator (DR-MO) by the external 10 MHz references generated by a frequency division of the 510 MHz main oscillators (MMO). LINAC-MO, DR-MO, and MR-MO belong to the commercial Agilent E8663 series [42]. The phase drift caused by the long-distance transmission is compensated by phase monitoring and direct sampling technique [43]. The slow drift of the beam energy caused by phase drift is suppressed.

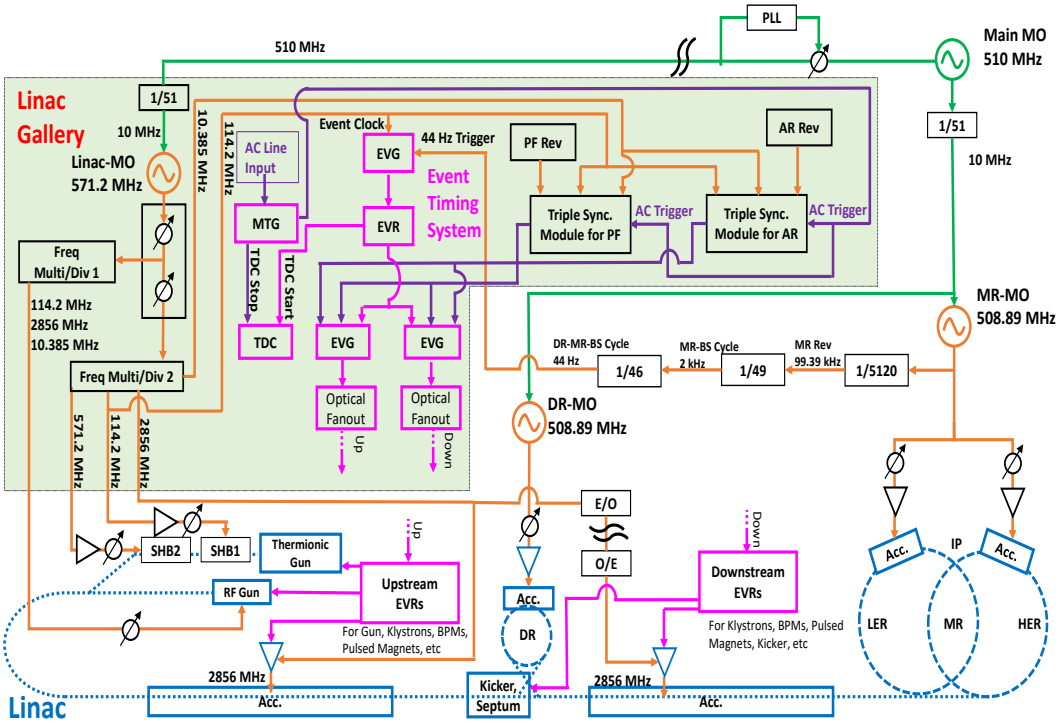


FIGURE 3.8: Block diagram of synchronization system for LINAC, DR, and MR.

The fundamental frequency between LINAC-MO and MR-MO is 10.385 MHz, which means 55 cycles of LINAC-MO covers exactly 49 cycles of MR-MO. For laser oscillation of the RF gun, a supply of 10.38 MHz, 114.24 MHz, and 2856 MHz are required from the main drive system. The 11th harmonic (114.24 MHz) and 55th harmonic (571.2 MHz) of the fundamental frequency are used to drive two subharmonic bunchers (SHBs) immediately after the electron gun [44]. The 2856 MHz RF field is used to drive the accelerator structures. Both DR and MR use 508.89 MHz as the ring RF frequency. The integer relation of RF frequencies is shown in Table 3.2.

| Frequency | Ratio | Purpose |
|---|---|---|
| 10.385 MHz | - | RF Gun |
| 114.24 MHz | ×11 | LINAC SHB1 & RF Gun |
| 571.2 MHz | ×55 | LINAC SHB2 |
| 2856 MHz | ×275 | LINAC Main RF & RF Gun |
| 508.89 MHz | ×49 | DR & MR RF |

TABLE 3.2: Integer relation of RF frequencies at KEK LINAC

However, the PF and the PF-AR are not synchronized to LINAC because the two accelerators use independent RFs. Thus, the chance coincidence of LINAC RF (114.24 MHz and 10.385 MHz) and PF/PF-AR RF revolution frequency is utilized through the

triple sync module (shown in Fig. 3.8). The output of the triple sync module is used as the main trigger of PF/PF-AR injection timing [45].

## 3.3 Bucket Selection for SuperKEKB

### 3.3.1 Delay Calculation of RF Buckets

RF frequencies are also used for driving the timing system at KEK LINAC. The timing system uses 114.24 MHz as the event clock to deliver the event codes, and the beam repetition rate (BRR) is 50 Hz. The harmonic number for DR and MR is 230 and 5120, respectively. Note that there only exists a positron DR, the synchronization between LINAC and HER is simple. The bucket selection cycle (BSC) for LINAC and HER $f_{LI-HER-BS}$ can be easily derived as 2.03 kHz based on Eq. 2.4. Thus, we will mainly focus on the BSC of LER. According to Section 2.1, several significant frequencies for timing system can be calculated in Table 3.3. Note that the BSC for DR only is practically useful when performing DR-injection-only mode for beam study.

| **Frequency** | **Period** | **Remarks** |
|---|---|---|
| 2856 MHz | 350 ps | RF frequency for LINAC |
| 508.89 MHz | 1.97 ns | RF frequency for DR & LER |
| 114.24 MHz | 8.75 ns | Event clock |
| 2.21 MHz | 452 ns | DR revolution frequency |
| 99.39 kHz | 10.06 $\mu$s | LER revolution frequency |
| 45.15 kHz | 22.15 $\mu$s | BSC for DR only |
| 2.03 kHz | 493 $\mu$s | BSC for LER only |
| 88.19 Hz | 11.34 ms | BSC for DR and LER |
| 50 Hz | 20 ms | BRR |

TABLE 3.3: Bucket selection frequencies at KEK LINAC

The integer relation between LINAC RF and LER RF is 275/49. Thus, the positron beam injection opportunity appears either every 49 ticks of 508.89 MHz or every 275 ticks of 2856 MHz. Furthermore, after waiting for 49 ticks of LER revolution frequency, the same LER RF bucket can be injected again. Similarly, the ratio of DR harmonic number and LER harmonic number is 23/512 which means the same combination of DR RF bucket and LER RF bucket can be selected every 512 cycles of DR or 23 cycles of LER. Concerning the LINAC synchronization, the overall BSC becomes 88.19 Hz as shown in Fig. 3.9.

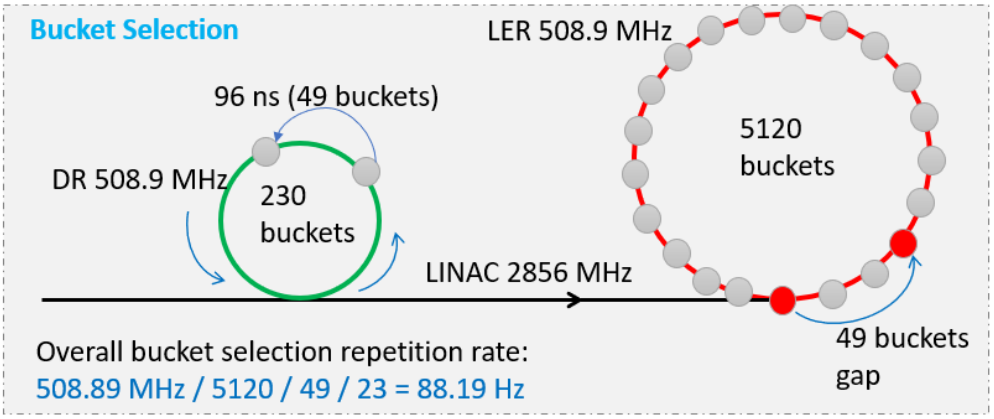


FIGURE 3.9: Bucket selection for DR and LER.

The relation between injection delay and bucket number in LER and DR can be described as following,

$$N_{LER} = MOD\left(\frac{T_{delay} * 49}{96.3}, 5120\right) \tag{3.1}$$

$$N_{DR} = MOD\left(\frac{T_{delay} * 49}{96.3}, 230\right) \tag{3.2}$$

where $N_{LER}$ and $N_{DR}$ represent the bucket number in LER and DR, respectively. Table 3.4 also shows the relation between injection opportunity and bucket number. The calculation is based on Eq. 3.1 and Eq. 3.2. After 11.34 ms, both DR RF bucket "#0" and LER RF bucket "#0" can be filled again. By adding a proper delay value (must be an integer multiplication of 96.3 ns) based on BSC, arbitrary LER RF buckets can be filled. Note that the BSC of 22.68 ms (i.e., 44 Hz) is used because we want to decrease the interrupt handling times and simplify the system.

Figure 3.10 shows the simplified procedure of delay calculation for DR and LER. First, the bucket number for LER is designated (for example, bucket "#49" will be filled), and then the delay value $T_{delay2}$ for LER can be acquired by Eq. 3.1. Since $T_{delay2}$ also represents the DR extraction timing, thus, the DR bucket number is obtained. The delay value for DR injection is periodic based on Eq. 3.1 and the $T_{delay1}$ is selected because of the DR storage time limit. The detailed calculation process can be referred to in [46].

In practice, the calculation of bucket selection delay for LER is tougher because the DR storage time should be taken into consideration. The minimal damping time is determined to be 40 ms, which is longer than 20 ms, owing to the requirement of position

| Injection opportunity | Delay | DR Bucket | MR Bucket |
|---|---|---|---|
| 0 | 0 ns | 0 | 0 |
| 1 | 96.3 ns | 49 | 49 |
| 2 | 192.6 ns | 98 | 98 |
| 3 | 288.9 ns | 147 | 147 |
| .. | .. | .. | .. |
| 230 | 22.1 $\mu$s | 0 | 1030 |
| .. | .. | .. | .. |
| 5120 | 493 $\mu$s | 180 | 0 |
| .. | .. | .. | .. |
| 20771 | 1.99 ms | 29 | 4019 |
| 20772 | 2 ms | 78 | 4068 |
| .. | .. | .. | .. |
| 117760 | 11.34 ms | 0 | 0 |

TABLE 3.4: The relation between injection opportunity and bucket number.

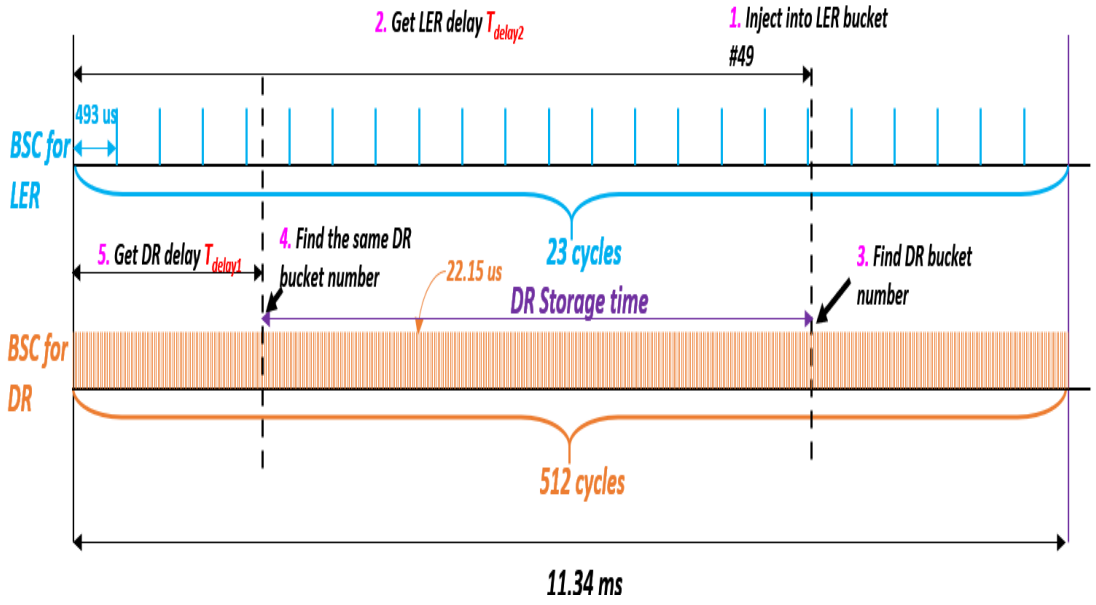


FIGURE 3.10: Delay calculation for DR and LER.

emittance. As a result, the injection and extraction of DR are separated into two pulses and should be controlled by two EVGs. Thus, the LINAC is virtually divided into two parts, which include the "Upstream LINAC" and "Downstream LINAC". Apart from the basic accelerator devices at LINAC, such as klystrons and BPMs, the major difference of controlled hardware between "Upstream LINAC" and "Downstream LINAC" is that the "Upstream LINAC" includes the electron gun and injection magnets at DR, the "Downstream LINAC" includes the extraction magnets at DR and injection magnets of MR. In other words, the former is responsible for DR injection with the "Upstream EVG" while the latter controls the DR extraction and MR injection through "Downstream

EVG". We will fully discuss this part in Section 4.3.

### 3.3.2 Decision Making of Injection Bucket

Several factors are known to play a role in determining which RF bucket should be filled. For example, continuous injection into the same RF bucket or adjacent RF buckets should be avoided. If the same RF bucket is selected, the bunch stored in that RF bucket is repeatedly kicked in 50 Hz. As a result, there is not enough time to damp the bunch by the transverse radiation damping effect. The coupled bunch instability, heating of the beam pipes, and degradation of the vacuum caused by high beam current would also raise the difficulty of short spacing RF buckets selection [47].

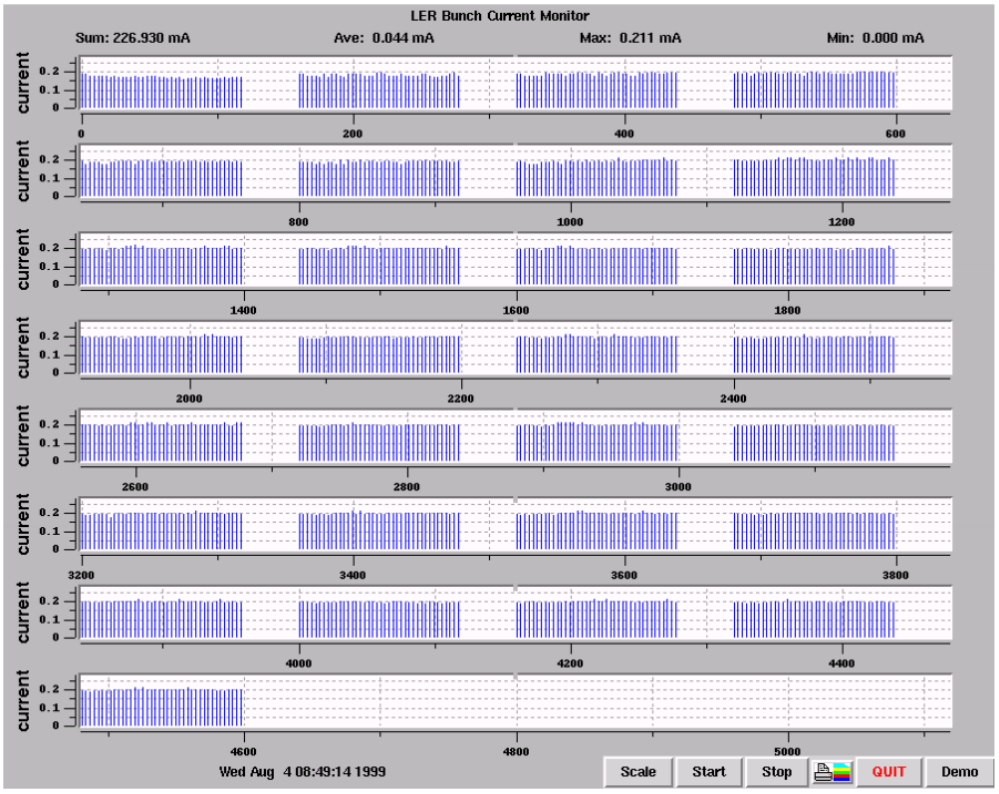


FIGURE 3.11: An example of fill pattern in LER during KEKB era.

Also, the transverse coupled-bunch instabilities caused by the fast-ion instability can be alleviated through the multi-trains filling. When a train of electrons passes a point in the ring, each bunch ionizes the residual-gas [48, 49]. These ions are accumulated as trailing bunches pass the point and cleared out during the training gap. Consequently, a fill pattern is necessary to carefully determine the multi-trains filling scheme. The fill pattern decides,

- the number of the trains
- the number of bunches per train
- the bunch spacing

As Fig. 3.11 shows, bunches in HER are divided into 32-trains, 40 bunches per train, and 6 ns bunch spacing.

To cure the instabilities, the bunch-by-bunch feedback system is also developed to kick the beam and damp the oscillation [50, 51]. The feedback system achieved a satisfactory effect in the SuperKEKB era and normally 2-trains filling is used (Fig. 3.12). The gaps shown in Fig. 3.12 comes from the abort system. The beam abort system is constructed at SuperKEKB to protect the accelerator components, Belle II detector, as well as ensuring the radiation safety [52]. A fast response is required to quickly deliver the stored beam into a beam dump and prevent spewing the beam everywhere in the ring. Because of this, the stored bunches are separated into several trains to reserve adequate bunch spacing as the abort gap. The beam abort gap is designed to be less than 200 ns (around 100 RF buckets). The requirement comes from the luminosity degradation due to beam-loading effects as well as the requirement for the stable operation of RF cavities.

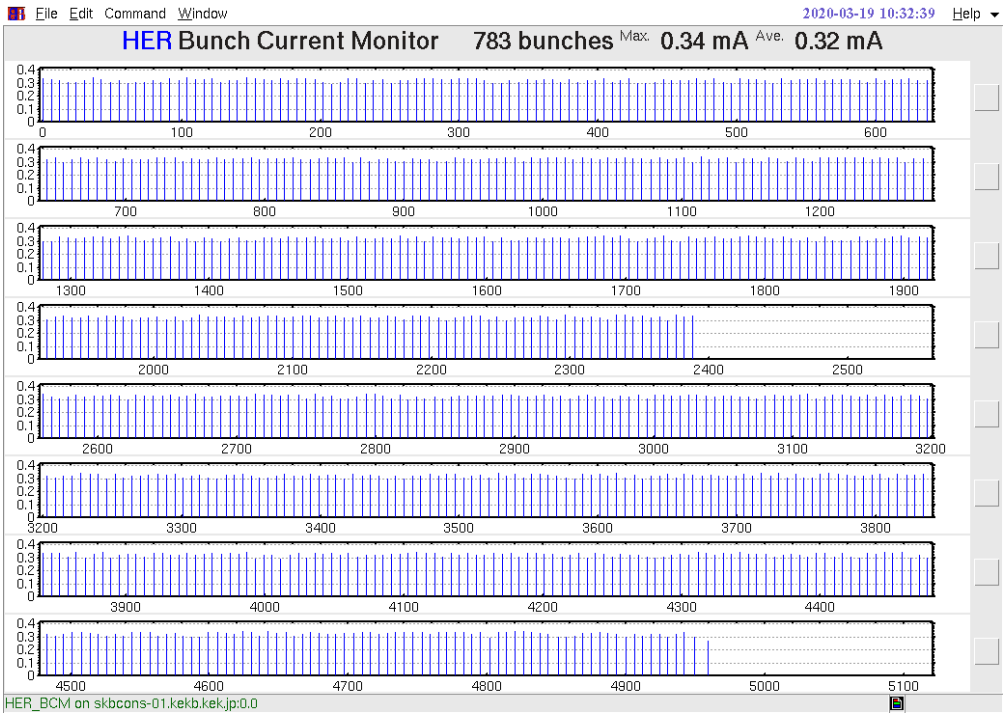


FIGURE 3.12: Fill pattern during SuperKEKB era for HER.

The bunch currents inside the RF buckets become different since the beam lifetime varies with the position of the stored RF bucket. The lowest bunch current bucket should be selected for injecting to save the beam and increase the luminosity. This function is called "Bunch Current Equalizer (BCE)". The bunch-by-bunch current monitor, as a by-product of the bunch-by-bunch feedback system, provides the beam current data of every stored RF bucket with an 8-bit ADC. The implementation of beam current monitor is described in [51]. However, "BCE" is restricted when "2-bunch" mode is selection, i.e., , two bunches are formed every injection pulse with a 96.3 ns bunch spacing. Therefore, other than the fill mode of "BCE", a fill mode of "star" type is supported for the "2-bunch" operation. The fill mode of "star" needs to memorize the previously filled RF bucket and selects the RF bucket with a proper distance to the last filled bucket. The bucket spacing is carefully chosen to obey the fill pattern rule. By performing the "2-bunch" injection of "star" mode first and single bunch "BCE" mode later, the bunch current in the stored RF buckets can be equalized. An illustration of "star" fill mode is shown in Fig. 3.13.

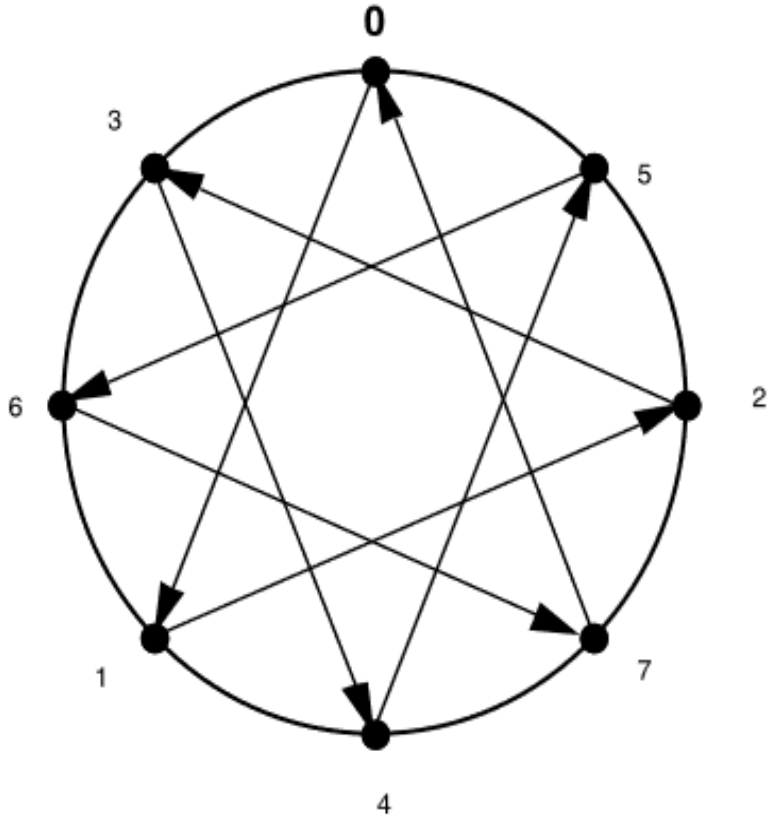


FIGURE 3.13: Bucket selection fill mode of "star" type.

Consequently, the decision on which bucket should be filled is done based on the following information:

1. fill pattern,
2. fill mode and associated parameters,
3. bunch current information of each RF bucket,
4. number of bunches,
5. the bucket address last filled.

### 3.3.3 Constituents of Bucket Selection System

The bucket selection system currently used for SuperKEKB is inherited from the KEKB bucket selection system, which started in 1998 [53]. Although the hardware and software evolved a lot, the fundamentals of the bucket selection system remained as a triangle structure as shown in Fig. 3.14. The MTS node located at LINAC first generates an interrupt to Central Control Building (CCB) node. The CCB node decides the RF bucket which would be injected based on either "BCE" fill mode or "star" fill mode. The bunch currents for the RF buckets measured by Bunch Current Monitor (BCM) node are required if the "BCE" fill mode is selected. The delay value of that RF bucket is subsequently calculated at CCB and is transferred to the MTS node to finish the bucket selection process [54, 55].

All these nodes equipped the RFM module which connects through a dedicated fiber-based communication network. The RFM network topology can be selected for either a ring topology or star topology. Through the fiber-optic HUB-5595 module, a star topology RFM network is configured to increase the robustness of the bucket selection system at SuperKEKB. The RFM network will continue to operate even if one RFM node is power cycled. This is extremely helpful because, in principle, an extra RFM monitoring node to diagnose the bucket selection program can be commissioned without affecting the beam operation.

Besides the high-speed data-sharing of the RFM module, the network interrupts delivering function is utilized to implement the control logic. After finishing the bucket

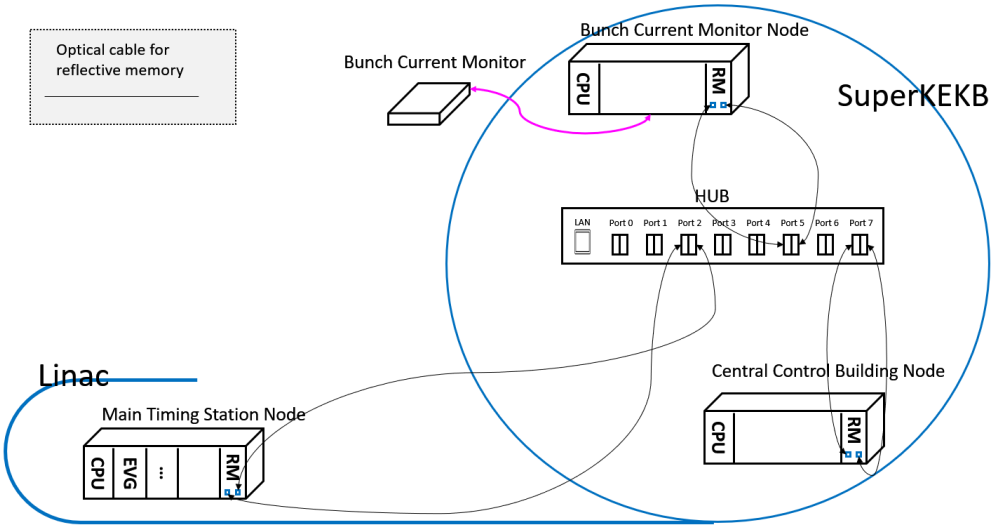


FIGURE 3.14: Bucket selection system with three functional nodes and one monitor node.

selection delay calculation, the CCB can send an interrupt to the MTS and the RFM module at the MTS can generate the VME interrupt to start the injection control process after receiving the network packets.

## 3.4 Beam Gate Control

The beam gate system, which integrates with the timing system, extends the flexibility of a stable injection to the SuperKEKB because it provides the ability to disable the trigger of some crucial hardware without needing to stop the timing signal [56]. There are occasions when the beam delivery should be prohibited or some devices should avoid blank firing to save the hardware lifetime. Thus, the "scheduled pause" or "immediate close" operation should be provided [38, 57]. For example, the "scheduled pause" option for electron gun is demanded during the injection pattern switch process since the preparation event timing signal is wrongly sent out to the newly-set injection pattern and the erroneous trigger should be canceled by masking with "beam gate close" signal. A detailed description of this situation is introduced in Section 4.1. The "immediate close" is required for the beam abort system when some emergent circumstances happen, such as earthquake or beam loss.

The DBus feature of the event module is utilized to deliver the beam gate signal. The DBus accepts 8 TTL inputs that are then converted into one-byte data and transferred

| **Target** | **DBus bit** |
|---|---|
| LER Gun | None |
| DR Injection Kicker | Upstream EVG DBus bit4 |
| DR Injection Septum | Upstream EVG DBus bit5 |
| DR Extraction Kicker | Downstream EVG DBus bit4 |
| DR Extraction Septum | Downstream EVG DBus bit5 |
| LER Injection Hardware | Downstream EVG DBus bit1 |
| HER Gun | None |
| HER Injection Hardware | Downstream EVG DBus bit3 |

TABLE 3.5: Summary of beam gate signals.

through an event link with the speed of 57 MHz, i.e., half of the event clock. The actual trigger generation at local EVRs depends on the event code receiving as well as the status of specific DBus bit through the "AND" logic gate. The "AND" circuit assures that the pulse is sent to hardware only if the beam gate is "open".

The beam gate scheme is advantageous to the DR operation. We have mentioned that two EVGs are used to perform the DR injection and extraction. Consequently, two EVGs deliver different beam gate statuses with their DBus circuit. The DBus bit information is shown in Table 3.5. The beam gate system is also well-integrated with EPICS through a dedicated "bgate" EPICS record. The "bgate" record receives the beam gate status from Belle II and SuperKEKB.

# Chapter 4

# Requirement of Timing System at KEK LINAC

## 4.1 PPM

The fundamental features of the timing system which include the RF synchronization and bucket selection have been discussed in Chapter 3. However, there exist several special requirements for the timing system at KEK LINAC. One of these requirements comes from the pulse-to-pulse modulation (PPM) process.

Several concepts should be clarified before discussing the PPM. As Fig. 4.1 shows, every pulse includes several event codes for controlling the RF gun, the kicker or septum magnet, klystron, and preparation event code for the beam mode of the next pulse. A fixed-length beam mode that is written into the EVG sequence RAM is defined as an injection sequence which is significant for the implementation of sequence shift. For example, a 4 pulses sequence and a 2 pulses sequence are shown in Fig. 4.1. Whereas the sequence only includes part of the beam modes, all beam modes consist of a basic operation repetition unit called an injection pattern. The injection pattern can be separated into several sequences to increase the flexibility of the EVG setting. The

injection pattern plays back continuously until an operator, or an automatic injection program changes the pattern.

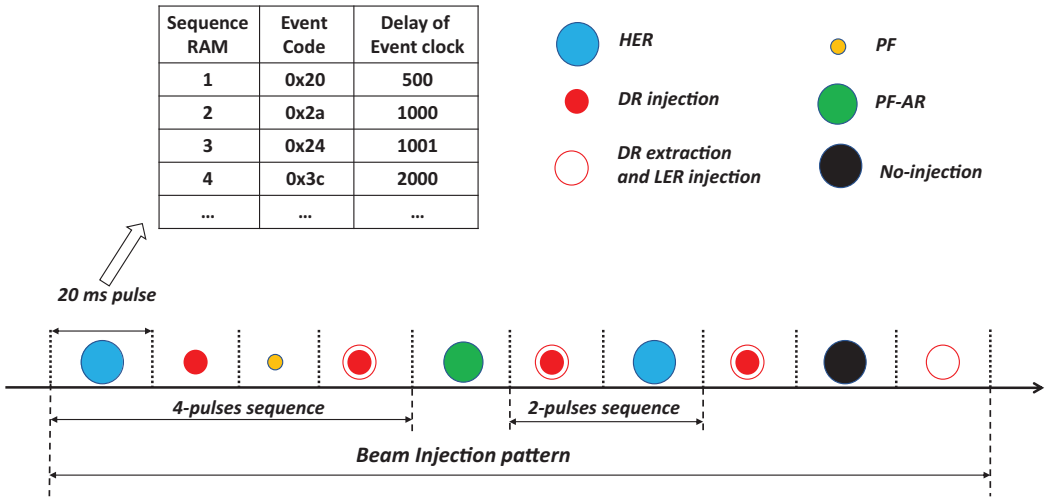


FIGURE 4.1: Injection pattern, sequence, beam mode, and event codes.

### 4.1.1 Simultaneous Injection

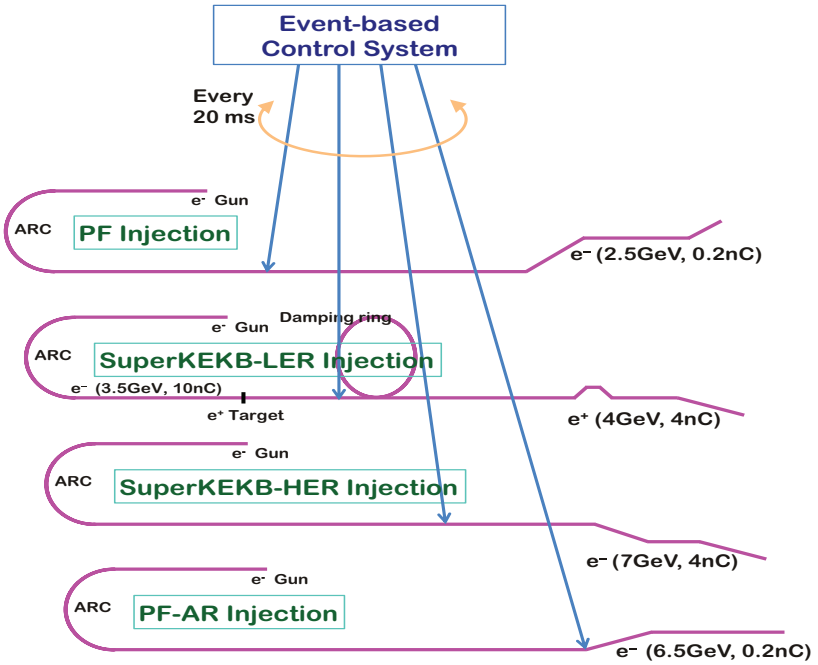


FIGURE 4.2: PPM operation for 4 (+1) rings at LINAC [3].

The event timing system is required to perform the simultaneous injection to several rings. The event codes and their relative delays are basically fixed for accelerators with a single kind of beam mode. However, it is significant at multi-accelerator facilities, such

as KEK LINAC, to switch the beam mode quickly because different beam modes are used. The accelerator devices need to be capable of pulsed operation while the trigger signals and control parameters derived from the timing system should change accordingly based on the beam repetition rate (BRR). The 50 Hz PPM successfully shares the LINAC between 4 destination rings (PF, PF-AR, and SuperKEKB HER/LER) and an intermediate DR for LER with quite different energies and bunch charges (See Fig. 4.2). The beam properties of 4 (+1) target rings of LINAC is shown in Table 4.1. By changing hundreds of parameters through PPM, the simultaneous top-up injection to 4 rings is accomplished to contribute to the physics experiment. The PPM at LINAC is achieved through the event-based control system which manages the injection pattern, generates different event codes for different beam modes, and supplies trigger signals to accelerator components with specific delays.

| **Direction** | **Particle** | **Energy (GeV)** | **Charge (nC)** | **# of bunches** |
|---|---|---|---|---|
| SuperKEKB-LER | $e^+$ | 4.0 | 4.0 | 2 |
| SuperKEKB-DR | $e^+$ | 1.1 | 4.0 | 2 |
| SuperKEKB-HER | $e^-$ | 7.0 | 4.0 | 2 |
| PF | $e^-$ | 2.5 | 0.2 | 1 |
| PF-AR | $e^-$ | 6.5 | 0.2 | 1 |

TABLE 4.1: Beam properties of 5 rings.

### 4.1.2 Beam Mode and Injection Pattern

The PPM is conducted every pulse which represents different kinds of beam modes. At LINAC, a total of 12 beam modes are defined which include 5 beam modes for normal beam operation, 5 beam modes for corresponding beam study, one beam mode for "no injection mode (NIM)" and one for "no trigger mode (NTM)". The beam modes defined at LINAC are shown in Table 4.2. The KBE and KBP mode is the most frequently used beam modes for electron beam and positron beam, respectively. Both NIM and NTM mode prohibits the beam generation from the particle source and provides trigger signals for the klystron. The difference is that the former mode is used to fill up the empty pulses of the injection pattern and the latter beam mode is set during the initialization period of the timing system and provides a less-frequent signal to warm up the klystron.

The beam-mode-dependent event codes are arranged in a series of sequences and transferred in a single pulse every 20 ms. Several beam modes constitute an injection pattern

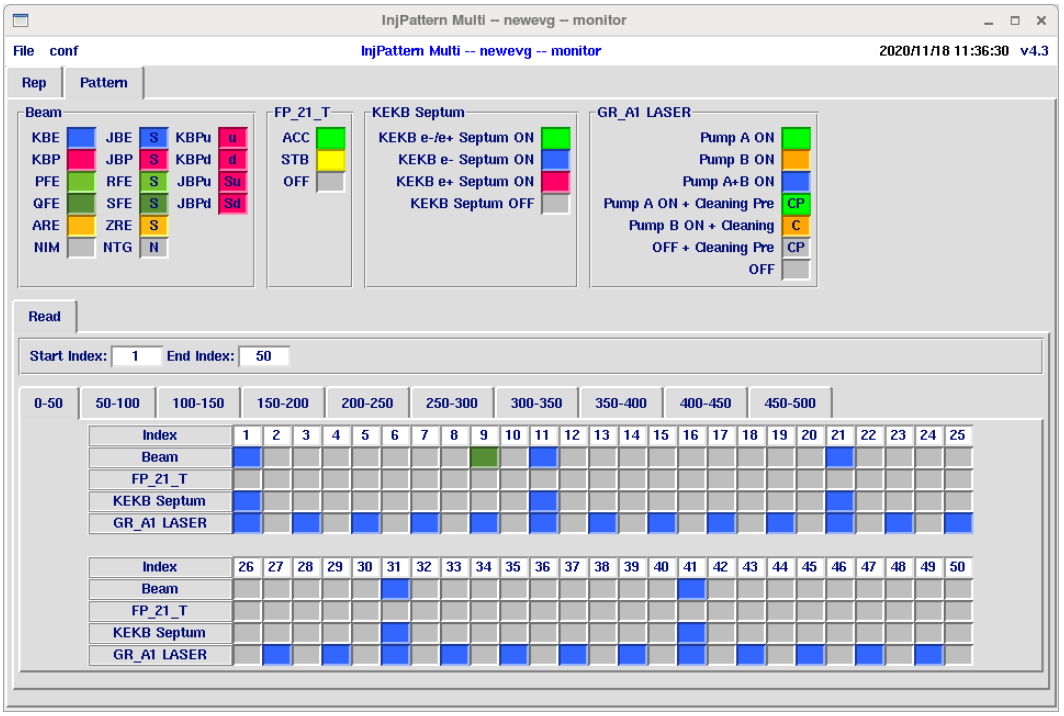


FIGURE 4.3: The GUI of IP-GEN program.

| Beam Mode | Event codes | Meaning |
|---|---|---|
| KBE | 30∼39 | HER injection |
| KBP | 40∼49 | LER injection |
| PFE | 50∼59 | PF injection |
| QFE | 60∼69 | PF injection |
| ARE | 70∼79 | PF-AR injection |
| JBE | 130∼139 | HER injection study |
| JBP | 140∼149 | LER injection study |
| RFE | 150∼159 | PF injection study |
| SFE | 160∼169 | PF injection study |
| ZRE | 170∼179 | PF-AR injection study |
| NIM | 180∼189 | No injection mode |
| NTM | 190∼199 | No trigger mode |

TABLE 4.2: Beam modes and event codes defined at KEK LINAC.

that is produced by a software named injection pattern generator (IP-GEN). The IP-GEN reads the beam mode frequency values specified from downstream rings and/or human operators, and then it generates the real injection pattern with a length up to 10 s (500∗20 ms) through some rules such as the pre-assigned beam mode priorities. The location of each beam mode inside the injection pattern can also be manually configured by the operator. All the beam modes inside an injection pattern are delivered one by one and the whole pattern is repeated until a new pattern is set at the end of the previous pattern. An example of the injection pattern is shown in Fig. 4.3. The 5 Hz KBE mode

and 1 Hz QFE mode are selected while the other 44 Hz is taken up by the NIM mode. The injection order of the beam mode can be determined not only by the beam mode priorities but also by the manual selection of the box in the GUI program of IP-GEN.

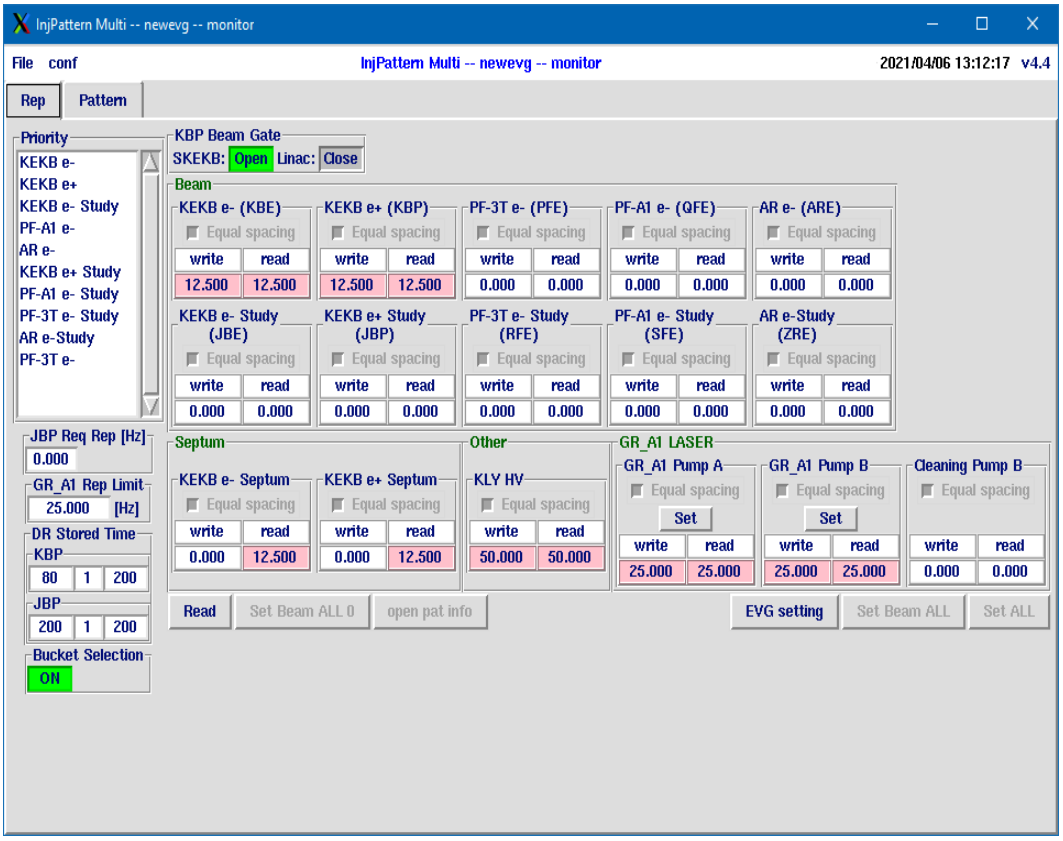


FIGURE 4.4: The repetition rate of beam modes in IP-GEN program.

The injection pattern can be automatically changed when the operator changes some parameters through the GUI program (see Fig. 4.4). For example, if the operator decreases the HER mode repetition rate, the non-injection mode repetition rate would increase accordingly. Similarly, if the sum of the repetition rates of different beam modes exceeds the limits, the repetition rate of the lower priority beam mode will decrease automatically. These parameters mainly include the following:

1. RF gun operation mode
2. Kicker magnet operation mode
3. Septum magnet operation mode
4. Beam mode repetition rate
5. Beam mode priority

6. Positron bunch storage time at DR

### 4.1.3 Dependency between Pulses

It is not an effortless task to change the beam mode pulse-to-pulse because of the existence of some requirements that originates from the injection and extraction hardware, i.e., pulsed kicker magnet at DR. Apart from the main-trigger signal, the kicker magnet needs some charge time which results in the requirement of the preparation trigger (pre-trigger) event. The pre-trigger should be delivered precisely before the main trigger, for example, 12 ms earlier than the main trigger for the DR kicker magnet with a precision of 0.1 ns [58]. The main-trigger timing changes every pulse owing to the bucket selection. Consequently, the pre-trigger timing changes per pulse accordingly.

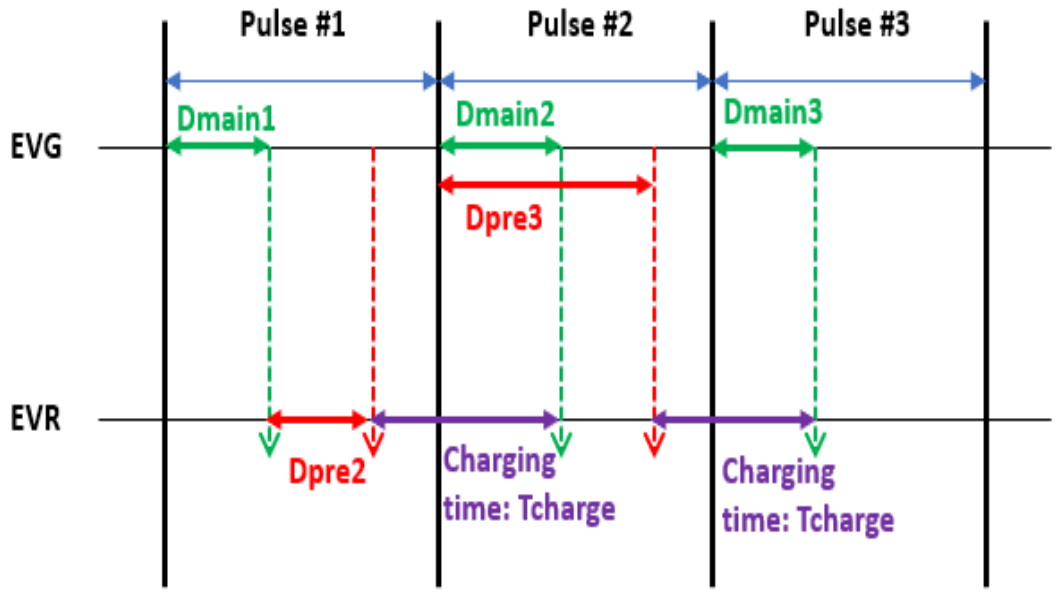


FIGURE 4.5: Schematic view of pre-trigger generation.

The logic used for pre-trigger generation are shown in Fig. 4.5. At first, it is necessary to calculate the main-trigger delay $D_{main}$ in the current pulse and next pulse based on which RF bucket is selected by the bucket selection scheme (see Section 3.3). The pre-trigger timing is denoted as $D_{pre}$ and can be calculated through the fixed charging time ($T_{charge}$) and the main-trigger delay. Since the charging time for the DR kicker magnet (12 ms) is close to the LINAC BRR, the pre-trigger is produced at the previous pulse. As a result, the pre-trigger for "pulse #2" is generated at "pulse #1". There are two kinds of methods to generate the pre-trigger signal and they are demonstrated as in

Eq. 4.1 and Eq. 4.2, respectively. The number "20" in the equations represents 20 ms and it is intuitive to derive the equation from Fig. 4.5.

Both delay values of pre-trigger are calculated inside the EVG, and the difference is that $D_{pre2}$ value is transferred through the data buffer feature of EVG, and the trigger delay is set at local EVR while the delay time of $D_{pre3}$ is counted by EVG and trigger is distributed to EVR through a dedicated event code. The advantage of pre-trigger calculation through Eq. 4.2 is that we could avoid the restriction of uncertainty of $D_{main}$ since $D_{pre2}$ timing is dependent on $D_{main1}$ timing. As we have introduced in Section 3.2 before, PF/PF-AR use different RF frequency with LINAC. The main triggers of PF/PF-AR injection cannot be calculated precisely since a chance coincidence algorithm between LINAC RF, and PF/PF-AR RF is utilized. Thus, the PF/PF-AR beam mode must not precede the LER beam mode if the method in Eq.4.1 is used.

$$D_{pre2} = D_{main2} - D_{main1} + 20 - T_{charge} \tag{4.1}$$

$$D_{pre3} = D_{main3} + 20 - T_{charge} \tag{4.2}$$

Another kind of cross-pulses dependency originates from the DR operation, we will discuss it later in Section 4.3.

## 4.2 AC50 Synchronization

As previously stated, the event timing triggering signal comes from AC50. It is usually necessary to maintain the beam intensity and quality on the same level for consecutive triggers. Some devices are sensitive to the AC line phase and might not satisfy the stability requirement when working at different AC line phases. The klystron is a good illustration of this. Some klystrons use the AC-powered filament or heater to heat the electron cathode, and the changing AC phase might generate a magnetic field that eventually affects the velocity modulation process of the klystron. Another measurement of the RF power and phase stability caused by the AC power line can be referred to

from [59]. Apart from the klystron, the power supply of the pulsed injection magnet also needs a stable AC phase to achieve the higher precision of magnetic field [4].

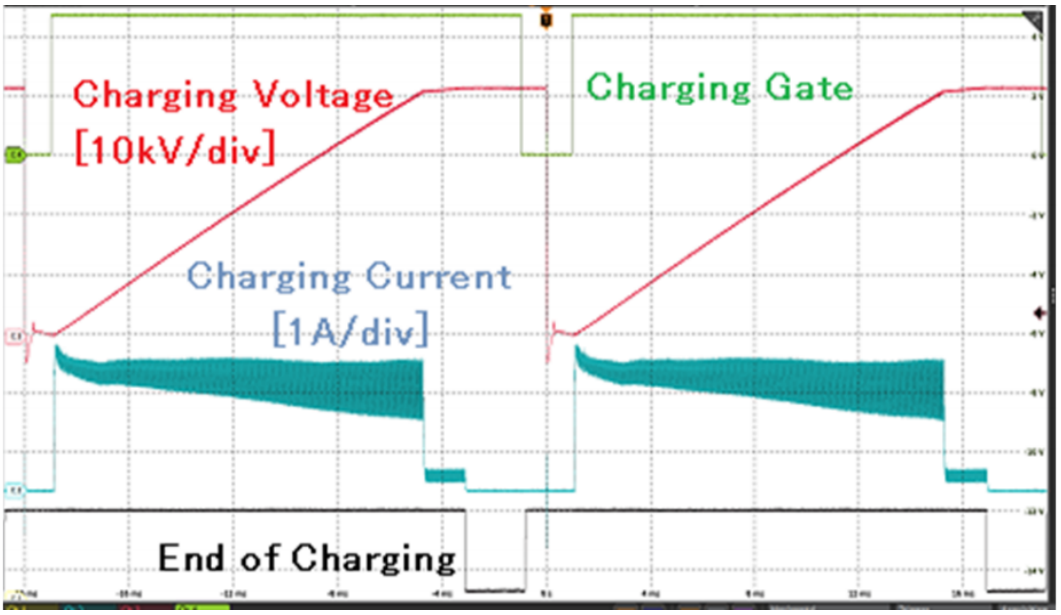


FIGURE 4.6: Charging time of PFN.

Another restriction of trigger interval comes from the klystron modulator. 60 high-power klystron units are installed at LINAC to accelerator the beam. The power supply of klystron, also known as klystron modulator, uses a charging power supply, a Pulse Forming Network (PFN), a thyratron switch, and a pulse transformer to provide 44 kV charging voltage to klystron [60]. The waveform of the charging gate signal in Fig. 4.6 shows that the ordered charging period is 18 ms to supply stable power for klystron. Therefore, the timing system is required to provide the trigger with an interval of at least 18 ms.

In the ordinary situation, the AC50 synchronization of the timing system for HER injection can be accomplished through the flip-flop circuit inside the MRF EVG module. The output of the synchronized signal is then used for triggering the sequence RAM which includes the event codes and delays. Both the AC50 synchronization and constrain of 18 ms trigger interval can be achieved. However, the BSC for LER is 22.68 ms, which cannot coincide with AC50 for every pulse. As Fig. 4.7 shows, the real trigger must appear in the 2 ms range near AC50 to satisfy both the AC50 trigger and 18 ms pulse interval restriction. The range of 2 ms is used for bucket selection purposes. This constrains conflicts with one cycle of the LER injection period.

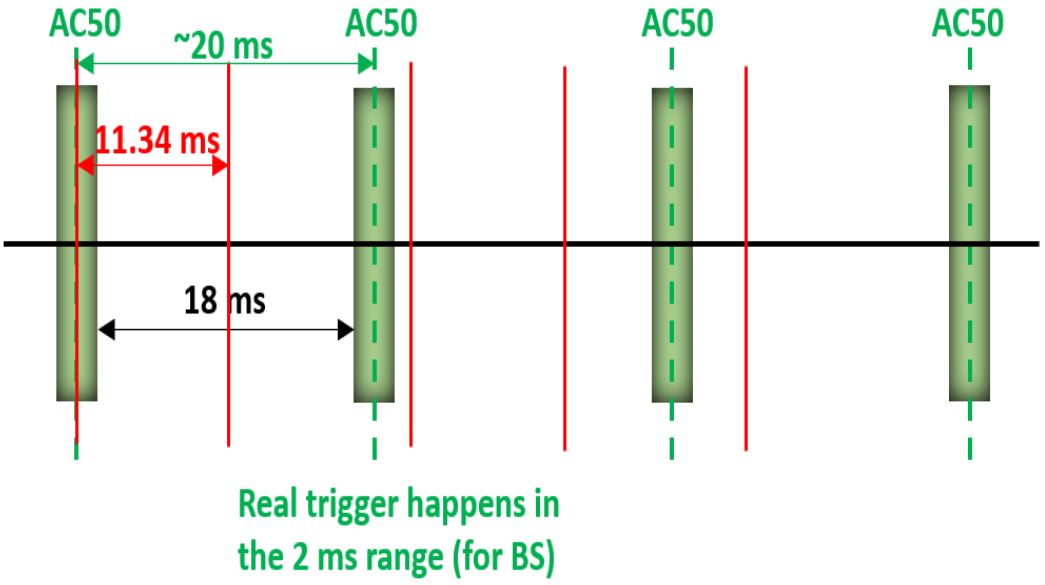


FIGURE 4.7: Synchronization between AC50 and BSC for LER cannot be achieved every pulse.

## 4.3 DR Operation

To increase the luminosity of SuperKEKB, the emittance of the injected positron beam should be small enough to be accepted in the aperture of the LER. The adoption of a new collision scheme called "nano-beam" requires the construction of DR [61]. Thus, the timing system needs to consider the operation of DR. Several new restrictions further increase the complexity of system implementation.

### 4.3.1 Dependency between Injection and Extraction Pulse

The pre-trigger of the kicker magnet at DR brings the dependency between subsequent pulses. Meanwhile, the DR operation brings the dependency between injection pulse and extraction pulse. At least 40 ms DR storage time is needed to achieve a satisfactory damping effect. Consequently, two pulses, which include one pulse for DR injection and one pulse for DR extraction, are needed to fully finish one time of LER injection. We have mentioned that two EVGs collaborate to control the injection process. Based on the repetition rate of LER injection and DR storage time, there are three DR operation modes. These DR operation modes can be categorized like Table 4.3.

| **Beam Mode** | **Beam Gate** | | **Use** |
|---|---|---|---|
| | Injection | Extraction | |
| KBP | Open | Open | Continuous injection |
| KBPu | Open | Close | Gun firing and DR injection |
| KBPd | Close | Open | DR extraction and LER injection |

TABLE 4.3: DR operation modes.

KBPu mode stands for the upstream LINAC operation for positron beam delivering. The electron gun is fired, and the electron beam bombards a tungsten target to generate a positron beam which is then injected into DR through DR injection kicker and septum. On the other hand, KBPd mode means that stored beam in DR is extracted but there is no newly injected beam for DR. KBP mode is normally used for continuous injection to LER which means both extraction and injection are performed in a single pulse.

The delay value of trigger signal in KBPd pulse is calculated at several pulses before, i.e., in KBPu pulse, because of the bucket selection process. After deciding the LER bucket number with the help of either the "BCE" or "star" scheme, the delay for LER injection, also known as the delay for DR extraction, can be calculated. The DR bucket number is then derived based on the DR storage time. Finally, the delay for DR injection is acquired and set in the upstream EVG. After DR storage time has passed, the delay for LER injection is used for extracting the stored bunch in DR.

### 4.3.2 DR Storage Time

The minimal DR storage timing $T_{storage}$ is limited to 40 ms while the maximal DR storage time is decided to owe to another consideration [4]. Because of the hardware at downstream LINAC, the DR extraction timing must also refer to the AC50 phase. Note that the DR extraction timing is calculated based on the AC50 in the DR injection pulse, the extraction timing has a relative drift to AC50 since the AC50 always drifts. Figure 4.8 shows time difference between DR extraction timing and AC50 measured in 2018 [46]. The time difference becomes larger when $T_{storage}$ becomes longer. The maximal DR storage time, $T_{max}$, is decided to be 200 ms.

$$T_{storage} = Min(n_{pulse} * T_{rep}, T_{max}) \tag{4.3}$$

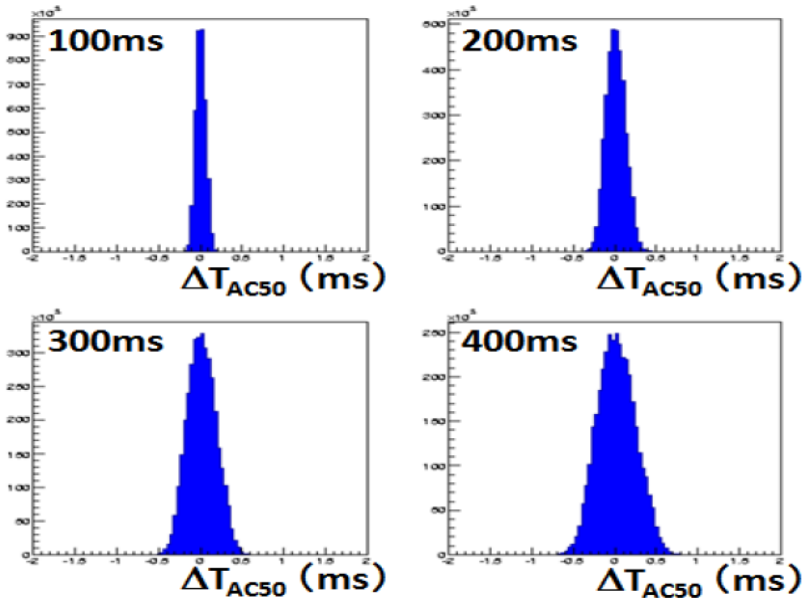


FIGURE 4.8: Time difference between DR extraction trigger and AC50.

The 2-pulse injection is implemented by storing bunches of two LINAC pulses in DR to improve the DR operation efficiency. Both 2-pulse operation mode and LER injection repetition rate ($f_{rep}$) affect the real $T_{storage}$. The calculation can be referred in Eq. 4.3. Table 4.4 lists several calculation examples of DR storage time.

| $f_{rep}$ [Hz] | $T_{rep}$ [ms] | $n_{pulse}$ | $T_{max}$ [ms] | $T_{storage}$ [ms] |
|---|---|---|---|---|
| 50 | 20 | 2 | 200 | 40 |
| 25 | 40 | 2 | 200 | 80 |
| 25 | 40 | 1 | 200 | 40 |
| 12.5 | 80 | 2 | 200 | 160 |
| 12.5 | 80 | 1 | 200 | 80 |
| 10 | 100 | 2 | 200 | 200 |
| 10 | 100 | 1 | 200 | 100 |
| 5 | 200 | 1 | 200 | 200 |
| 1 | 1000 | 1 | 200 | 200 |

TABLE 4.4: DR storage time is affected by KBP mode repetition rate and 2-pulse mode.

### 4.3.3 2-bunch and 2-pulse operation

2-bunch operation is adopted to increase the LINAC operation efficiency since the charge of high intensity, single-bunched primary electron beam for positron production has almost approached the beam blow-up threshold due to single-bunch transverse wakefield effects [62]. To inject two bunches into the DR, the DR kicker needs to supply a magnetic

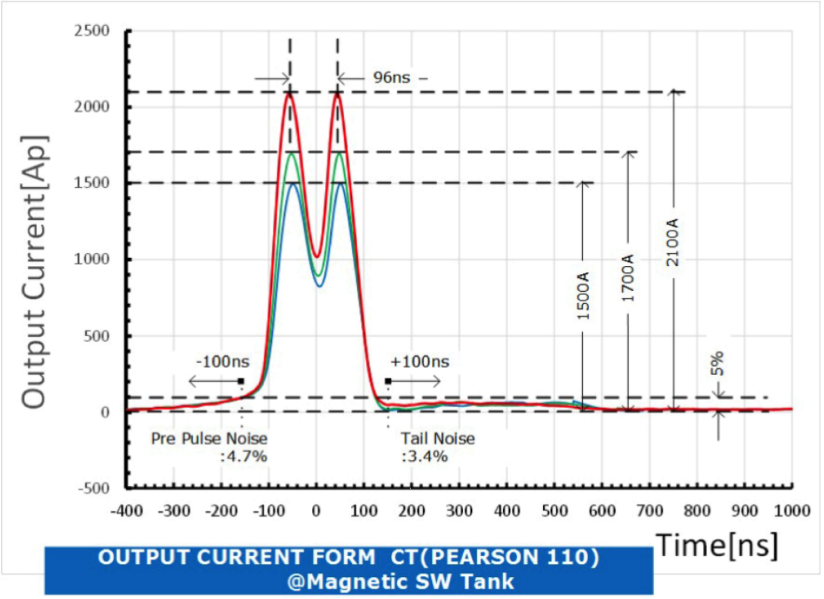


FIGURE 4.9: DR kicker magnets are active due to the power supply rising and falling time of 100 ns.

field with two peaks and the distance should be exactly 96.3 ns. As shown in Fig. 4.9, the DR kicker magnet power supply provides the required bi-peak shape of the magnetic field. The rising and falling time before and after the bi-peak output will affect the stored bunches when the 2-bunch injection is performing. As a result, the RF buckets, that are at a distance of fewer than 100 ns to stored bunches, should not be selected [4].

Figure 4.10 shows the 2-bunch and 1-pulse operation of DR. The DR storage time is 40 ms and the KBP repetition rate is 25 Hz. During the DR extraction pulse, the stored 2 bunches which are injected two pulses before are first extracted and then two new bunches are injected into DR. All the DR RF buckets can be selected under this circumstance.

Another situation is described in Fig. 4.11. If DR storage time is increased to 80 ms, the 2-bunch and 2-pulse operation become necessary. Considering the 96 ns (49 RF buckets) bunch space of 2-bunch beam and 100 ns kicker magnet field rising time (50 RF buckets), only 31 DR RF buckets can be selected for the newly injected bunch during the 2-bunch and 2-pulse operation. For example, if DR bucket "#0" and "#49" are already occupied, newly injected two bunches can only select the range between "#100 (#149 for the second bunch)" and "#130 (#179 for the second bunch)".

When this restriction comes together with the 2 ms injection window limit caused by the

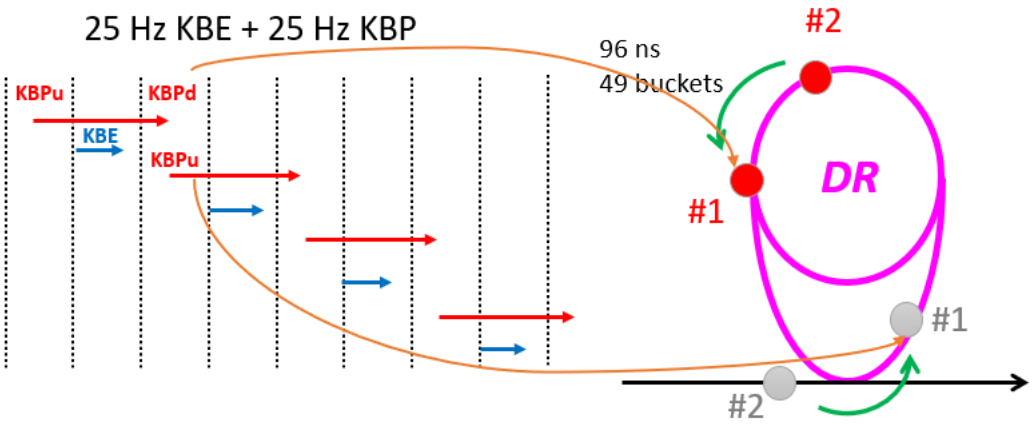


FIGURE 4.10: DR operation with 2-bunch and 1-pulse injection.

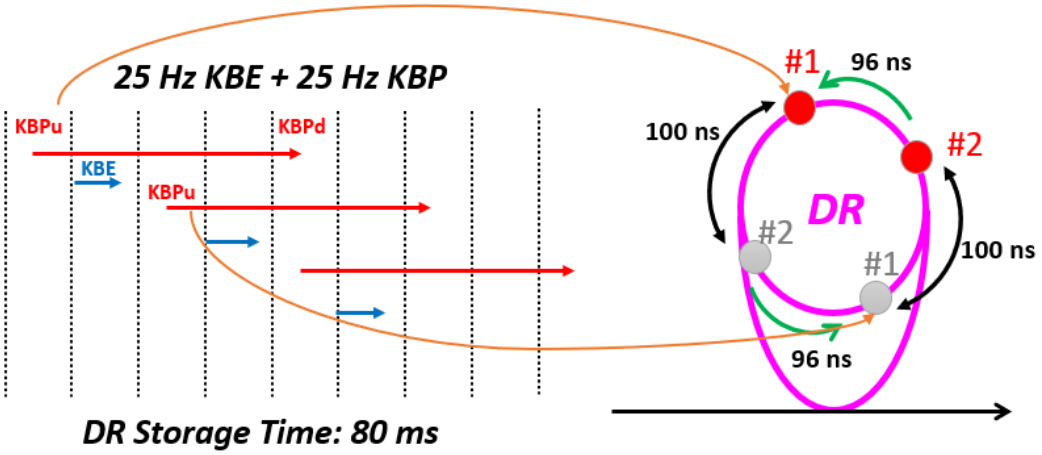


FIGURE 4.11: DR operation with 2-bunch and 2-pulse injection.

klystron modulator, the available LER RF buckets number is also affected. For example, if we want to inject into LER bucket "#0", the DR-LER bucket combination for can be calculated based on Eq. 3.1 and Eq. 3.1. There exist a total of 23 BSC for LER cycles to inject into the same LER bucket. Table 4.5 shows the relation between cycle number, injection opportunity, delay time and DR RF bucket. All 23 DR RF buckets that can inject into the LER RF bucket "#0" are listed.

Figure 4.12 shows the time chart of DR bucket selection during 2-bunch and 2-pulse operation. The AC50 comes in the middle of cycle "#5" and cycle "#6". The 2 ms injection window restricts the candidate DR RF bucket number. If we want to inject into LER bucket "#0" and DR bucket "#0" and "#49" are already occupied, the possible DR RF buckets are between "#100" and "#130". However, as Fig. 4.12 shows, only DR

| Cycle | Injection opportunity | Delay [$\mu$s] | LER Bucket | DR Bucket |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 5120*1 | 493*1 | 0 | 180 |
| 2 | 5120*2 | 493*2 | 0 | 130 |
| 3 | 5120*3 | 493*3 | 0 | 80 |
| 4 | 5120*4 | 493*4 | 0 | 30 |
| 5 | 5120*5 | 493*5 | 0 | 210 |
| 6 | 5120*6 | 493*6 | 0 | 160 |
| 7 | 5120*7 | 493*7 | 0 | 110 |
| 8 | 5120*8 | 493*8 | 0 | 60 |
| 9 | 5120*9 | 493*9 | 0 | 10 |
| 10 | 5120*10 | 493*10 | 0 | 190 |
| 11 | 5120*11 | 493*11 | 0 | 140 |
| 12 | 5120*12 | 493*12 | 0 | 90 |
| 13 | 5120*13 | 493*13 | 0 | 40 |
| 14 | 5120*14 | 493*14 | 0 | 220 |
| 15 | 5120*15 | 493*15 | 0 | 170 |
| 16 | 5120*16 | 493*16 | 0 | 120 |
| 17 | 5120*17 | 493*17 | 0 | 70 |
| 18 | 5120*18 | 493*18 | 0 | 20 |
| 19 | 5120*19 | 493*19 | 0 | 200 |
| 20 | 5120*20 | 493*20 | 0 | 150 |
| 21 | 5120*21 | 493*21 | 0 | 100 |
| 22 | 5120*22 | 493*22 | 0 | 50 |

TABLE 4.5: Injection delay and corresponding DR bucket for LER bucket "#0".

RF buckets "#80", "#30", "#210" and "#160" can be used. Under this circumstance, the LER RF bucket "#0" cannot be injected into this pulse.

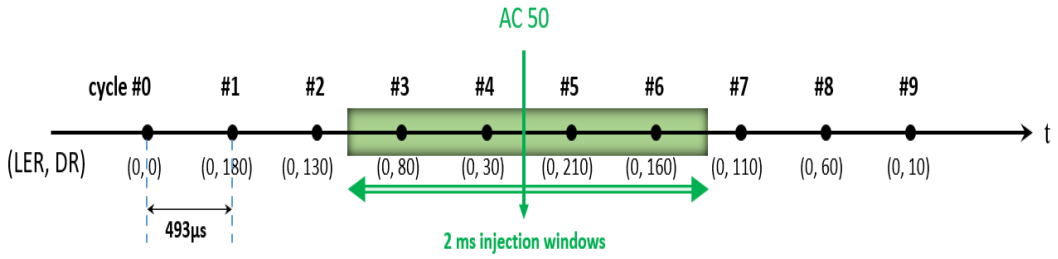


FIGURE 4.12: The 2 ms injection windows comes together with 2-bunch and 2-pulse operation.

Note that, this restriction appears not only when 2-bunch and 2-pulse operation is used. Because of the shape of the DR kicker magnet field, this restriction exists for 1-bunch and 2-pulse operations. The optional DR buckets are 81 [63]. Appendix A.1 shows the simulation process through a python program. The results are listed in Table 4.6.

There are only 2798 LER RF buckets that can be selected for 2-bunch and 2-pulse mode. Almost half of the LER RF buckets cannot be selected during the operation.

| DR,MR | | Pulse | |
|---|---|---|---|
| | | 1 | 2 |
| Bunch | 1 | 230,5120 | 80,5120 |
| | 2 | 230,5120 | 31,2798 |

TABLE 4.6: Available RF buckets for DR operation.

# Chapter 5

# Implementation of Timing System at KEK LINAC

## 5.1 Sequence Shift

We have already mentioned in Section 4.2 that the difficulty in finding the coincidence between AC50 and BSC for DR and LER every 50 Hz. The basic BSC for DR and LER is 88.19 Hz according to Section 3.3.1 and half of the frequency is used in practice since it is easy to implement. Thus, 44.1 Hz is used as the real repetition rate for LER bucket selection. The period of 44.1 Hz is 22.68 ms. As shown in Fig. 3.8, this signal is generated from the 508.89 MHz MR-MO and used for the master trigger of MTS.

One possible solution is to utilize the method called "sequence shift" by grouping several strict 50 Hz pulses as a sequence. The sequence itself is triggered every 22.68 ms and the actual event timing triggers, which follow the AC50 phase, happens at every pulse inside a sequence. Furthermore, two sequences of uneven length switch alternately to adjust the arriving timing of AC50.

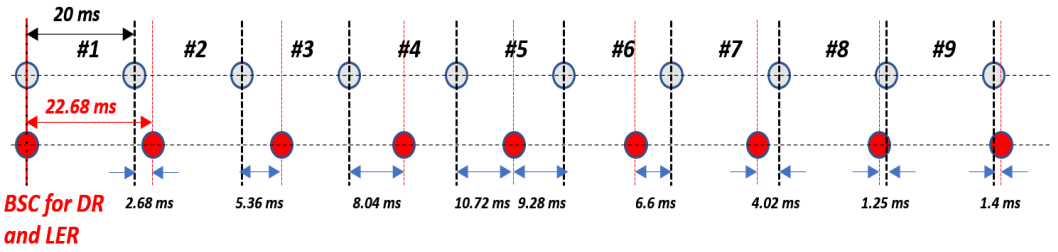


FIGURE 5.1: Time difference between BSC and 50 Hz.

### 5.1.1 8/9 Pulses Sequence Shift

Figure 5.1 shows the time difference between BSC and 50 Hz. The distance between 50 Hz trigger point and 44.1 Hz point can be calculated through Table 5.1. After 8 50-Hz pulses, the 44.1 Hz signal comes 1.25 ms earlier than the next 50 Hz pulse. In contrast, after 9 50-Hz pulses, the 44.1 Hz signal comes 1.4 ms later than the next 50 Hz pulse. As a result, all pulses inside an 8/9 pulses sequence can find the coincidence position with 44.1 Hz based on the fixed pulse length and pulse number. For example, the injection into LER at pulse "#2" (see Fig. 5.1) can be done by setting the sum of bucket selection delay value and 2.68 ms as the real trigger delay value.

| # of 50 Hz pulse | Sequence length [ms] | Distance [ms] |
|---|---|---|
| 1 | 20 | +2.68 |
| 2 | 40 | +5.36 |
| 3 | 60 | +8.04 |
| 4 | 80 | +10.72 |
| 5 | 100 | -9.28 |
| 6 | 120 | -6.6 |
| 7 | 140 | -4.02 |
| 8 | 260 | -1.25 |
| 9 | 180 | 1.4 |

TABLE 5.1: The time interval between 50 Hz pulse and 44.1 Hz pulse.

To deliver the injection triggers on the same phase of AC50, the TDC is used to assure the arrival time of AC50. The TDC receives the start signal at the pulse start point every 20 ms. The stop channel uses AC50 which originates from the MTG module. Thus, the AC50 delay is measured by the TDC module every pulse, as shown in Fig. 5.2. We manage the length of the sequence for modulating the AC50 position. At the end of the 9 pulses sequence, the next sequence is launched 1.4 ms later and that means the start signal of TDC comes 1.4 ms later. In other words, the AC50 comes 1.4 ms earlier in the new sequence compared with the old 9 pulses sequence. In practice, the AC50 should

always appear in the middle of every pulse to keep a stable operation, and this can be accomplished through the sequence shift algorithm (see Section 5.1.2).

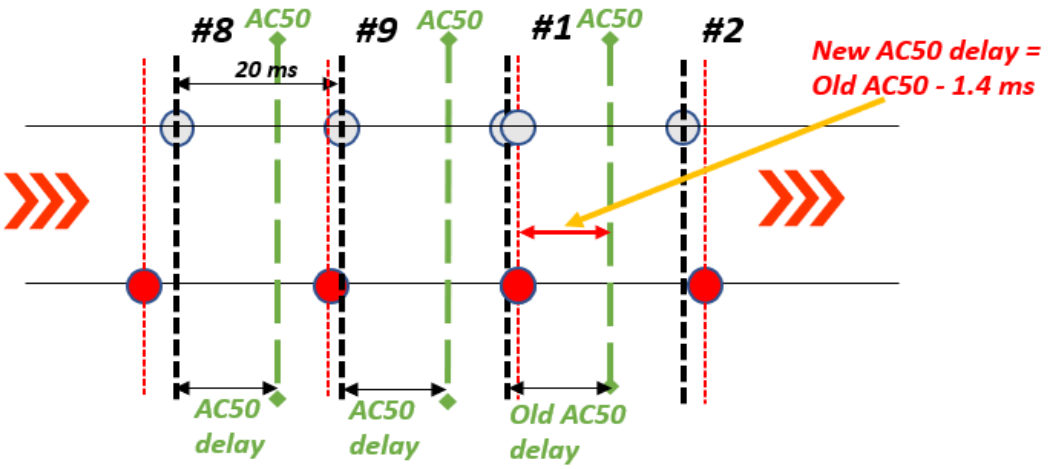


FIGURE 5.2: AC50 position manipulation by sequence shift.

Figure 5.3 shows the overall hierarchy of the timing chart at MTS. The injection pattern is divided into two kinds of sequences with 8/9 pulses. All sequences are trigged by a 44.1 Hz signal transferred from MR to synchronize with the BSC for DR and MR. Each pulse is strictly 20 ms and the main timing trigger happens together with the AC50 phase in a 2 ms window. Inside one 11.34 ms cycle, two fragment methods divide the cycle as 23 pieces of 493 $\mu$s or 512 pieces of 22.15 $\mu$s. As a result, the bucket selection delay for DR and MR can be acquired easily by two fragment methods. This process repeats after the sequence shift.

### 5.1.2 Sequence Shift Algorithm

During the start period of every pulse, hundreds of PPM parameters are changed to prepare the event delivery. Thus, the AC50 signal is required to come in the middle of every pulse to avoid interference from software processing. The sequence shift algorithm serves as a method to decide the next sequence length and its purpose is to keep the AC50 sit in the middle of every pulse.

| Sequence type | Length | Shit Value |
|---|---|---|
| Type A | 8 | 1.25 ms |
| Type B | 9 | -1.4 ms |

TABLE 5.2: Two kinds of sequence type.

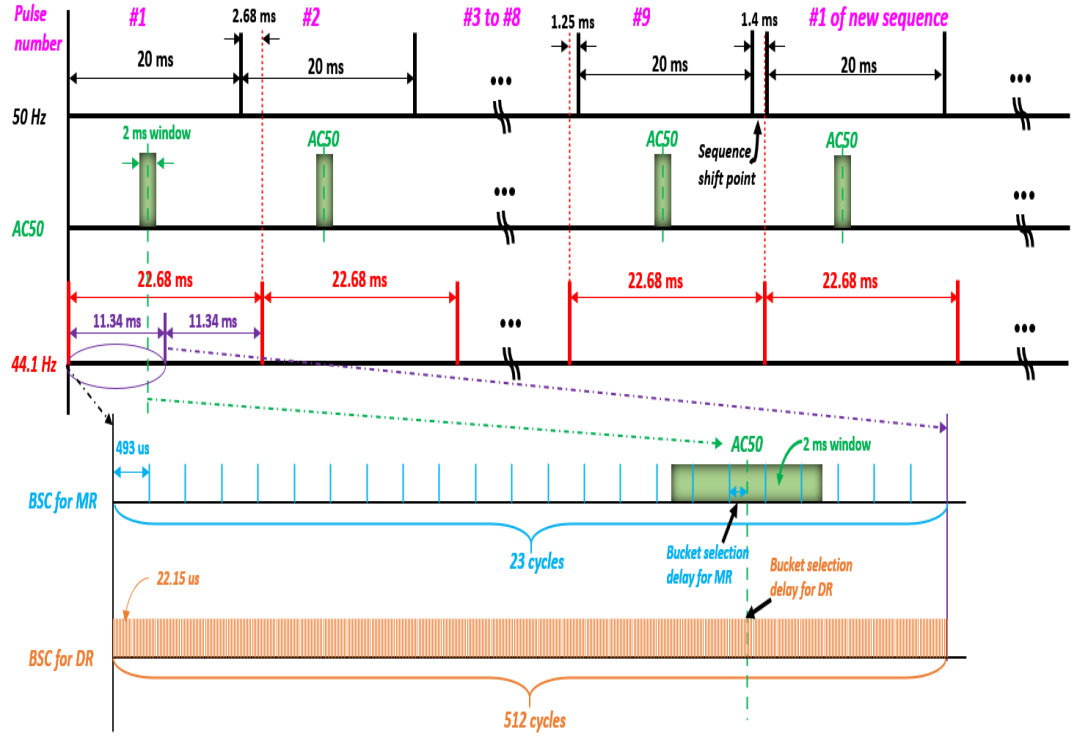


FIGURE 5.3: Logic of sequence shift.

The implementation of sequence shift requires several modules to provide adequate information. An MTG module with a voltage comparator circuit was manufactured to generate the AC50 signal at the fixed phase from the AC power line. A time-to-digital converter (TDC), which receives the "TDC start" and "TDC stop" signal, is used to measure the AC50 delay time with a resolution of 1 ns [2].

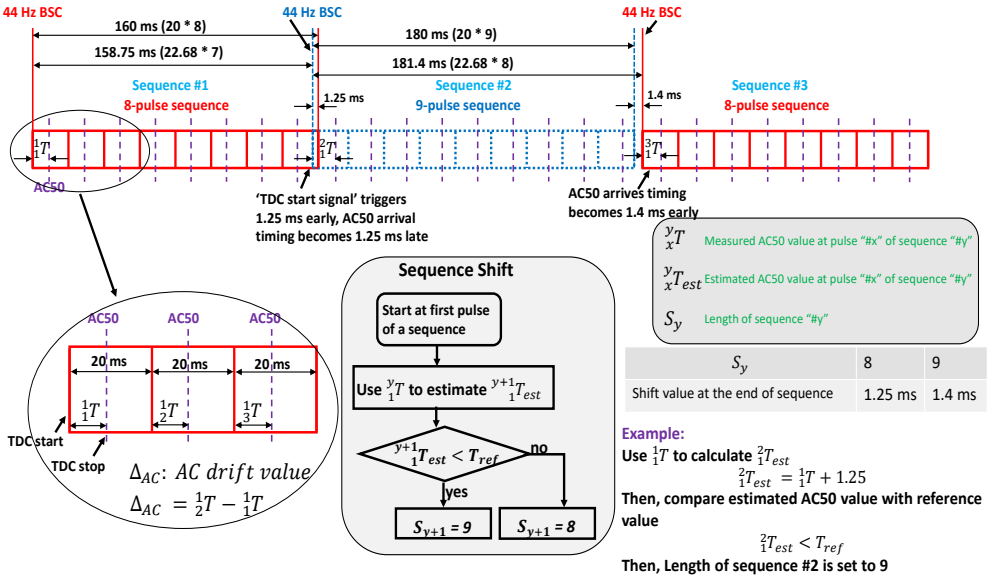


FIGURE 5.4: The schematic view of the sequence shift.

The schematic view of 8/9-pulse sequence shift is shown in Fig. 5.4. The sequence length was selected to 8 pulses and 9 pulses in 2015 [30]. Inside the 8/9-pulse sequence, the requirements for synchronizing to both 44 Hz BSC and AC50 are fulfilled at every pulse. The timing system starts with the 44 Hz BSC which serves as the fiducial point of bucket selection. Note that 44 Hz (i.e., 22.68 ms) rather than 88 Hz BSC is used because it is close to 20 ms and simplifies the system design. The pulse length is ideal 20 ms and different beam properties are modulated pulse-to-pulse. The AC50 arrival delay at every pulse is measured by the TDC module and is used for generating an AC50-synchronized beam timing signal. The range of AC50 arrival delay values is from 0 to 20 ms. The time distance between the fiducial point of bucket selection and AC50 in every pulse can be easily calculated based on the pulse number. For example, if the AC50 arrival delay measured in the third pulse is 10 ms, the overall bucket selection delay is 50 ms. Then, the DR and LER bucket number can be acquired through the formulas described in [46].

As shown in in Fig. 5.4, after an 8-pulse sequence, the discrepancy between ideal 20 ms pulse and 44 Hz BSC is 1.25 ms. The sequence "#2" is launched 1.25 ms earlier to resynchronize with 44 Hz BSC. Accordingly, the AC50 arrival delay at the first pulse of sequence "#2" becomes 1.25 ms later because the "TDC start" signal comes 1.25 ms earlier. Similarly, the sequence "#3" is launched 1.4 ms later after a 9-pulse sequence.

As the AC50 always drifts, the AC50 arrival timing can be out of the boundary in a pulse and break the synchronization requirement. The sequence shift algorithm is then used for compensating the AC50 drift and keeping AC50 arrival timing appear in the middle of a pulse. To explain the sequence shift algorithm, Let ${}^{y}_{x}T$ denote the AC50 arrival delay which is measured by TDC at pulse "#x" of sequence "#y', ${}^{y}_{x}T_{est}$ denote the estimated AC50 value at pulse "#x" of sequence "#y', $S_y$ denote length of sequence "#y" and $T_{ref}$ denote the reference value for AC50 arrival delay. The value of $S_y$ is either 8 or 9 which corresponds to AC50 shift value of 1.25 ms and 1.4 ms, respectively. The value of $T_{ref}$ is usually selected to be around 10 ms. The AC50 drift value $\Delta_{AC}$ can be expressed by the discrepancy of the AC50 arrival delay values for two continuous pulses.

The main purpose of sequence shift algorithm is to decide the length of next sequence and keep ${}^{y}_{x}T$ be close to $T_{ref}$. For example, the type of sequence "#2" is decided at

the first pulse of sequence "#1". The estimated AC50 arrival timing ${}^{2}_{1}T_{est}$ is derived from the TDC measurement value ${}^{1}_{1}T$ and sequence shift value (i.e., 1.25 ms). If ${}^{2}_{1}T_{est}$ is smaller than $T_{ref}$, the type of next sequence is selected as 9-pulse sequence; otherwise, 8-pulse sequence is selected.

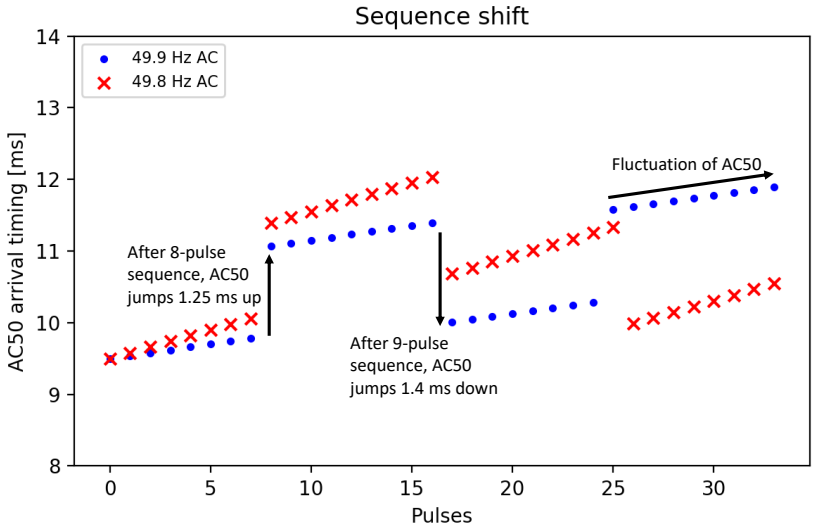


FIGURE 5.5: Example of sequence shift under two kinds of AC50 frequencies.

Figure 5.5 illustrates the example sequence shift under different AC50 frequencies. Every point represents the measured AC50 arrival delay in an injection pulse. The AC50 drift value $\Delta_{AC}$ is 40 $\mu$s and 80 $\mu$s for the AC line frequency of 49.9 and 49.8 Hz, respectively. The initial AC50 arrival timing is 9.5 ms and the AC50 reference value $T_{ref}$ is 9.85 ms. Two different decisions on the length of the next sequence are made at the first pulse of the second sequence. Larger AC50 arrival timing caused by fluctuation of AC50 is corrected by sequence shift. Consequently, the AC50 arrival delay value oscillates around the $T_{ref}$. The long-term stability of the 8/9-pulse sequence shift was studied in 2015 and loss of triggers was not observed [30].

### 5.1.3 16/18 Pulses Sequence Shift

According to Section 4.3.2, the maximal DR storage time is chosen to be 200 ms. The maximal pulse discrepancy between DR injection and DR extraction is also 200 ms which is longer than the sequence length (i.e., 160 ms for 8 pulses sequence and 180 ms for 9 pulses sequence).

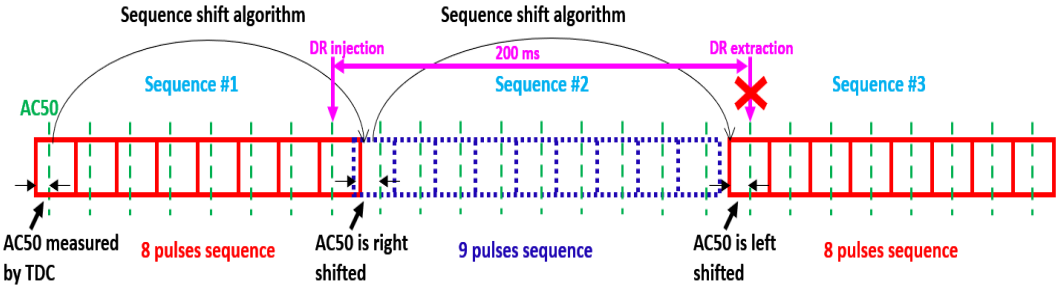


FIGURE 5.6: The conflict between 8/9 pulses sequence and DR storage time.

Figure 5.6 shows the problem when DR storage time of 200 ms is utilized. Both the DR injection and extraction delay are calculated in the DR injection pulse to keep the synchronization between DR and LER. If DR is injected at the end pulse of sequence "#1", the extraction timing happens 200 ms later, which is the first pulse of sequence "#3", should be determined also at the injection pulse. However, the sequence type of "#3" will not be decided until the delivery of sequence "#2". As a result, the extraction delay for MR is uncertain. Finally, the sequence length is enlarged to 16/18 pulses sequence to handle the 200 ms DR storage time and the sequence shift value changes to **2.8 ms** and **2.5 ms**.

## 5.2 Structure of Main Timing Station

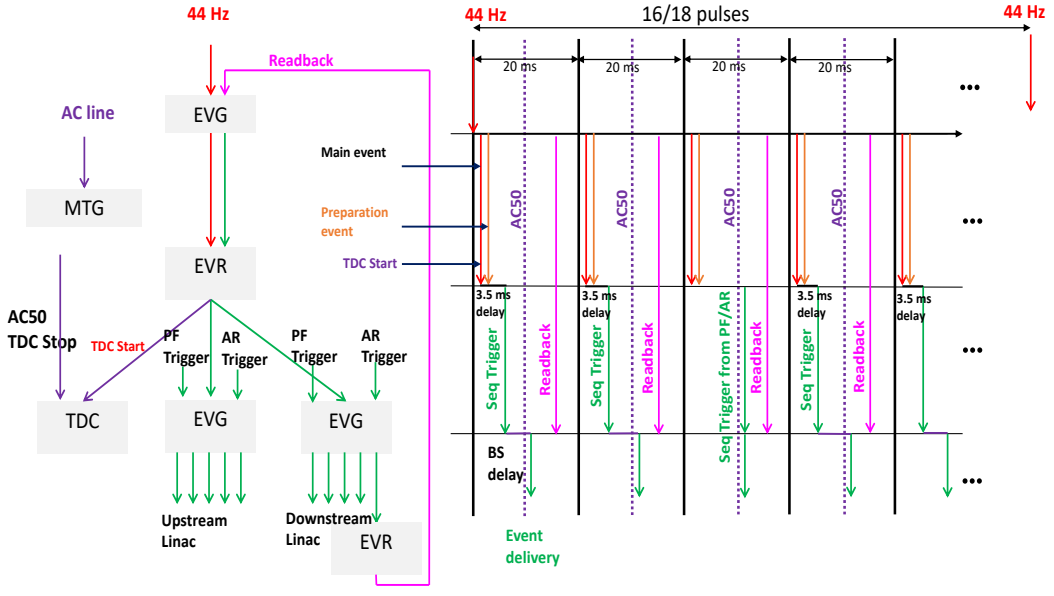


FIGURE 5.7: Schematic view of MTS.

Figure 5.7 shows the structure of MTS. Three EVGs and two EVRs are utilized to generate event codes and control the injection procedure [64]. The MTG and TDC module provide the ability to measure the AC50 arrival timing and supply the AC50 value for the decision-making of the sequence shift algorithm.

One upper-level EVG is triggered by the 44.1 Hz signal transmitted from SuperKEKB to synchronize the injection procedure between DR and LER. It carefully separates the injection pattern into 16/18 pulses sequence and delivers the main event and pre-event to the middle EVR every 20 ms. A fiber-based event link is used for event codes transmission. The main event and pre-event are then used for controlling two lower-level EVGs.

The middle EVR is responsible for generating pulses from the main event and pre-event. The pulse generated on the arrival of the main event triggers both the TDC and sequencer of two lower-level EVG. The trigger for TDC happens immediately and the trigger for two lower-level EVG happens after a 3.5 ms delay. This 3.5 ms delay is achieved by the pulse generator in EVR and this period is used to reserve the running time of beam mode change logic. The pre-event changes the contents of the sequencer called "software sequencer", which include beam mode of the next pulse as well as the sequencer trigger source. Note that, these changes only happen at the software level and need to be loaded later into the "hardware sequencer" to take effect.

Two lower-level EVGs send 12 or 13 event codes every pulse to all local EVRs all over the accelerator. One of the EVGs controls the upstream LINAC hardware while another manages the downstream LINAC. The events are changed based on the beam mode arrangement and the bucket selection delays are read from the RFM module which are calculated two pulses before. The trigger source of two lower-level EVGs switches is based on the beam mode. If the current beam mode is PF/PF-AR, then the trigger directly comes from the change coincidence between LINAC RF and PF/PF-AR revolution frequency. Other beam modes use the output pulse from EVR as a sequencer trigger.

A local EVR receives the event codes and sends a "readback" to upper-level EVG to assure that current event codes are successfully delivered. This "readback" signal rearms the "hardware sequencer" of two lower-level EVGs, whose contents are already changed on the pre-event triggering several milliseconds before. Then, these event codes inside

the "hardware sequencer" are sent out with defined delay when trigger signals come in the next pulse. It also triggers the processing of bucket selection of the next-next pulse by sending a network interrupt to the CCB node in SuperKEKB through the RFM module.

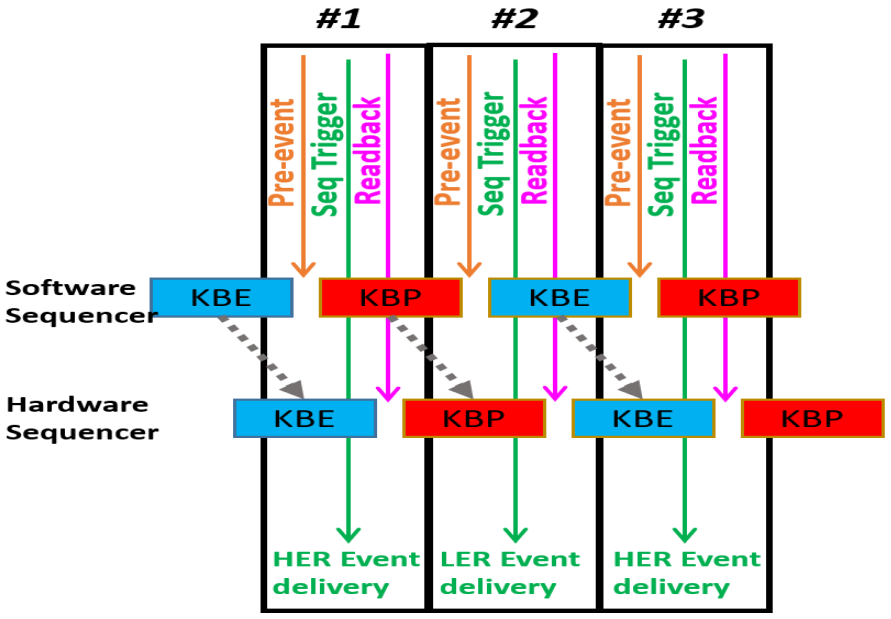


FIGURE 5.8: Sequence of 3 important triggers happening in one MTS pulse.

Figure 5.8 shows the sequence of 3 important signal for EVG sequencer. The content of "software sequencer" is changed upon the pre-event. Later, the real sequence trigger signal sends out the event codes in the "hardware sequencer". After the local EVR confirms the successful delivery of the event, the "readback" signal loads the content from "software sequencer" to "hardware sequencer".

With the help of this architecture, the requirements originate from double-ring bucket selection and AC50 synchronization are fulfilled.

## 5.3 RF Phase Shift of LINAC

### 5.3.1 Implementation of RF Phase Shift

The constriction discussed in Section 4.3.3 can be handled through a method like a sequence shift. By shift, the RF phase of "downstream LINAC", the extraction opportunities for bunches stored in DR are increased. Figure 5.9 shows the schematic diagram

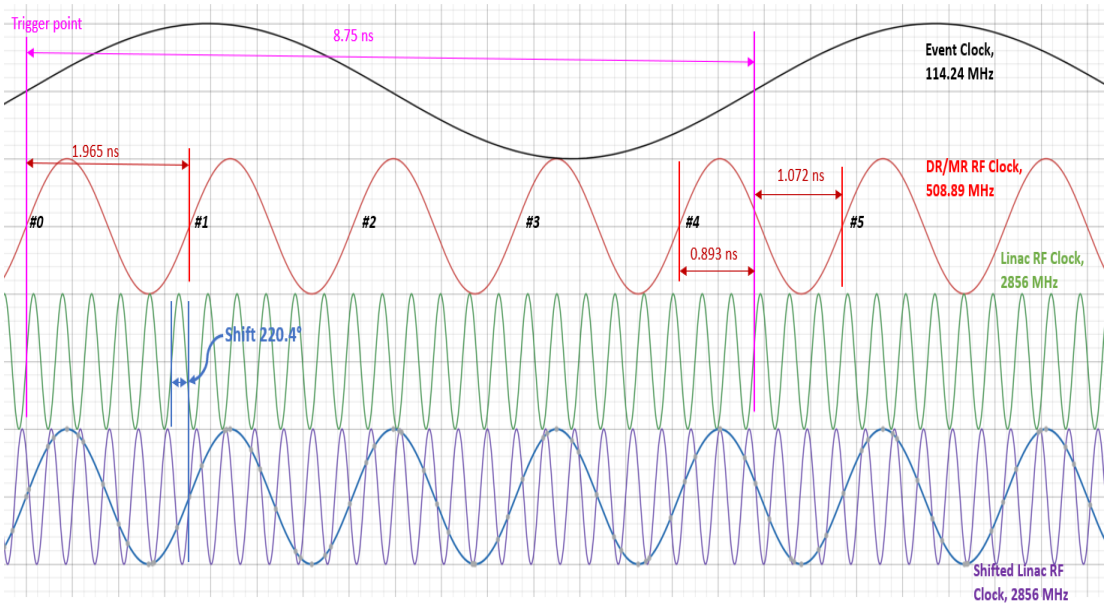


FIGURE 5.9: RF phase shift of downstream LINAC.

of RF phase shift. The coincidence relationship between three RF frequencies is listed. All the event timing system trigger signals should be delivered based on the 114.24 MHz event clock, i.e., 8.75 ns. In the event cycle of the DR/MR RF clock, a bucket can be filled. The coincidence points between DR/MR RF and LINAC RF appear every 49 cycles of the DR/MR RF clock or every 11 cycles of the event clock. Without RF phase shift, the distance between two contiguously injected RF buckets is 49. After bucket "#0" in DR/MR can is filled at the trigger point, the next injection opportunity appears at 96.3 ns later.

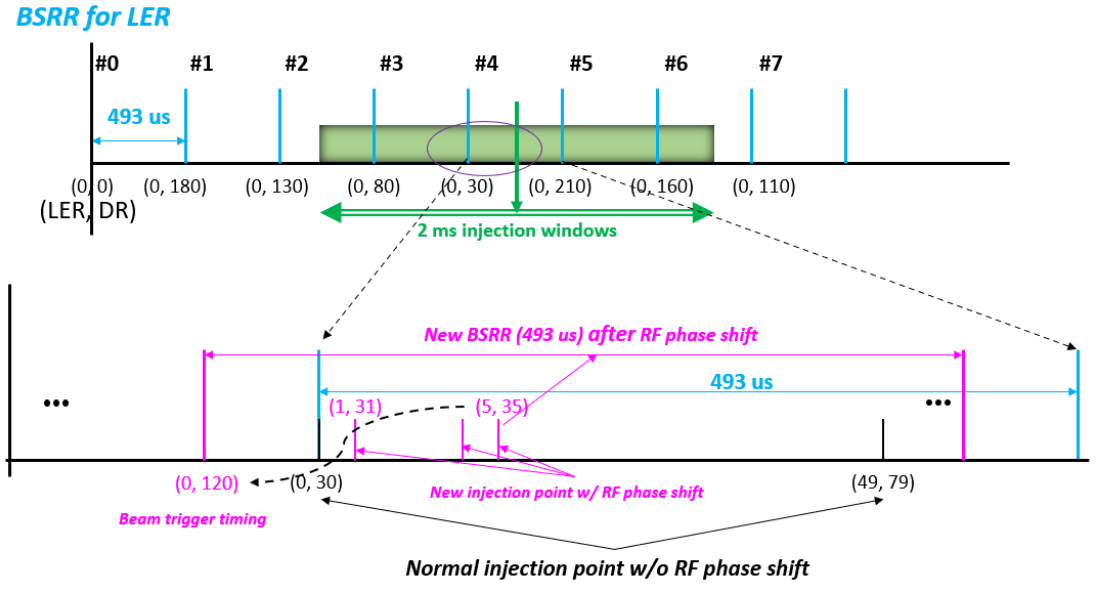


FIGURE 5.10: Schematic view of RF phase shift in downstream LINAC.

To increase the coincidence relation between ring RF and LINAC RF, we can shift LINAC RF to synchronize with ring RF again. As shown in Fig. 5.9, by shifting 220.4° of LINAC RF, RF bucket "#1" is synchronized with LINAC RF again and can be extracted into LINAC from DR. The time interval between event clock trigger point and real beam timing becomes 1.965 ns. Similarly, if we generate a trigger signal at one event cycle later (i.e., 8.75 ns later), RF bucket "#4" and "#5" can be extracted from DR into LER by shifting LINAC RF -0.893 ns (161.633°) and 1.072 ns (22.04°), respectively.

Consider LER bucket "#$m_0$" injection example in Section 4.3.3 again, if we want to inject into LER bucket "#0" and DR buckets "#0" and "#49" are already occupied, range of optional DR buckets are between "#100" and "#130". However, only "#80", "#30", "#210" and "#160" are available in 2 ms injection windows. As Fig. 5.10 shows, the normal injection points without RF phase shift allow us to inject into LER bucket "#0" through DR bucket "#30". By shifting the RF phase and generator the trigger for one event clock (8.75 ns) later, DR bucket "#5" can be extracted into LINAC and injected into LER bucket "#35". Based on the combination of DR bucket "#5" and LER bucket "#35", the current cycle of BSC for LER only can be determined through Table 3.4. Thus, the timing for LER bucket "#0" through DR bucket "#120" is acquired. DR bucket "#120" is also available under the restriction of 2 ms injection window and 2-bunch and 2-pulse operation. The overall effect is also demonstrated in Fig. 5.11. The BSC cycle is shifted when the "downstream LINAC" RF phase is shifted, and their relation can be calculated.

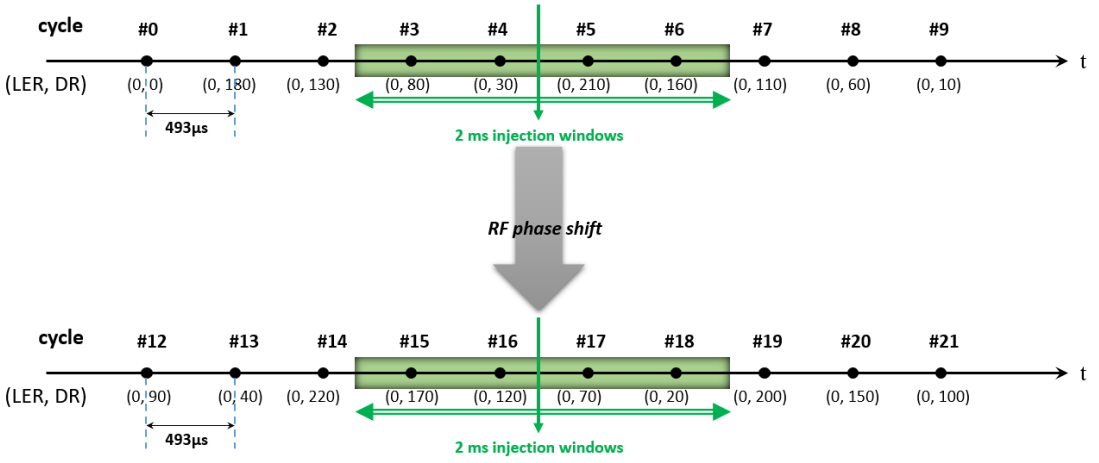


FIGURE 5.11: Equivalent view of BSC cycle shift by RF phase shift.

The calculation of new LER-DR bucket combination is described in Fig 5.12. After deciding the LER bucket number $M_0$ by bucket selection scheme, the bucket selection delay $clock_0$ and DR bucket number $D_0$ are calculated through the method described in Section 3.3.1. Then we check whether $D_0$ is available during the 2-bunch and 2-pulse operation. If $D_0$ can be selected, the LER injection is successfully performed without RF phase shift in "downstream LINAC". On the contrary, the RF phase in "downstream LINAC" is shifted to coincide with RF bucket $M_0 + n$ and $D_0 + n$. The corresponding event timing shift value is $k$ cycles of event clock $T_{event}$, i.e., $k * 8.75\ ns$. Note that, there are small time differences, which is denoted as $\Delta T$ between beam trigger and event timing trigger. We will discuss the impact of $\Delta T$ later. According to the bucket combination of $M_0+n$ and $D_0+n$, it is easy to find the delay value $Delay[M_0+n]$ based on Table 3.4. The delay value $Delay[M_0+n]$ represents the time interval between LER-DR combination of $(0, D_1)$ and $(M_0 + n, D_0 + n)$. Similarly, the delay value $Delay[M_0]$ represents the time interval between LER-DR combination of $(0, D_1)$ and $(M_0, D_2)$. What we finally want to know is the DR bucket $D_2$ and the bucket selection delay $clock_1$. By setting delay value of $clock_1$, LER bucket $M_0$ can be injected through DR bucket $D_2$. Then, we could check whether $D_2$ is available during 2-bunch and 2-pulse operation.

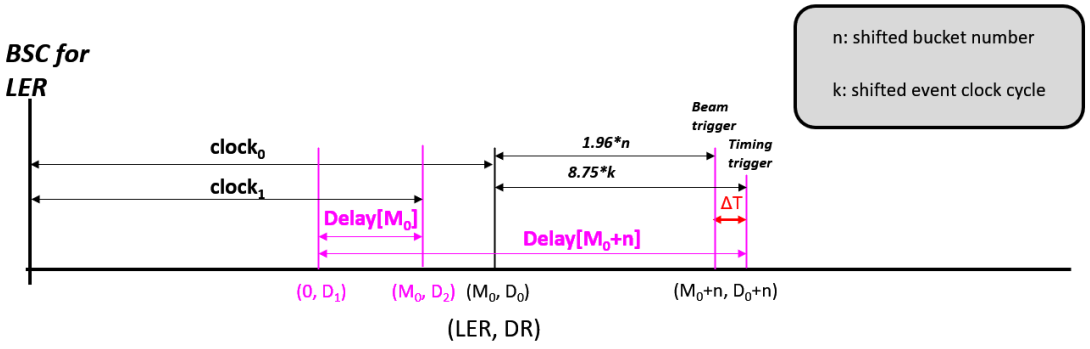


FIGURE 5.12: Calculation process of new DR bucket under RF phase shift.

$$clock_1 = clock_0 + T_{event} * k - Delay[M_0 + n] + Delay[M_0] \tag{5.1}$$

$$D_2 = MOD\left(\frac{clock_1 * 49}{96.3}, 230\right) \tag{5.2}$$

The delay value of $clock_1$ can be calculated through Eq. 5.1 and DR bucket $D_2$ can be calculated through Eq. 5.2.

### 5.3.2 Balance of DR Bucket Selection

Although another DR RF bucket can be selected with the help of RF phase shift, there are some compromises on the decision of the extent of phase shifting, which mainly includes,

- Time difference $\Delta T$,
- Injection window,
- optional DR bucket numbers.

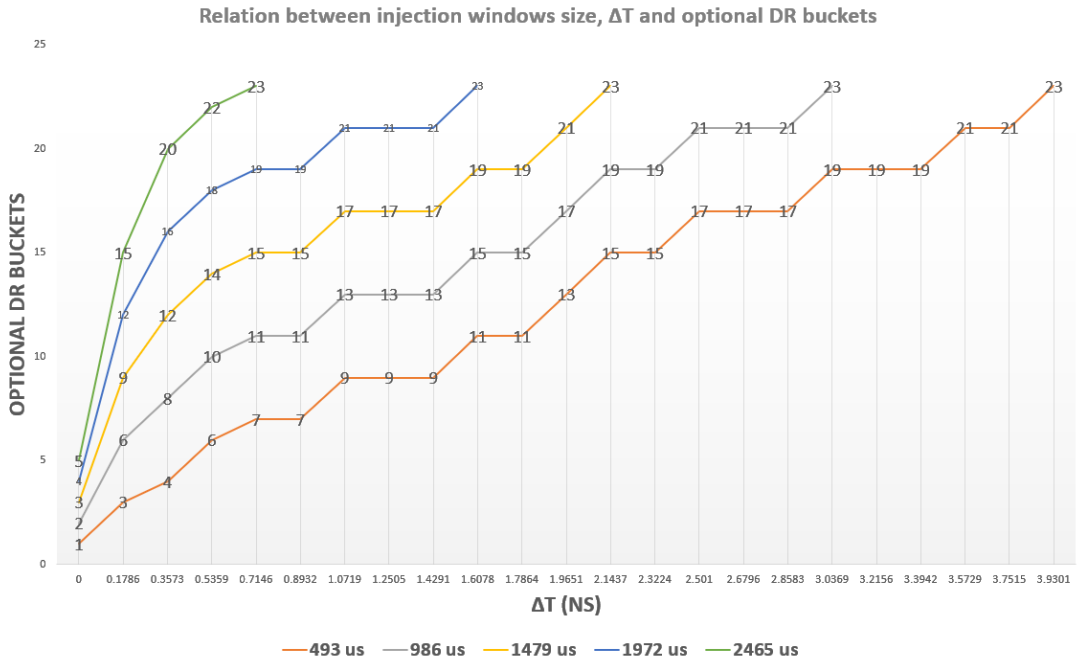


FIGURE 5.13: Optional DR buckets numbers.

Figure 5.13 shows the elective DR RF bucket numbers are affected by $\Delta T$ and injection window size. Five injection window sizes, which include 493 $\mu$s, 986 $\mu$s, 1479 $\mu$s, 1972 $\mu$s and 2465 $\mu$s, are displayed. The source data can be acquired in Appendix A.2.

The time difference $\Delta T$ between DR/LER RF phase and event clock is inevitable if the "downstream LINAC" RF phase is shifted. Most hardware at "downstream LINAC"

accepts the time difference and for those needing high precision trigger signal, the fine delay output channel of EVR must be used to provide 20 times finer delay than the 114.24 MHz event clock. Apart from the trigger signal, the impact on beam energy and injection efficiency must be considered. By increasing $\Delta T$, the coincidence points between DR and LINAC increase. But the time difference between beam trigger and event timing signal is also enlarged.

Other elective DR buckets can be acquired if we add or subtract some BSC cycles for LER (i.e., 493 $\mu$s). For example, Fig. 5.11 shows that DR RF bucket "#120" can be used to inject into LER RF bucket "#0" after RF phase shift. Meanwhile, DR bucket "#70" is also optional if we wait for 493 $\mu$s, and bucket "#170" is optional if the trigger starts 493 $\mu$s earlier. Since the injection window restriction is 2 ms, four DR RF buckets distributed in four cycles are all optional. However, the larger the injection windows are, the more severe the injection trigger fluctuates.

To inject into the same LER RF bucket, 23 DR RF buckets can be used in total. Four DR buckets are elective without RF phase shift or with RF phase shift. All the non-repetitive buckets consist of the optional DR buckets list. The perfect situation is that all 23 DR buckets are elective. The bucket restriction for 2-bunch and 2-pulse operations is 31. That means if we want to select one of the DR buckets locates inside the 31 buckets range, the optional buckets should have a bucket distance of at least 30.

Considering all the three factors, the optional RF phase types are listed in Table 5.3 and Table 5.4. To simplify the explanation, the calculation is based on the injection point of LER bucket "#0" through DR bucket "#0". Table 5.3 shows all the RF shift types with the restriction of 2.144 ns maximal $\Delta T$ value. The $\Delta T$ of RF shift types between "#0" and "#18" are less than 1.608 ns while the last 6 RF shift types are larger than 1.608 ns. Since the RF phase shift itself will generate a variation at a size of 493 $\mu$s, the maximal injection window becomes 1476 $\mu$s. If we want to select all 23 combinations in one pulse, the $\Delta T$ of 2.144 ns becomes necessary. The advantage of selecting all 23 combinations in one pulse is that we can separate the DR injection pulse and extraction pulse thoroughly. The DR extraction delay timing is calculated in the extraction pulse rather than during the injection pulse and the maximal DR storage time limit is removed.

Table 5.4 shows all the optional DR buckets under different RF phase shift. The "nearest cycle" represents the 493 $\mu$s cycle that is nearest to the AC50 and "Cycle-1" means one

| **RF Shift Type** | **Bucket Offset** | **Event Clock Offset** | $\Delta T$ [ns] |
|---|---|---|---|
| 0 | +0 | +0 | +0 |
| 1 | +4 | +1 | -0.893196 |
| 2 | +5 | +1 | +1.07183 |
| 3 | +9 | +2 | +0.178639 |
| 4 | +13 | +3 | -0.714556 |
| 5 | +14 | +3 | +1.25047 |
| 6 | +17 | +4 | -1.60775 |
| 7 | +18 | +4 | +0.357278 |
| 8 | +22 | +5 | -0.535917 |
| 9 | +23 | +5 | +1.42911 |
| 10 | +26 | +6 | -1.42911 |
| 11 | +27 | +6 | +0.535917 |
| 12 | +31 | +7 | -0.357278 |
| 13 | +32 | +7 | +1.60775 |
| 14 | +35 | +8 | -1.25047 |
| 15 | +36 | +8 | +0.714556 |
| 16 | +40 | +9 | -0.178639 |
| 17 | +44 | +10 | -1.07183 |
| 18 | +45 | +10 | +0.893196 |
| 19 | +1 | +0 | +1.965115 |
| 20 | +8 | +2 | -1.786468 |
| 21 | +10 | +2 | +2.143762 |
| 22 | +39 | +9 | -2.143762 |
| 23 | +41 | +9 | +1.786468 |
| 24 | +48 | +11 | -1.965115 |

TABLE 5.3: RF bucket offset, event clock offset and $\Delta T$ for different RF phase shift type.

BSC for the LER cycle before. If we set the injection window size as 986 $\mu$s, 19 out of 23 RF buckets can be selected.

| RF Shift Type | Cycle-2 | Cycle-1 | Nearest Cycle | Cycle+1 | Cycle+2 |
|---|---|---|---|---|---|
| 0 | +100 | +50 | +0 | +180 | +130 |
| 1 | +80 | +30 | +210 | +160 | 110 |
| 2 | +190 | +140 | +90 | +40 | +220 |
| 3 | +170 | +120 | +70 | +20 | +200 |
| 4 | +150 | +100 | +50 | +0 | +180 |
| 5 | +30 | +210 | +160 | +110 | +60 |
| 6 | +130 | +80 | +30 | +210 | +160 |
| 7 | +220 | +190 | +140 | +90 | +40 |
| 8 | +220 | +170 | +120 | +70 | +20 |
| 9 | +100 | +50 | +0 | +180 | +130 |
| 10 | +150 | +100 | +50 | +0 | +180 |
| 11 | +30 | +210 | +160 | +110 | +60 |
| 12 | +10 | +190 | +140 | +90 | +40 |
| 13 | +120 | +70 | +20 | +200 | +150 |
| 14 | +220 | +170 | +120 | +70 | +20 |
| 15 | +100 | +50 | +0 | +180 | +130 |
| 16 | +80 | +30 | +210 | +160 | +110 |
| 17 | +60 | +10 | +190 | +140 | +90 |
| 18 | +170 | +120 | +70 | +20 | +200 |
| 19 | +210 | +160 | +110 | +60 | +10 |
| 20 | +60 | +10 | +190 | +140 | +90 |
| 21 | +50 | +0 | +180 | +130 | +80 |
| 22 | +200 | +150 | +100 | +50 | +0 |
| 23 | +190 | +140 | +90 | +40 | +220 |
| 24 | +20 | +220 | +170 | +120 | +70 |

TABLE 5.4: Optional DR buckets for different RF phase shift type.

# Chapter 6

# Reliability Analysis of Timing System

## 6.1 System Requirements

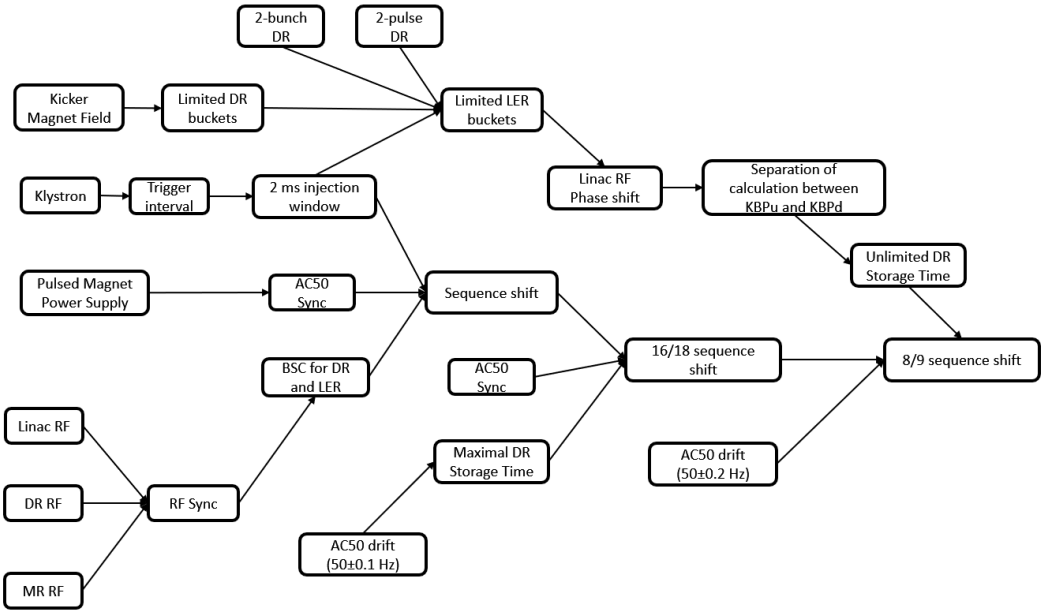


FIGURE 6.1: Timing system requirements.

We have introduced the function requirements of the timing system at LINAC and the architecture of timing system implementation. The overview of system requirements is summarized in Fig. 6.1. The AC50 synchronization requirement brings the sequence shift method which compensates for the effect of AC50 drift, and the sequence length is decided to be 16 and 18 owing to mildly AC50 drift. Another limit caused by bucket selection in DR 2-bunch and 2-pulse operation can be solved by RF phase shift in downstream LINAC. By applying the RF phase shift, the dependency between DR injection and LER injection is removed and consequently, the maximal DR storage time limit is removed. It increases the reliability to switch the sequence length from 16/18 to 8/9 since the compensation frequency for AC50 becomes twice fast.

The system requirements that originate from hardware and software-based implementations which include PPM, sequence shift, and bucket selection eventually increase the system complexity. Long-term stability is a crucial factor for a reliable timing system at LINAC.

The timing system, which satisfies the requirements to operate the DR for the positron injection, was installed and commissioned in 2018 [46]. As the growth of the system complexity comes from the bucket selection and 16/18-pulse sequence shift, several failure modes of the timing system are observed. An event code log system, which monitors and saves all event codes received in EVR, is developed to diagnose the failure modes in 2019 [65]. The severity of some timing system failures is minimal because the trigger signals for devices are masked and inhibited by beam gate system [56] when some abnormal events are transmitted. On the other hand, a timing system failure that stops the delivery of event codes for a few minutes is severe for physics runs because it usually triggers the beam abort system to dump all the beams at SuperKEKB. It normally takes 10 minutes for the operator to check the status of the accelerator and restart the injection. Thus, it is urgent and significant to understand the failure cause and stabilize the operation. To further analyze the failure mode and failure mechanism, data acquisition of timing system is developed to diagnose the system and identify the failure cause.

## 6.2 Data and Information Acquisition

Failure location identification and failure data monitoring are the fundamental concerns when performing failure mode analysis. The event code log system is beneficial to understand what happens during the failure.

### 6.2.1 Event Code Log

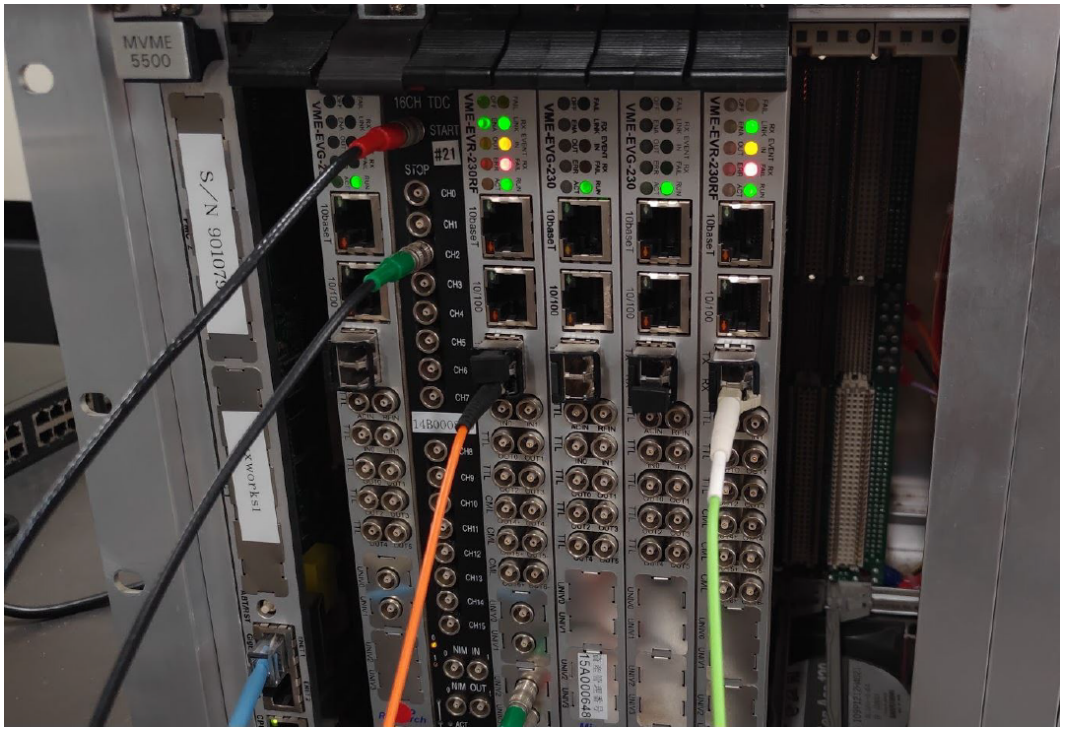


FIGURE 6.2: Two EVRs are used for event code log.

The most intuitive method for understanding the failure mechanism of event delivery is to log all the event codes and timestamps in local EVR. Since two sets of event codes are transferred to upstream LINAC and downstream LINAC hardware, two local EVRs, i.e., upstream EVR and downstream EVR are necessary to completely monitor the event code delivery status. Figure 6.2 shows the hardware of the event code log system. It consists of the MVME-5500 on-board CPU controller with the operation system of VxWorks 6.8.3 and two VME-EVR-230-RF modules from the MRF company.

The EPICS-based timing system allows the operator to modify the timing parameters and monitor system status remotely. The device support for MRF event timing modules called “mrfioc2” is maintained by the EPICS community and provides the interface

between hardware and EPICS record. For example, the delay time and width for the output pulse of an EVR can be changed through "Channel Access" commands. The event codes received in an EVR are put into the event FIFO memory with the 64-bit timestamp information. The 80-bit wide FIFO can hold up to 511 events. The driver program of "mrfioc2" writes event code from the FIFO into the "VAL" field of an EPICS record and sets the "TIME" field of the record as the timestamp from the register upon the trigger of the VME interrupt generated by EVR. This record can be monitored through the "camonitor" command.

The difficulty to log all the event codes through the record provided by "mrfioc2" lies at the processing speed of CA transmission. The minimal interval between event codes is 8.75 ns since the event clock is 114.24 MHz. According to the IOC performance measurement in cite2005xuRealTimePerformance, the latency of EPICS IOC is at the microsecond level. Thus, it is reluctant for event code logging by directly monitoring the EPICS IOC. Another architecture for CA-based event code log system is described in Fig. 6.3. By grouping the event codes into a "waveform" record, the CA transmission interval is enlarged. Every time the record triggered by EVR is processed, it sends the event code and timestamp to the "waveform" record. To store the event code and timestamp information inside the "waveform" record, the EPICS device driver is modified. With the help of a new device driver, the "waveform" record, which contains 1600 sets of event code and correspondent timestamp, is processed every 5 seconds. Then all values are received through "camonitor" at the CA client side. After the elimination of duplication, the event codes and timestamp are saved to disk and successfully logged.

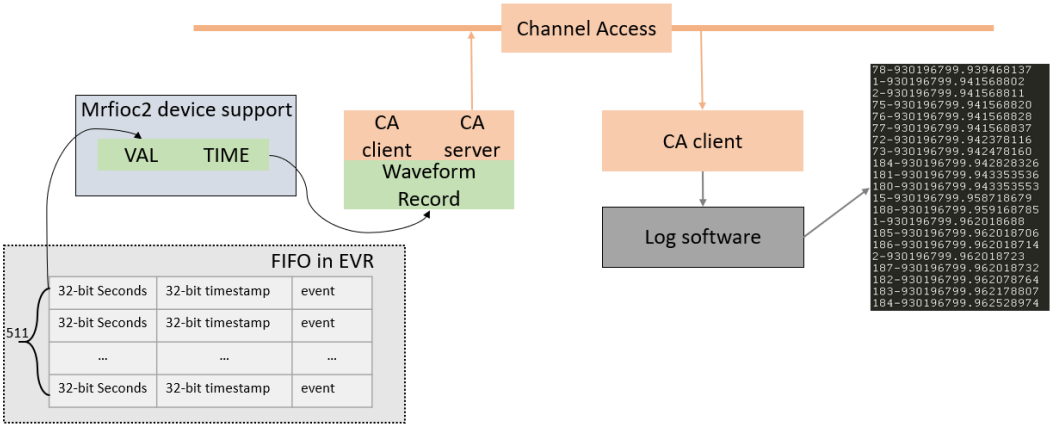


FIGURE 6.3: Architecture of CA-based event code log system.

However, data loss was found in the client during periodically scanning of the "waveform" record. The reason comes from the high CPU load according to Fig. 6.4. The scan-5 task is responsible for the "waveform" record processing and the delay for this task is around 4.5 ms. In other words, if the delay of the scan-5 task is longer than 5 s, the "waveform" record wound is not scanned and event codes are lost in the client [66].

| NAME | ENTRY | TID | PRI | STATUS | PC | SP | ERRNO | DELAY |
|---|---|---|---|---|---|---|---|---|
| tJobTask | 1ce564 | 4db1d0 | 0 | PEND | 24ec6c | 4db0f0 | 0 | 0 |
| tExcTask | 1cd904 | 302970 | 0 | PEND | 24ec6c | 302870 | 0 | 0 |
| tLogTask | logTask | 4de570 | 0 | PEND | 24ce28 | 4de430 | 0 | 0 |
| tNbioLog | 1cf238 | 4e1ea0 | 0 | PEND | 24ec6c | 4e1d80 | 0 | 0 |
| tShell0 | shellTask | 5f7d60 | 1 | PEND | 24ec6c | 5f7a30 | 0 | 0 |
| tShellRem6> | shellTask | 614790 | 1 | READY | 257338 | 612990 | ad0007 | 0 |
| ipcom_tick> | 261900 | 5bb410 | 20 | DELAY | 25615c | 5bb390 | 0 | 91 |
| tNet0 | ipcomNetTask | 4e6fc0 | 50 | READY | 24ec6c | 4e6eb0 | 3d0001 | 0 |
| ipcom_sysl> | 17af48 | 5a2670 | 50 | PEND | 24f588 | 5a24c0 | 0 | 0 |
| ipcom_teln> | ipcom_telnet | 5dcb70 | 50 | PEND | 24ec6c | 5dc970 | 0 | 0 |
| ipsntps | 1bab80 | 5dfd60 | 50 | PEND+T | 24ec6c | 5dfbe0 | 3d0004 | 519514 |
| ipcom_teln> | ipcom_telnet | 1fffda80 | 50 | PEND | 24ec6c | 1fffd860 | 0 | 0 |
| tStdioProx> | 18186c | 1ffff4b0 | 50 | READY | 24ea64 | 1fffefb0 | 0 | 0 |
| tLogin1fff> | 181af0 | 6034c0 | 50 | PEND | 24f588 | 6033f0 | 0 | 0 |
| tPortmapd | portmapd | 5e3d10 | 54 | PEND | 24ec6c | 5e3ac0 | 16 | 0 |
| EVRFIFO | af4d00 | 634b60 | 109 | READY | 24ce28 | 634980 | 0 | 0 |
| EVRFIFO | af4d00 | c00ed0 | 109 | READY | 24ce28 | c00cf0 | 0 | 0 |
| cbHigh | af4d00 | 74c7b0 | 128 | PEND | 24ec6c | 74c690 | 0 | 0 |
| timerQueue | af4d00 | 6f73b0 | 129 | PEND | 24ec6c | 6f7230 | 3d0004 | 0 |
| scanOnce | af4d00 | 7df930 | 132 | PEND | 24ec6c | 7df800 | 0 | 0 |
| scan-0.1 | af4d00 | 80f250 | 133 | PEND+T | 24ec6c | 80f090 | 3d0004 | 28 |
| scan-0.2 | af4d00 | 808730 | 134 | PEND+T | 24ec6c | 808570 | 3d0004 | 128 |
| cbMedium | af4d00 | 743f90 | 135 | PEND | 24ec6c | 743e70 | 0 | 0 |
| scan-0.5 | af4d00 | 801c10 | 135 | PEND+T | 24ec6c | 801a50 | 3d0004 | 26 |
| scan-1 | af4d00 | 7fb0f0 | 136 | PEND+T | 24ec6c | 7faf30 | 3d0004 | 80 |
| scan-2 | af4d00 | 7f45d0 | 137 | PEND+T | 24ec6c | 7f4410 | 3d0004 | 1579 |
| scan-5 | af4d00 | 7edab0 | 138 | PEND+T | 24ec6c | 7ed8f0 | 3d0004 | 4579 |
| scan-10 | af4d00 | 7e6f90 | 139 | PEND+T | 24ec6c | 7e6dd0 | 3d0004 | 9579 |

FIGURE 6.4: VxWorks task delay information.

The overhead for CA is too high. To tackle this problem, we decide to modify the "mrfioc2" driver by adding a new larger buffer to perform the time-memory trade-off [67]. A new VxWorks task called "evtlog" is also created to directly write the event codes to disk rather than through CA to decrease the computation time and network connection cost. One task created by the original "mrfioc" driver reads the event code and timestamp from EVR FIFO and puts them into an "epicsRingBuffer". Then all the contents inside the "epicsRingBuffer" are drained out by the "evtlog" task to disk. The CPU load through the low-level interface method is dramatically decreased and all event codes are logged without data lost.

The source code of this modification can be referred to from [68]. This event code log system works well after the deployment in June 2019 and event codes information for both upstream LINAC and downstream LINAC can be fully stored to disk. The event log system is important for us to locate the error of timing signals and help up to summarize the failure modes.

### 6.2.2 AC50 Log

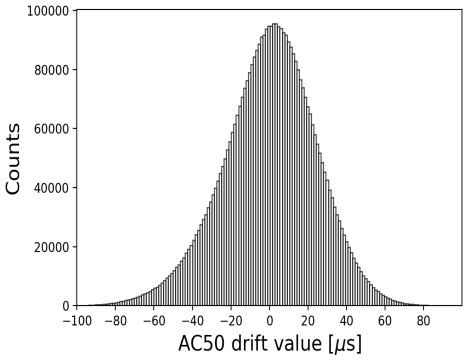


FIGURE 6.5: Histogram of AC50 drift value in 24 hours.

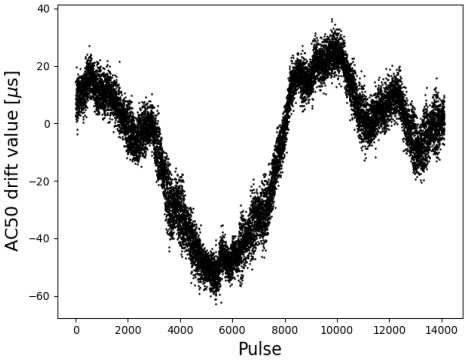


FIGURE 6.6: AC50 drift value in ∼5 minutes.

According to the Tokyo Electric Power Company, the AC power line used at KEK fluctuates within 50±0.2 Hz (i.e., AC50 fluctuates within ±80 $\mu$s) to balance the supply and demand requirement of the electricity market [69]. Since the sequence shift also uses AC50 arrival timing as the reference, we need to understand the arrival timing of AC50 and deduce the procedure inside one pulse.

The AC50 log system is much easier than the event code log since the update frequency (50 Hz) is relatively slow. As a result, EPICS CA is stable enough to monitor the AC50 arrival timing. The AC50 arrival time in a pulse is measured by TDC and saved in an EPICS "waveform" through the device driver program. The length of this "waveform" is 64 to hold 16 channels stop signal and 4 measurements for each channel. A python client program is developed to save the TDC measurement results for every pulse.

Based on the AC50 log, the status of AC50 drift is visualized in Fig. 6.5 and Fig. 6.6. The drift value of less than 80 $\mu$s is observed.

The AC50 log is also connected with the LINAC operation log by monitoring the abnormal AC50 value. If such an error is observed, a warning message is written into the operation log database to help the operator understand the situation.

## 6.3 Failure Mode of Timing System

The event code log and AC50 log record the significant information of the timing system. Based on the analysis of the log data, some abnormal behaviors of the event timing

system are observed [65]. In principle, the event timing system failure modes mainly include,

1. **Event Code Anomaly**. The event codes received at EVR are not as expected. Some of the event codes in a single pulse might be missing or duplicated.

2. **Delay Anomaly**. The time sequence of event codes is wrong. The events are not received at the correct time, which is calculated based on the bucket selection and AC50 phase.

The partition is somewhat rough since both event code and delay could be wrong during the operation (or even worse, the event codes are not sent out). Here we will discuss two representative failure modes.

### 6.3.1 Beam Mode Replacement

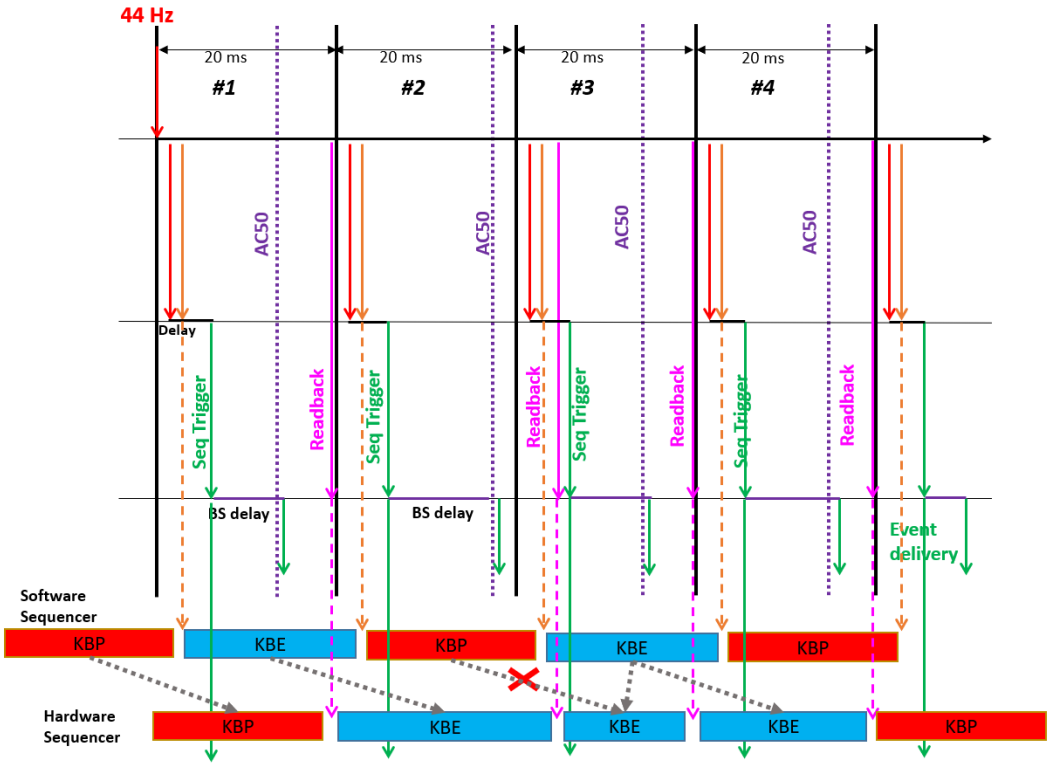


FIGURE 6.7: Failure mode of beam mode replacement.

Figure 6.7 shows the one kind of the failure mode. The beam mode for LER should be transferred in pulse "#3" but beam mode for HER is sent. The contents of "software

sequencer" and "hardware sequencer" are modulated pulse by pulse and the description can be referred to in Section 5.2.

Owing to the drastic drift of AC50 and the shift of 16/18 pulses sequence, the AC50 signal comes very late inside the 50 ms pulse. Thus, the "readback" signal is delayed accordingly. If the "readback" signal comes later than pre-event, the pre-event first changes the "software sequencer" to the value of the next beam mode and then "readback" signal loads "software sequencer" value to "hardware sequencer". Then, the "hardware sequencer" is triggered by the delay of the main event in the same pulse. The overall effect is that the beam mode in pulse "#3" is replaced by pulse "#4".

### 6.3.2 Redundant Beam Mode

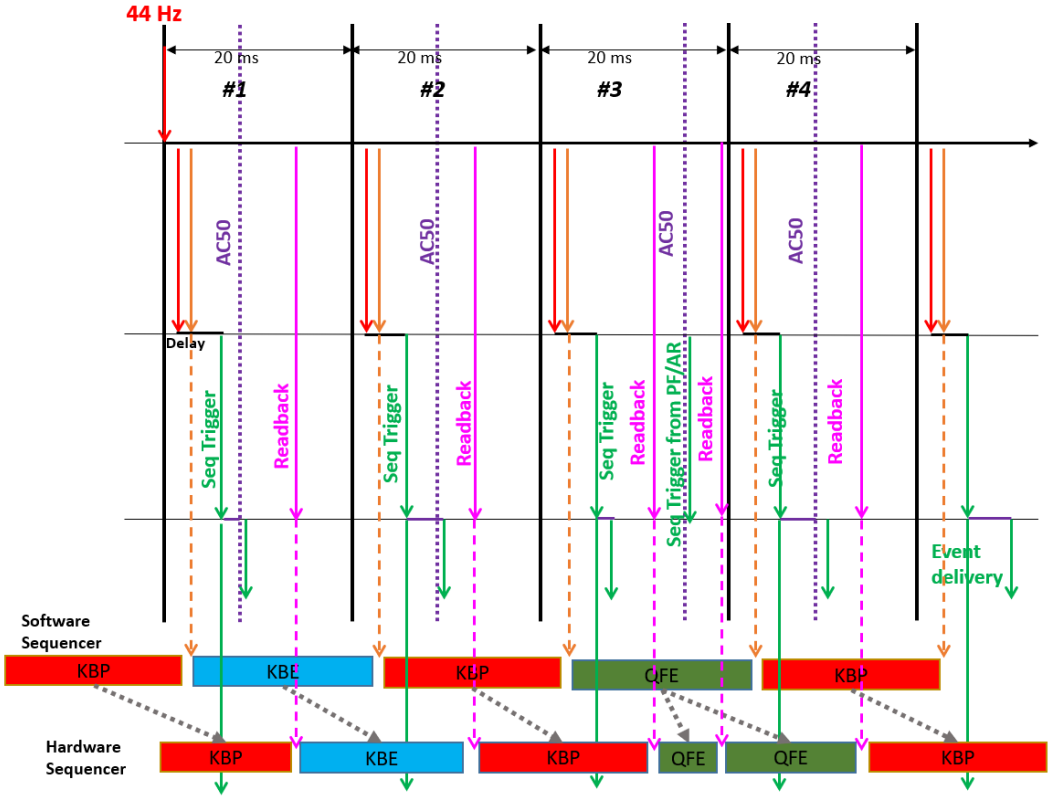


FIGURE 6.8: Failure mode of beam mode redundancy.

When the event code log is checked, sometimes an extra beam mode of PF/PF-AR is inserted between LER mode and a PF/PF-AR mode. As Fig. 6.8 shows, the LER "readback" signal in pulse "#3" comes too early and causes the "hardware sequencer" change the beam mode and trigger source to the next pulse, i.e., PF beam mode. Note the "hardware sequencer" trigger source for LER comes from the main event in middle

EVR and for PF the source is obtained from the change coincidence between PF revolution frequency and LINAC RF frequency. Consequently, the "hardware sequencer" is triggered twice in a single pulse.

This failure mode is induced by abnormal bucket selection delay and the failure cause comes from the software bug in the bucket selection algorithm or injection pattern switch. The mechanism of the latter is explained in Section 6.4.2.

## 6.4 Failure Mechanism and Failure Cause

### 6.4.1 AC50 Drift

The failure beam mode replacement is mainly caused by undesirable AC50 arrival timing. Thus, the AC50 drift speed and the AC50 drift tolerance of the sequence shift algorithm are investigated to understand the failure mechanism.

According to the AC50 log, the status of AC50 fluctuation can be visualized. Two situations of the drift speed of AC50 are shown in Fig. 6.9 and Fig. 6.10. The horizontal axis stands for the AC50 drift value and the vertical axis represents the time of occurrence. In most situations, AC50 drifts mildly in 50±0.1 Hz, i.e., 40$\mu$s in 20 ms.

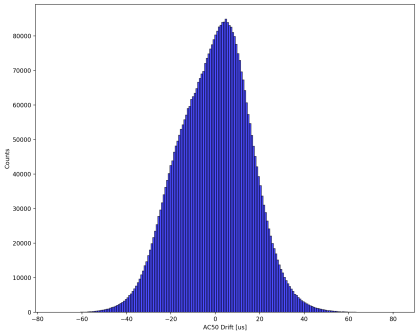


FIGURE 6.9: AC50 drifts mildly in 24 h.

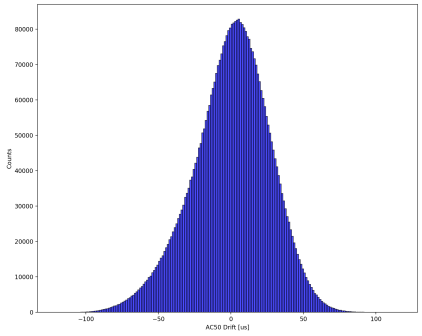


FIGURE 6.10: AC50 drifts strongly in 24 h.

The timing of the AC50 position in a pulse can be acquired from the AC50 log. As Fig. 6.11 shows, the AC50 arrival timing chart shows that AC50 might come late when strong AC50 fluctuation happens.

Since the estimated AC50 is used in the sequence shift algorithm to judge the sequence type of the next pulse. The estimated AC50 is different from the real AC50, and the

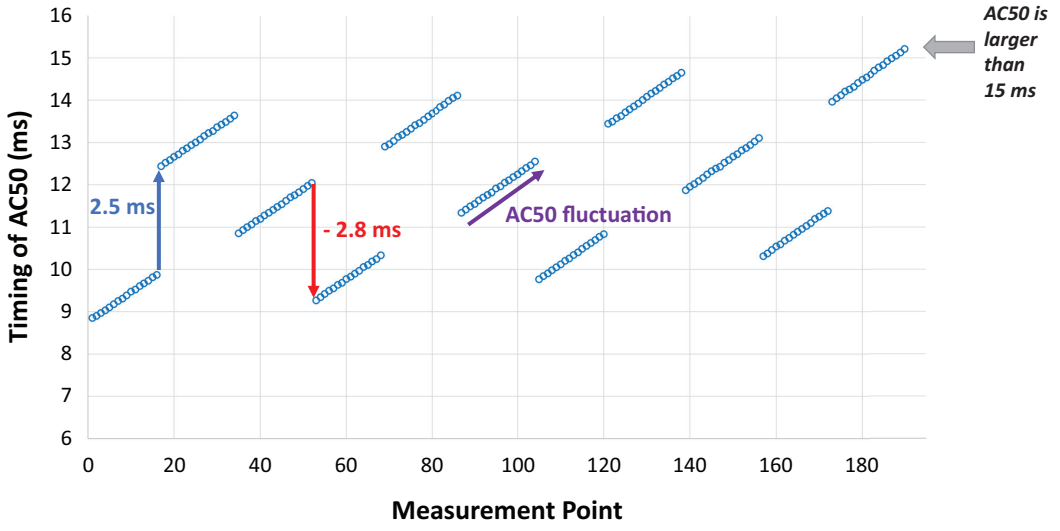


FIGURE 6.11: Drift of AC50.

discrepancy becomes larger when AC50 drifts drastically. Table 6.1 compares the ideal and real cases. The reference value for sequence shift algorithm $T_{ref}$ is set to 10 ms as it is easy for calculation.

For example, the AC50 arrival timing of the first pulse in sequence #1 $X_1$ determines the type of sequence #2 $S_2$ by calculating estimated value $E_2$. Since $E_2$ is 9.9 which is smaller than $T_{ref}$, the sequence type of #2 is decided to be 2.5, the AC50 should jump up 2.5 ms in sequence #3. This decision works well for mildly AC50 drift or without AC50 drift. However, if AC50 drifts for 60 $\mu$s per pulse, $E_2$ is far away from the real AC50 value. The AC50 fluctuation is then reflected at the end of sequence #3, where the AC50 drift becomes 15.6 ms, which enters the race condition. If the timing system goes into the race condition, then the normal processing logic is messed up and the various abnormal situation will appear.

| **Sequence #** | **Without AC50 drift** | | | | **With AC50 drift** | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_n$ | $X_n$ | $Y_n$ | $E_{n+1}$ | $S_n$ | $X_n$ | $Y_n$ | $E_{n+1}$ |
| 1 | -2.8 | 12.7 | 12.7 | 9.9 | -2.8 | 12.7 | 13.8 | 9.9 |
| 2 | 2.5 | 9.9 | 9.9 | 12.4 | 2.5 | 11.1 | 12 | 13.6 |
| 3 | -2.8 | 12.4 | 12.4 | 9.4 | -2.8 | 14.5 | 15.6 | 11.7 |
| 4 | 2.5 | 9.4 | 9.4 | 11.9 | -2.8 | 12.9 | 14.8 | 10.1 |
| .. | .. | .. | .. | .. | .. | .. | | |

TABLE 6.1: Analysis of the decision making of the sequence shift.

To quantify the possibility of the relationship between timing system error and AC50 drift, the limit of the race condition is chosen to be less than 4.5 ms and larger than 15

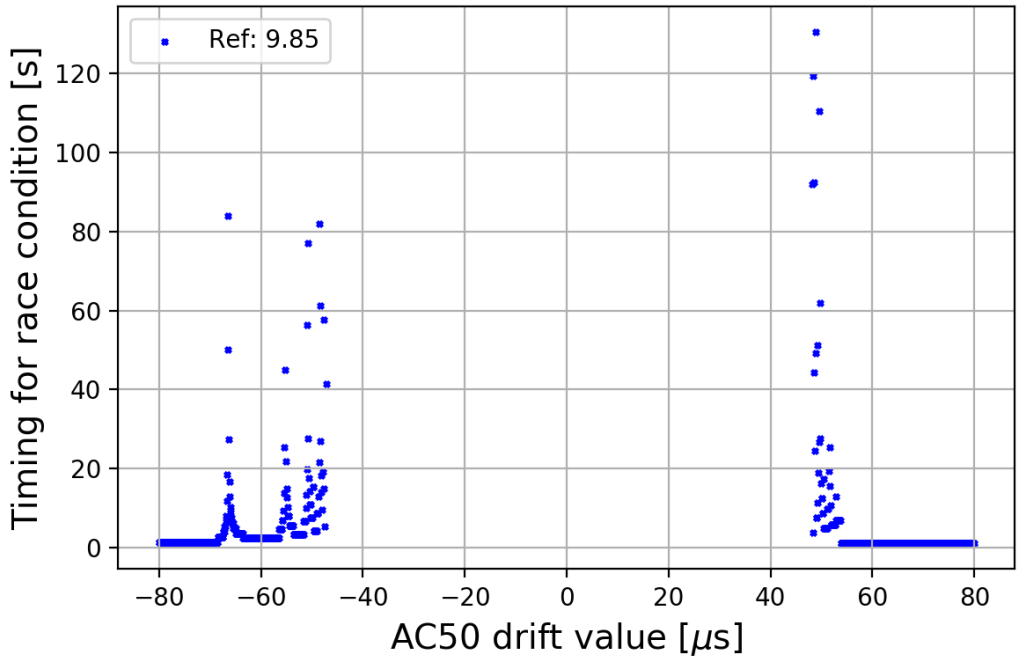


FIGURE 6.12: The relation between time to failure and of extend of AC50 drift for 16/18 pulses sequence shift.

ms, which is decided based on the operational experience. According to the algorithm, we can simulate the process of a sequence shift using computer code. Figure 6.12 shows the simulation result of 16/18-pulse sequence shift. The initial AC50 arrival timing is 10 ms, and $T_{ref}$ is 9.85 ms. If $|\Delta_{AC}| <= 40\mu$s, the 16/18-pulse sequence shift can always compensate for the AC50 drift, and race conditions will not happen. While $\Delta_{AC}$ is ∼45 $\mu$s, the timing system goes into race condition after ∼130 s. If $\Delta_{AC}$ becomes larger, e.g., 60 $\mu$s, the timing for race condition only requires ∼0.6 s. Note that the figure is asymmetric because both the sequence shift value (2.5 and 2.8 ms) and boundary for race conditions (4.5 and 15 ms) are different. The source code of simulation can be referred to in Appendix A.3.

Similarly, for 8/9 pulses sequence shift, the tolerance of AC50 drift improves as shown in Fig. 6.13. The threshold for AC50 drift becomes ∼120 $\mu$s.

### 6.4.2 Injection Pattern Switch

We have mentioned that the failure mode of the redundant beam mode is caused by an abnormal bucket selection delay. The program bug for bucket selection is one of the possibilities since the bucket selection program needs too many conditions to handle.

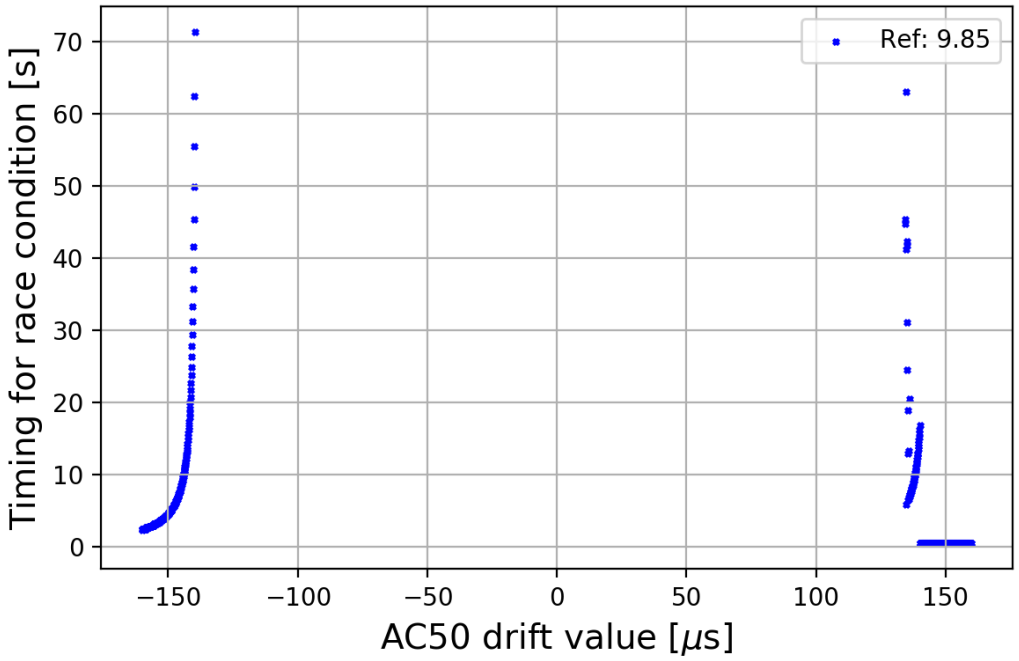


FIGURE 6.13: 8/9 pulses sequence shift method is able to handle lager AC50 drift value.

And that is the reason why the bucket selection log is planned to quickly diagnose the program and fix the bug.

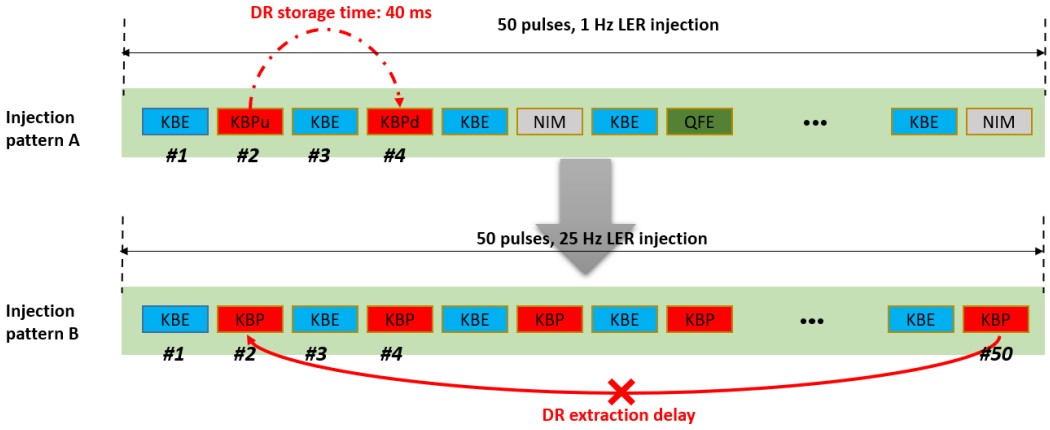


FIGURE 6.14: Injection pattern switch error caused by DR operation.

Apart from the random error during the program running, another kind of bucket selection delay error is caused by the injection pattern switch. As the Fig. 6.14 shows, the injection pattern switches from "injection pattern A" to "injection pattern B". Both patterns constitute 50 pulses.

The "injection pattern A" performs 1 Hz LER injection by setting beam mode of pulse "#2" and pulse "#4" to KBPu and KBPd, respectively. In other words, pulse "#2"

injects positron beam into DR, and pulse "#4" extract the beam to LER.

The "injection pattern B" operates at a higher LER injection repetition rate, i.e., 25 Hz. Every pulse for LER combines KBPu and KBPd which means both extraction and injection happen in the KBP pulse. The extraction bucket selection delay for pulse "#4" is decided in pulse "#2". Similarly, the beam injected in pulse "#50" should be extracted in pulse "#2". However, at the initial period of "injection pattern B", the extraction delay remains unknown. There are two possibilities to set the extraction delay value for pulse "#2",

- Reset the extraction delay value to a default value, e.g., 5 ms, during injection pattern switch.
- Use the extraction delay value of the last injection pattern. Here means the delay value of pulse "#4" of "injection pattern A".

Both situations result in the abnormal bucket selection delay hence the failure mode of redundant beam mode. The root reason for this situation is the cross-pattern dependency of LER injection which means the DR injection pulse and DR extraction pulse occur in a different cycle of injection pattern. This one-pulse error does not affect the beam since there is no beam in DR. However, the trigger signal is delivered to devices like klystron and this trigger might violate the 18 ms trigger interval requirement of the klystron.

As we have summarized in Table 4.4, whether LER injection can be finished in a single cycle of current injection pattern depends on the DR storage time, KBP mode repetition rate, DR 2-pulse storage mode, and length of injection pattern.

## 6.5 Reliability Requirements Evaluation

The reliability requirements of the timing system at KEK LINAC can be evaluated based on how often the failures appear, how long do the outages continue and what is the impact of failures and outages.

Figure 6.12 demonstrates the threshold for risky AC50 drift value is 60 $\mu$s every 20 ms. Therefore, counts of AC50 drift which is larger than 60 $\mu$s and counts of maximal continuous large AC50 drift are shown in Fig. 6.15.

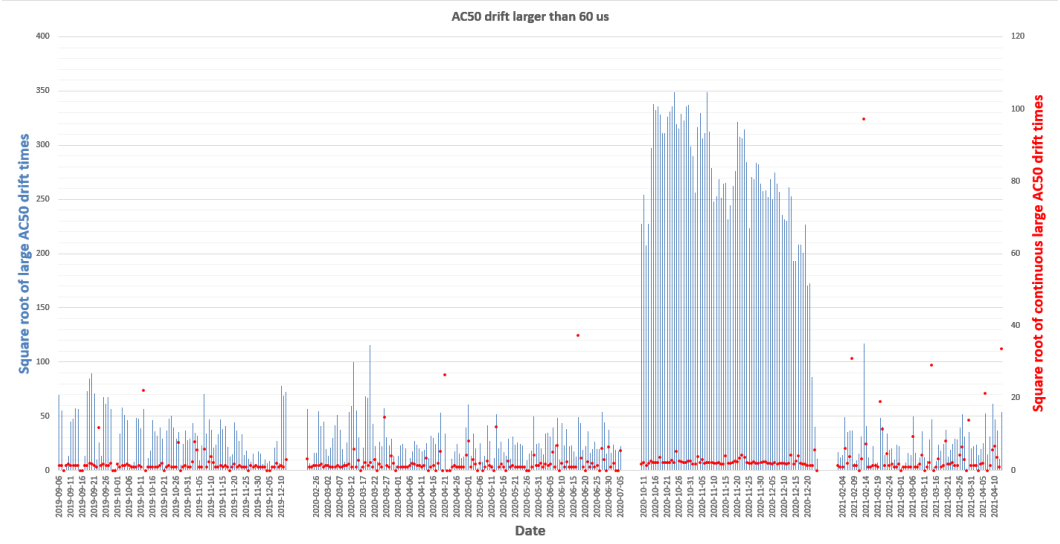


FIGURE 6.15: Counts of large AC50 drift from June, 2019 to April, 2021.

There are many abnormal AC50 drift situations from October 2020 to December 2020 but these drifts were not continuous. These data are thus considered outliers. The counts of maximal continuous large AC50 drift increase from February 2021. The occurrence of such kind of failure is not often (i.e., 9 times) in 2020. However, the number of failures increases to 18 times in a month since the 2021 spring, and the beam operation is frequently interrupted.

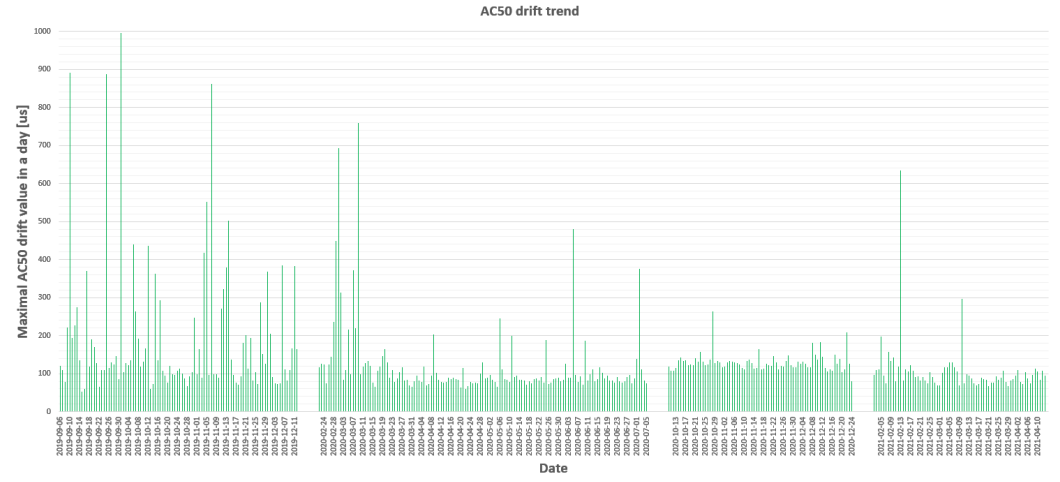


FIGURE 6.16: Maximal AC50 drift value in a day from June, 2019 to April, 2021.

The maximal AC50 drift value in a single day is also displayed in Fig. 6.16. As shown in the figure, the AC50 drifts severely on some days which could cause problems since the timing system relies on the AC50 to function normally.

Different impacts exist for the various timing system failure modes. There is a high possibility that the timing system stops the delivery of the events if the AC50 arrival time is less than 4.5 ms or larger than 15 ms. If this situation happens during the physics run, then the klystron will be down and cause the beam to abort. Another minor failure happens when the bucket selection delay value is wrong. This failure does not affect the beam since either the beam gate is closed or there is no beam in DR. However, the klystron is triggered with an unexpected interval and the DR kicker is blank fired.

# Chapter 7

# Reliability Improvement and Future Prospects

## 7.1 Reliability Improvement

To guarantee a stable timing system and avoid the race condition, the following measurements can be considered.

### 7.1.1 AC50 Independent Operation

An intuitive method is to remove the AC50 dependency since the failure of the timing system is caused by AC50 fluctuation. It is possible to evaluate the performance of significant hardware in different AC50 arrival timing and consider the possibility to replace the hardware that has a strong dependency on AC50; currently, the quality of the power supply has improved significantly, and some accelerator facilities are using AC50-independent devices, for example, the J-PARC timing is independent with AC line [70]. Thus, an experiment is performed to evaluate the effect of AC50-independent operation.

An experiment was conducted by replacing the AC50 trigger from the MTG module with a strictly 50 Hz trigger. The bema position can be measured using BPM. The energy jitter is then calculated through the dispersion function in Eq. 7.1, where $\delta x(s)$ is the horizontal beam position, $D(s)$ is the dispersion function and $\Delta P/P$ represents the energy jitter.

$$\Delta x(s) = D(s)\frac{\Delta P}{P} \tag{7.1}$$

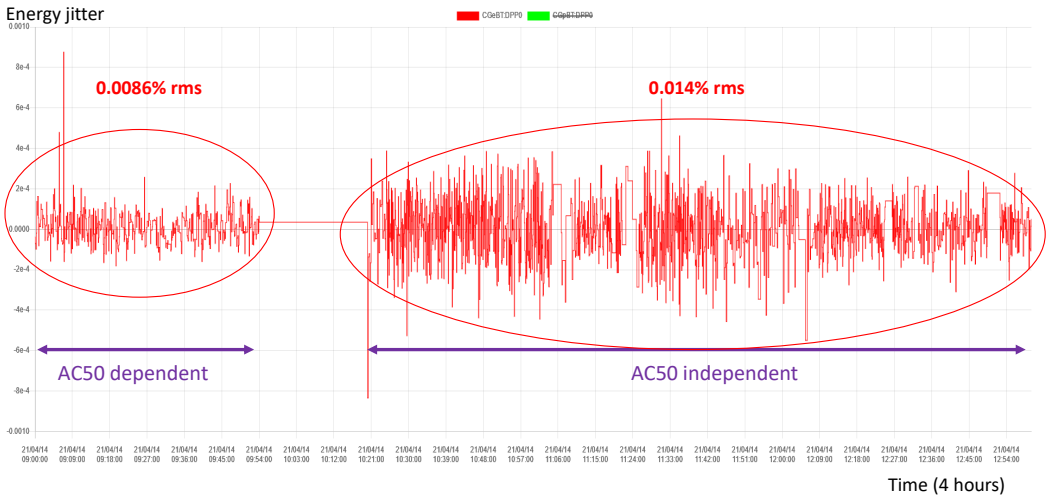


FIGURE 7.1: Change of energy jitter at the beam transport line of LINAC.

After replacing the MTG module with a strictly 50 Hz signal generator, the timing trigger signal is delivered at a different phase of the AC line. The hardware at LINAC works under the AC50-independent mode. The energy jitter of electron bunch at the beam transport line of LINAC is measured and the results are displayed in Fig. 7.1. The average energy jitter for AC50-dependent mode is 0.0086% (r.m.s) and it increases to 0.014% (r.m.s) after switching to the AC50-independent mode. Though the beam quality is indeed related to AC line frequency, the overall energy jitter (0.079%) is still acceptable for SuperKEKB MR since the required energy spread in the current operation stage is 0.1% [71]. Consequently, the injection for SuperKEKB rings can be performed without synchronizing to the AC line.

Another hardware experiment was also done by measuring the klystron output and AC50 timing. Figure 7.2 shows the relation between AC50 and RF power. Still, no strong relation between RF power and AC50 was found.

However, during the experiment, a strong dependency between AC line frequency and the power supply of the injection kicker magnets at PF are observed. The timing trigger

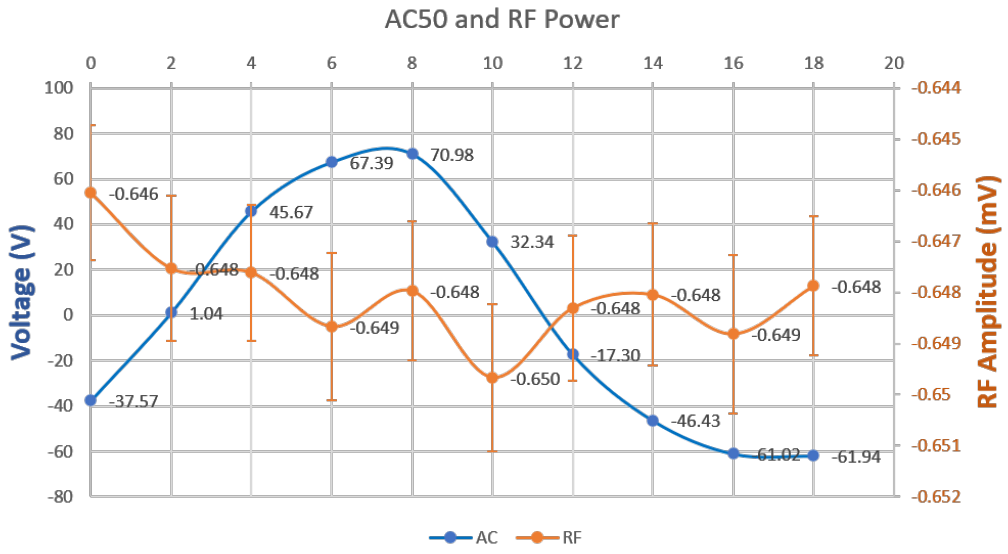


FIGURE 7.2: Relation between klystron output and AC50 arrival timing.

for PF ring injection must synchronize with the AC power line. Figure 7.3 shows the variance between 4 PF kickers.

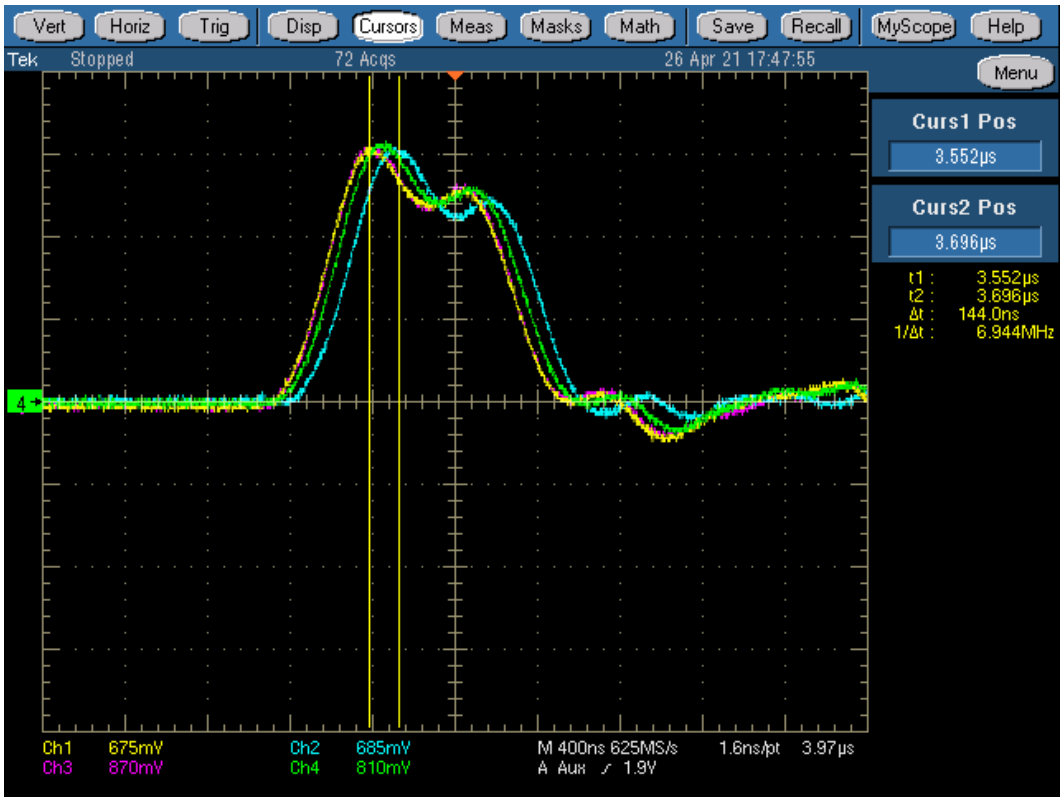


FIGURE 7.3: Schematic diagram of AC50 regulator module.

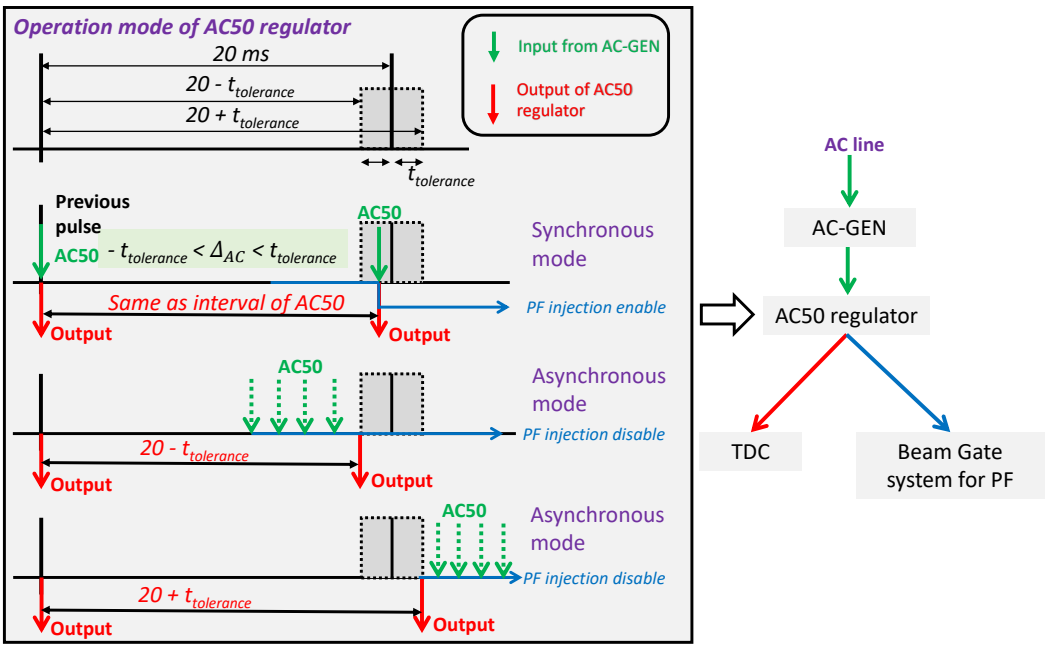


FIGURE 7.4: Schematic diagram of AC50 regulator module.

### 7.1.2 Partially AC50 Independent Operation

Considering that strong AC50 drift occurrence is rather rare according to the data measured by TDC, a CompactRIO-based module called AC50 regulator is designed to switch between the AC50-dependent and AC50-independent modes. As Fig. 7.4 shows, the AC50 regulator module is inserted between the MTG and TDC modules. It supports two operation modes, synchronous mode, an asynchronous mode, which corresponds to AC50-dependent and AC50-independent operation, respectively. Under synchronous mode, the AC50 regulator module directly passes the AC50 signal to the TDC module. On the other hand, the module generates outputs with a fixed interval to TDC when the AC50 drift value is large. The timing system starts to operate under AC50-independent mode in a short period. When the AC50 drift value becomes smaller, the module switches to synchronous mode within several seconds, and the timing system trigger synchronizes with the AC line again.

A parameter called $t_{tolerance}$, which is decided based on the simulation result of sequence shift (see Fig. 6.12), is used to determine the maximal AC50 drift value that the AC50 regulator permits. If AC50 drift value $|\Delta_{AC}|$ is larger than $t_{tolerance}$, the module enters asynchronous mode. The range of output interval is restricted to be $20 - t_{tolerance}$ or $20 + t_{tolerance}$. Meanwhile, the PF injection is disabled by sending a signal to the beam

gate system. Combining the simulation results and data analysis, the value of $t_{tolerance}$ is set to 40 $\mu$s at LINAC. The output interval of the AC50 regulator is within 20±0.04 ms. About 1% pulses are prohibited for PF injection.

### 7.1.3 Performance of AC50 regulator

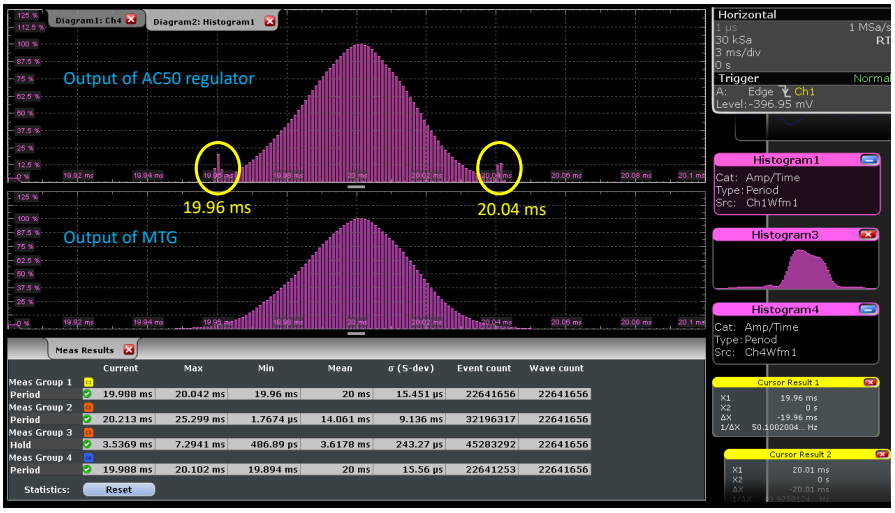


FIGURE 7.5: Comparison of AC50 regulator and MTG output.

The AC50 regulator module is installed and tested in the 2021 spring. Since then, the timing system failure caused by strong AC50 fluctuation never happens. The processing delay of the AC50 regulator is ∼500 ns. The long-term stability of the AC50 regulator module is studied by measuring the output signal interval of the AC50 regulator and MTG module. The histogram shown in Fig. 7.5 indicates that the range of the AC50 regulator output is guaranteed within 20±0.04 ms.

The AC50 regulator must switch back to synchronous mode after strong AC drift stops. There are only theoretical possibilities that the frequencies of AC line and regulator output are the same, though remaining at a different phase. In practice, the AC line always drifts, and it will catch up with regulator output after a short period. According to the data measured by TDC in one month, the average transition time from asynchronous mode to synchronous mode is ∼31 s. Figure 7.6 displays an example of the transition process. The red dots are the arrival time of regulator output while the blue dots are the arrival time of AC50. The asynchronous mode lasts for ∼80 s and it takes ∼20 s to resynchronize with the AC line after strong AC drift stops.

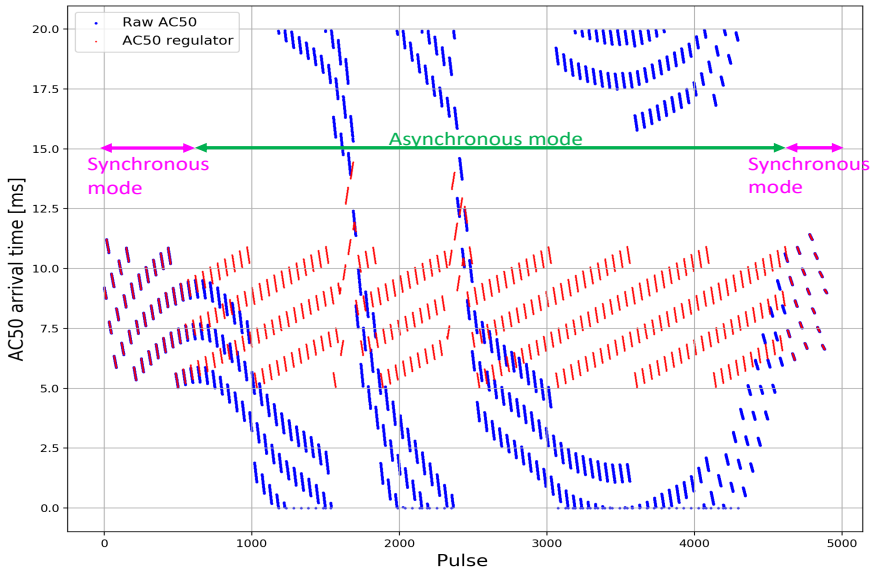


FIGURE 7.6: Resynchronization to AC50 after strong AC50 fluctuation stops.

### 7.1.4 Improvement for sequence shift

The AC50 regulator stabilizes the timing system and reduces the accelerator failure time at LINAC. However, there are still concerns about the degradation of the beam quality. To operate the timing system under AC50-dependent mode, two sequence shift improvements are proposed to optimize the timing system.

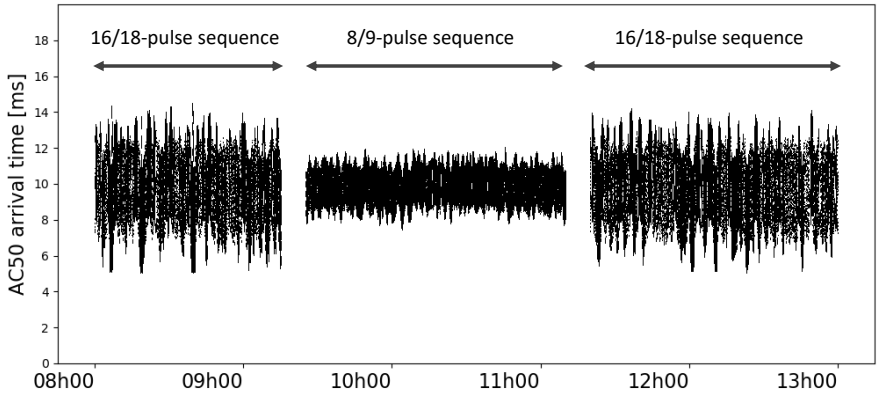


FIGURE 7.7: Comparison of AC50 arrival timing between 16/18-pulse sequence and 8/9-pulse sequence.

As Fig. 7.7 shows, compared with the 16/18-pulse injection sequence, the 8/9-pulse injection sequence increases the robustness of the sequence shift algorithm. Switching to the 8/9-pulse injection sequence is a possible method to solve the timing failure because the AC50 adjustment speed is faster. The restriction of the sequence length originates

from the DR storage time and the root reason is the coupling of DR injection and extraction. The DR extraction delay is calculated at the injection pulse, which results in the extraction timing having a time difference with the drifted AC50. Shifting the RF phase at the downstream LINAC is an efficient way to increase the DR extraction opportunity and relieve the stress of long sequence management. Under these circumstances, the dependency between DR and MR injections can be removed (See Section 5.3 for detail). The operation of an 8/9-pulse sequence shift is possible as the injection and extraction delay calculations can be separated.

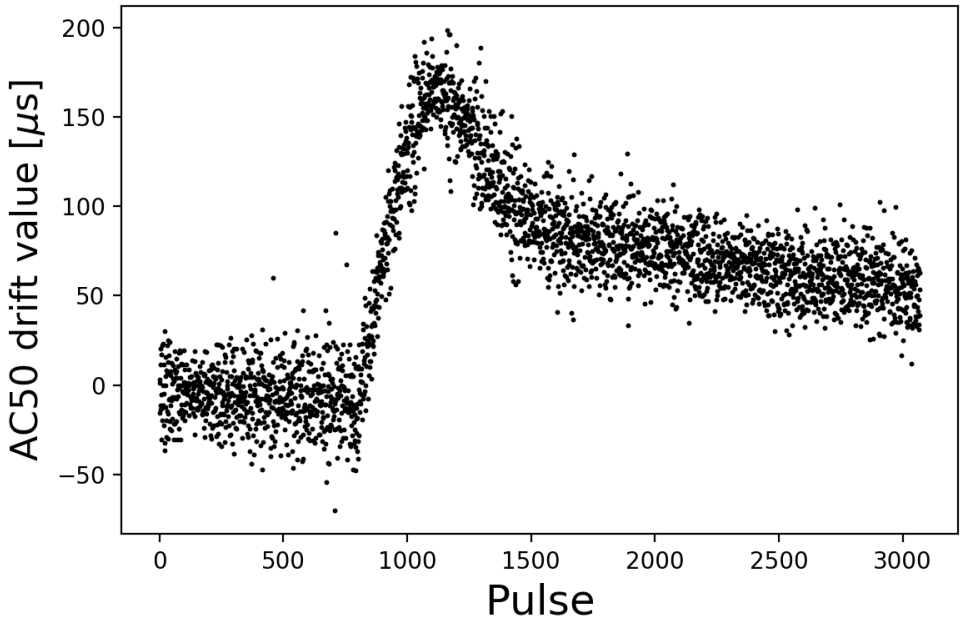


FIGURE 7.8: Extremely strong AC50 drift recorded by TDC.

Apart from the 8/9-pulse sequence shift, the sequence shift algorithm can be further improved by considering the AC50 drift value. Currently, the estimated AC50 arrival time is used to determine the next sequence type. If strong AC50 drift happens, the estimated value has a large deviation from the real value. The timing system could enter race conditions when an inappropriate sequence type is selected. To avoid such a situation, the sequence shift algorithm is modified and the average AC50 drift value in recent pulses is utilized to help the sequence shift algorithm to estimate the AC50 arrival time. Figure 7.8 shows a timing system failure that is caused by the extremely strong AC50 drift. The AC50 drift value reached 120 $\mu$s and lasted for several seconds. Figure 7.9, 7.10, 7.11 compare three sequence shift schemes which include, 16/18-pulse

sequence shift which is currently using, 8/9-pulse sequence shift and 8/9 pulse sequence shift with a functionality of making use of the AC drift value.

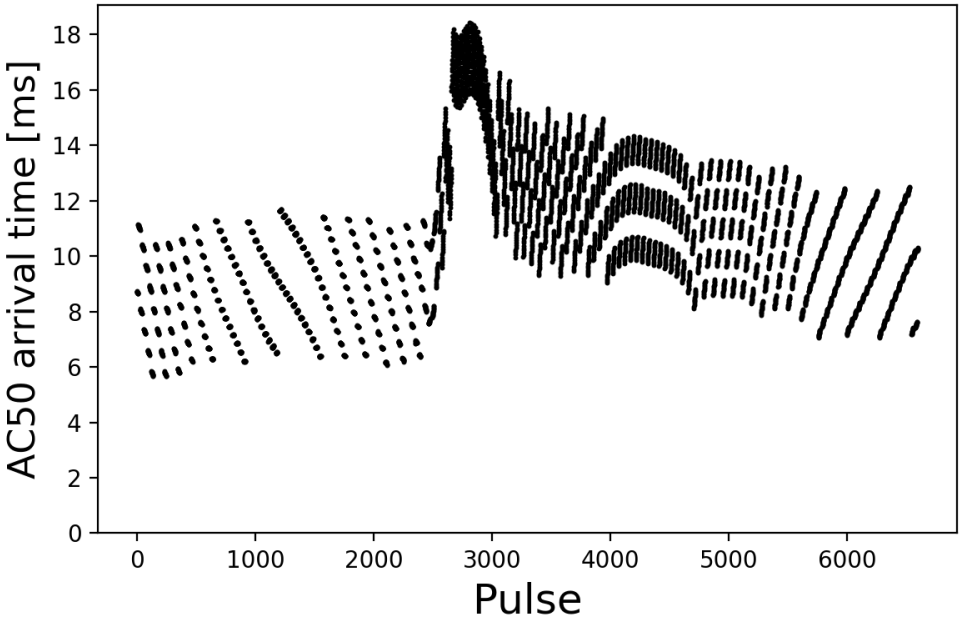


FIGURE 7.9: 16/18-pulse sequence shift data measured by TDC.

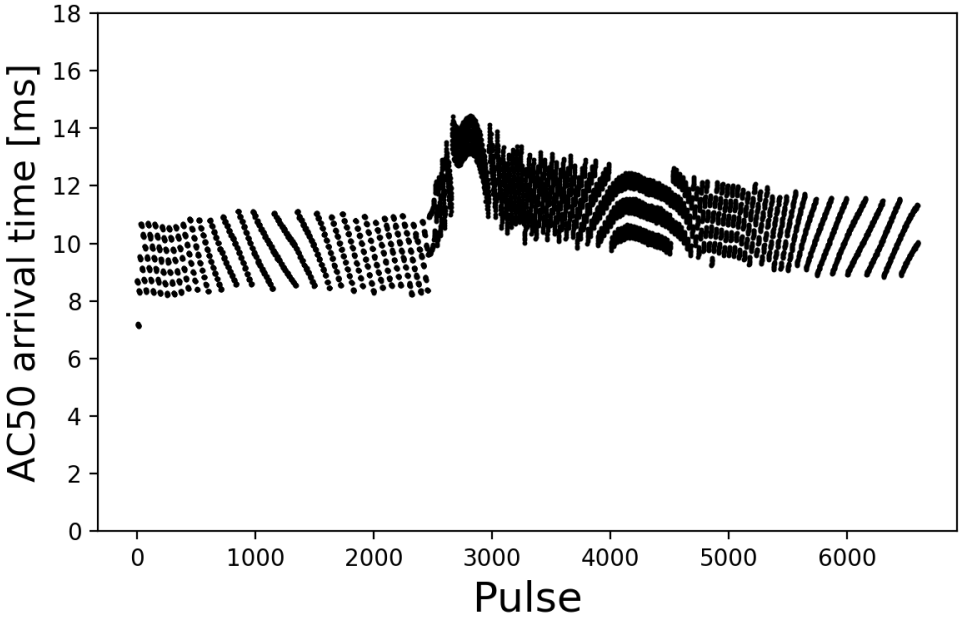


FIGURE 7.10: Simulation of 8/9 pulse sequence shift.

The 8/9-pulse sequence operation with recent AC50 drift value compensation has been planned for 2021 summer.

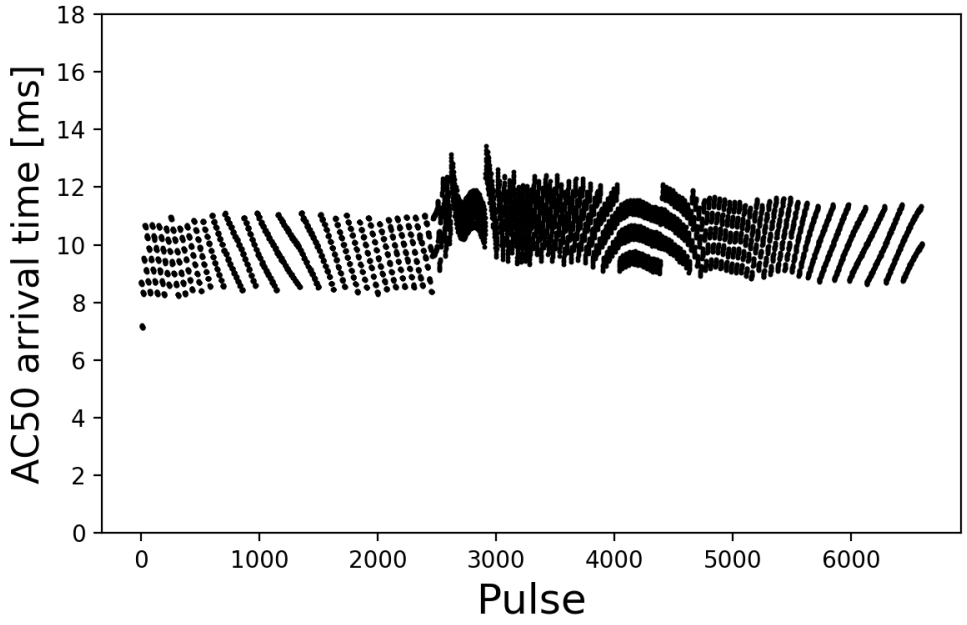


FIGURE 7.11: Simulation of 8/9 pulse sequence shift with considering the AC drift.

## 7.2 Future prospects

### 7.2.1 Log Data Synchronization


FIGURE 7.12: Abort Trigger System log displayed in Grafana.

Apart from the trigger delivery function, the timing system also needs to provide the ability to correlate the log data from different sub-systems. Normally timestamps or a tag called pulse ID are used to identify which pulse the data comes from. Figure 7.12 shows the abort trigger system displayed in Grafana [72], which is a popular dashboard for log data visualization. The abort request timestamp and related pulse ID are recorded for diagnosis purpose [73]. Thus, it is significant to analyze the data based on device log-in during that short period. The timestamp of the abort trigger system is received from MTS and synchronized with the event timing system, and it is simple to identify the event codes through timestamp. However, other log systems are not correlated with the timestamp from event timing. These log systems are listed in Table 7.1.

| **Log System** | **Data Format** | **Tag** |
|---|---|---|
| Abort | Json | EVG timestamp & 16-bit pulse ID |
| Pulsed Magnet | CSV | NTP timestamp & 32-bit pulse ID |
| BPM | Plain text (bz2 compressed) | 32-bit pulse ID |
| RF Monitor | Plain text (bz2 compressed) | 32-bit pulse ID |
| Event Code | Plain text | EVG timestamp |
| Data Buffer | CSV | EVG & NTP timestamp & 32-bit pulse ID |

TABLE 7.1: Tagged data for different log systems.

### 7.2.2 Smooth Pattern Switch

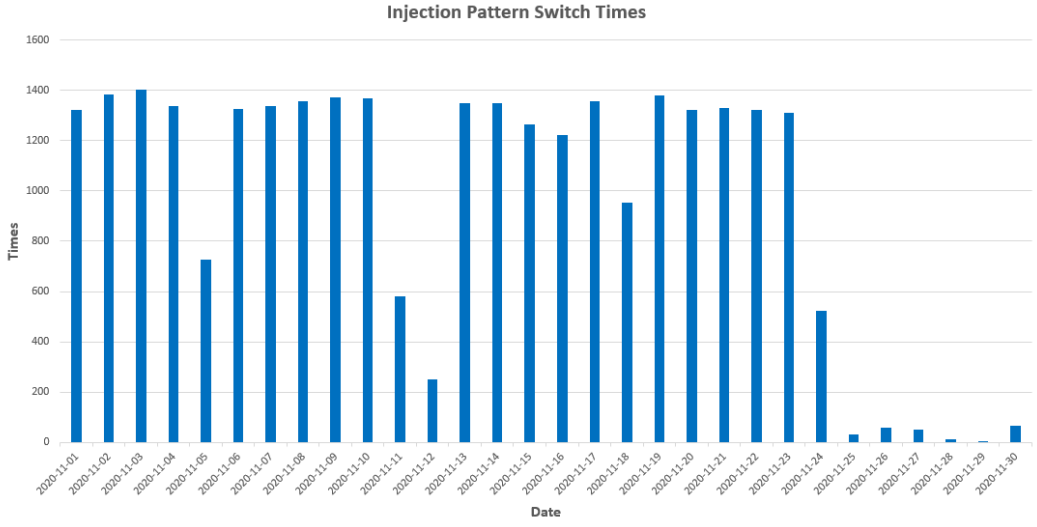


FIGURE 7.13: Injection pattern switch times in November, 2020.

The beam operation must stop during the injection pattern switch period to avoid the abnormal event timing signal is applied to hardware. Though closing the beam gate brutally can avoid bad beam generation, a smooth way should be used to change the

injection pattern reliably. One of the concerns on beam gate closing is that the beam gate closing action is done by the operator. The pattern switch times in November 2020 are shown in Fig. 7.13. The action of thousands of times per day should be manipulated by an automatic program to avoid human error.

Another concern is about the injection pattern switch error caused by DR operation as we have discussed in Section 6.4.2. Though this error does not affect the beam since the beam gate is closed (or since there is no beam in DR, depending on the operation mode), the trigger signal is still delivered to some devices like klystrons and kicker magnets. Thus, the 18 ms klystron trigger interval may be broken. We may consider some methods in the future to avoid this situation. For example, by adding some pseudo pulses during the injection pattern switch to allow the pseudo pulses to perform preparation trigger calculation.

# Chapter 8

# Conclusion

From the demand for stable operation and maintenance, the timing system takes an important role in the accelerator. This thesis mainly introduces the basic parts of the timing system, which include,

- RF synchronization,
- Trigger delivery,
- Bucket selection.

RF synchronization is necessary to inject the beam from LINAC into the storage ring. The relation between LINAC RF frequency and ring RF frequency is also discussed. If these two frequencies match an integer multiple relations, the synchronization is simple and easy to achieve. Otherwise, the greatest common frequency is used to find the coincidence point for injection.

Apart from the synchronization between LINAC and ring, synchronization between multi-rings bring new requirement. These three RF synchronization schemes are compared with the example of SLS timing, BEPC II timing, and SuperKEKB timing. Several concepts about RF frequency synchronization are also introduced, like revolution

frequency and bucket selection repetition rate. These concepts are crucial for those who want to design a timing system or understand the existent timing system.

The goal of the timing system is to provide a precise trigger signal for hardware in a scheduled sequence. The evolution of trigger delivery is introduced based on the historic order. From various kinds of timing modules for different institutes to de-facto standard event modules among accelerator facilities, the timing system becomes much more flexible and scalable. The basic block of EVG and EVR are talked to understand how a timing system in modern accelerator complete the control mission.

One of the most significant targets for a timing system is Bucket selection. There are several schemes to decide which RF bucket should be injected. At SuperKEKB, the "BCE" and "star" schemes are commonly utilized to accommodate the physics run. After the RF bucket number is determined, the bucket selection delay should be calculated and set at EVG. The delay calculation for the selected RF bucket should base on a fiducial point. Usually, the revolution frequency functions as the fiducial point. Arbitrary RF buckets can be filled through the revolution frequency fiducial and bucket delay value.

Recently, another timing system implementation (i.e., White Rabbit project) rather than a traditional event-based timing system is developed from CERN. The timestamp-based timing system provides other thoughts to coordinate the devices. Several key technologies, like frequency synchronization through Sync-E protocol and PHY, timestamp synchronization through IEEE-1588, are also introduced. The precision of a timestamp-based timing system is nearly the same as an event-based timing system which provides an extra option to build a timing system. Furthermore, the timestamp-based timing system is inherent in the ability to perform log data synchronization while an extra tag is needed for an event-based timing system.

In practice, the timing system is constrained by hardware. At LINAC, the timing system must satisfy three major requirements,

- PPM,
- AC50 synchronization,
- DR operation.

It is inevitable to choose PPM since KEK LINAC needs to provide a beam for 4 rings. Accordingly, the timing system must switch the beam mode and control parameters turn-by-turn. To keep the hardware, operate in good stability, the AC50 synchronization is also mandatory. Concerning AC50 drift, these restrictions eventually force us to develop several modules, such as the TDC and MTG module, to perform AC50 synchronization every pulse.

The operation of DR increases the dependency between DR injection pulse and DR extraction pulse. Besides that, the preparation trigger for the injection magnet requires a timing system to provide trigger one pulse before. The pre-trigger requirement conflicts with the PF/PF-AR beam mode since the chance coincidence is used to generate a trigger signal for PF/PF-AR. As a result, the implementation of pre-event is changed from data buffer transmission to event code delivery to tackle the conflict.

The detailed implementation of the timing system at KEK LINAC is also discussed. The reason for sequence shift and how to sequence shift is achieved are thoroughly analyzed. Another conceivable restriction between 8/9 pulses sequence shift and DR storage time is described and a solution of 16/18 pulses sequence shift scheme is chosen to be the basic structure of the main timing station.

There are obstacles to limit the LER RF bucket selection number which comes from the DR injection kicker magnet during DR two-bunch and two-pulse operation. We choose to shift the RF phase in downstream LINAC to solve the restriction. By shifting the RF phase, the chance for extraction from DR increases, and all the LER RF buckets can be selected.

All these restrictions raise the complexity of the timing system. Thus, it is difficult to understand what was happening in the timing system behaves abnormally. To locate the problem source and quickly handle the error, several log systems for the timing system are newly constructed. Firstly, the event code log system is implemented by a low-level driver program for EVR, and it works well during the elapsed two years. Then, the AC50 log system is regarded as necessary after some brief analysis of the timing system. Finally, two basic failure modes are summarized to describe the timing system error. The theoretical failure recurrence is done based on the timing log and the error source is located.

Most of the timing system errors are caused by AC50 drift. Through the computer simulation, the sequence shift algorithm is designed to handle mildly AC50 drift (i.e., 50±0.1 Hz) but sometimes the AC50 sharply fluctuates in 50±0.2 Hz. The strong AC50 drift destroys the PPM logic and generates an abnormal trigger signal to hardware. The beam operation must stop when these signals are received by some timing-sensitive hardware, such as the klystron modulator.

Several solutions are proposed to solve this problem. The temporary solution is to use an AC50 regulator module to perform a partially AC50-dependent operation. The performance of the AC50 regulator is tested and it successfully solves the timing system failure caused by strong AC drift. However, this method causes the degradation of beam quality as well as the efficiency of LINAC.

The ultimate solution is RF phase shift for downstream LINAC and upgrade of sequence shift. The functionality of phase shift for downstream LINAC has been tested recently and is able to increase the RF bucket number for two-bunch and two-pulse operations. The physics commissioning is still undergoing. The 8/9 pulses sequence shift can only increase the tolerance of AC50 drift level and if AC50 fluctuations in 50±0.4 Hz, the failure will occur again. Thus, we propose the idea of adding the information of recent AC drift value to estimate the AC50 arrival time in the future. In this way, the sequence shift becomes more intelligent. The construction and test of the new sequence shift scheme are scheduled for 2021 summer.

# Appendix A

# Source Code

## A.1 DR Buckets for 2-bunch and 2-pulse

```
#/usr/bin/python3

def cal_bs_delay(harm_dr, dr_occupied_bkt, kicker_delay_bkt):
    mr_avail_one_bunch, dr_avail_one_bunch = set(), set()
    mr_avail_two_bunch, dr_avail_two_bunch = set(), set()
    idx = 0
    mr_rf = 114.24/11.0*49
    delay_period = (1 / mr_rf) * 49000
    harm_mr = 5120
    delay = idx * delay_period
    while delay <= 2000000:
        mr_bkt = idx * 49 % harm_mr
        dr_bkt = idx * 49 % harm_dr

        # bkt number ranges from 0-229
        # bkt 0 and 49 are occupied, from bkt 49, wait for ‘
    kicker_delay_bkt‘ bucket

        # for one bunch injection
        if dr_occupied_bkt + kicker_delay_bkt < dr_bkt < harm_dr - 49 -
    kicker_delay_bkt + dr_occupied_bkt:
```

```
20              mr_avail_one_bunch.add(mr_bkt)
21              dr_avail_one_bunch.add(dr_bkt)
22          # for two bunch injection
23          if dr_occupied_bkt + 49 + kicker_delay_bkt < dr_bkt < harm_dr -
    49 - kicker_delay_bkt + dr_occupied_bkt:
24              mr_avail_two_bunch.add(mr_bkt)
25              dr_avail_two_bunch.add(dr_bkt)
26          idx += 1
27          delay = idx * delay_period
28      print("************************************")
29      print("one_bunch: MR:", len(mr_avail_one_bunch), " DR:", len(
    dr_avail_one_bunch))
30      print("************************************")
31      print("two_bunch MR:", len(mr_avail_two_bunch), "DR:", len(
    dr_avail_two_bunch))
32
33
34  if __name__ == '__main__':
35      # note, the logic does not consider occupied bucket other than 0 and
    49.
36    cal_bs_delay(230, 0, 50)
```

Listing A.1: Available DR buckets for 2-bunch and 2-pulse injection.

## A.2 Available DR buckets for RF Phase Shift

```
1  #/usr/bin/python3
2  # 8.75 ns
3  Event_CLk = 1000 / 114.24
4  # 1.965 ns
5  MR_Clk = 1000 / (114.24 / 11 * 49)
6
7
8  def cal_delay(mr_bkt, dr_bkt):
9      for i in range(0, 5120 * 23):
10         if i * 49 % 5120 == mr_bkt and i * 49 % 230 == dr_bkt:
11             cycle = int(i / 5120)
12             oppo = i % 5120
13             # print(i, cycle, oppo)
14             dr_for_ler0 = cycle * 49 * 5120 % 230
```

```
            # print(dr_for_ler0)
            return dr_for_ler0


def cal_delta_t(delta_t):
    _all_delta = set()
    _res = []
    for bkt_num in range(0, 49):
        for evt_clk in range(0, 12):
            delta = abs(round(MR_Clk * bkt_num - Event_CLk * evt_clk, 4))
            if delta < delta_t:
                _all_delta.add(delta)
                dr_bkt = cal_delay(bkt_num, bkt_num)
                _res.append(
                    [bkt_num, delta, (dr_bkt + 100) % 230, (dr_bkt + 50)
    % 230, dr_bkt, (dr_bkt - 50 + 230) % 230,
                     (dr_bkt - 100 + 230) % 230])
                # print(bkt_num, dr_bkt, delta)
    return sorted(_all_delta), _res


def cal_dr_bkt(delta, data: [[]]):
    dr_cand_493, dr_cand_986, dr_cand_1479, dr_cand_1972, dr_cand_2465 =
    [], [], [], [], []
    for i in range(len(delta)):
        temp1, temp2, temp3, temp4, temp5 = set(), set(), set(), set(),
    set()
        for j in data:
            if j[1] <= delta[i]:
                temp1.add(j[4])

                temp2.add(j[4])
                temp2.add(j[5])

                temp3.add(j[3])
                temp3.add(j[4])
                temp3.add(j[5])

                temp4.add(j[3])
                temp4.add(j[4])
                temp4.add(j[5])
```

```
                temp4.add(j[6])

                temp5.add(j[2])
                temp5.add(j[3])
                temp5.add(j[4])
                temp5.add(j[5])
                temp5.add(j[6])
        dr_cand_493.append(len(temp1))
        dr_cand_986.append(len(temp2))
        dr_cand_1479.append(len(temp3))
        dr_cand_1972.append(len(temp4))
        dr_cand_2465.append(len(temp5))

    return dr_cand_493, dr_cand_986, dr_cand_1479, dr_cand_1972,
    dr_cand_2465


if __name__ == '__main__':
    # cal_delay(23, 23)
    all_delta, res = cal_delta_t(4)
    print(all_delta)
    for ii in cal_dr_bkt(all_delta, res):
        print(ii)
```

Listing A.2: Available DR buckets for RF Phase Shift

## A.3 Sequence Shift Simulation

```
#/usr/bin/python3
import numpy as np
import matplotlib.pyplot as plt

freq = 114.24 / 11 / 5120 / 46 * 1000000  # Unit Hz
period = 1 / freq * 1000  # Unit [ms]
seq = [0, 1]


def seq_shift_simulation(speed, ref, loop, seq_type, l_bound, r_bound):
    if seq_type == "16/18" or seq_type == 0:
        seq_length = [18, 16]
```

```
13          seq_shift = [-2.854830, 2.50202]
14      else:
15          seq_length = [9, 8]
16          seq_shift = [-2.854830 / 2, 2.50202 / 2]
17      y_pre = 10
18      y_max = 0
19      s_pre = 0
20      s_cur = 1
21      time_passed = 0
22      failure_time = 0
23      failure_happened = 0
24      for i in range(0, loop):
25          if (y_pre + seq_shift[s_pre] + seq_shift[s_cur]) > ref:
26              s_next = 0
27          else:
28              s_next = 1
29          y_cur = y_pre + speed + seq_shift[s_pre] + seq_length[s_cur] *
    speed
30          time_passed += seq_length[s_cur] * 20 - seq_shift[s_cur]
31          if y_cur > y_max:
32              y_max = y_cur
33          if failure_happened == 0 and (y_cur > r_bound or y_cur < l_bound)
    :
34              failure_time = round(time_passed / 1000, 3)
35              failure_happened = 1
36          y_pre = y_cur
37          s_pre = s_cur
38          s_cur = s_next
39      return failure_time
40
41
42  if __name__ == '__main__':
43      idx1 = np.arange(-80, 80, 0.1)
44      idx2 = np.arange(-160, 160, 0.1)
45      left_boundary = 4.5
46      right_boundary = 15
47      ref_value = 9.85
48      thresh_1, thresh_2 = [], []
49      plt.figure(figsize=(6, 4), dpi=200)
50      plt.grid(True)
51
```

```
    for i in idx1:
        thresh_1.append(
            seq_shift_simulation(speed=i / 1000, ref=ref_value, loop=500,
     seq_type=0, l_bound=left_boundary,
                                 r_bound=right_boundary))
    thresh_1 = np.array(thresh_1)
    mask1 = thresh_1 > 0
    fig_title1 = f"Simulation of AC50 drift with 16/18 pulses sequence ({
    left_boundary}, {right_boundary})"
    label1 = f"Ref: {ref_value}"
    # plt.title(fig_title1)
    plt.scatter(idx1[mask1], thresh_1[mask1], marker="x", color='blue', s
    =5, label=label1)

    # for i in idx2:
    #     thresh_2.append(
    #         seq_shift_simulation(speed=i / 1000, ref=ref_value, loop
    =500, seq_type=1, l_bound=left_boundary,
    #                              r_bound=right_boundary))
    # thresh_2 = np.array(thresh_2)
    # mask2 = thresh_2 > 0
    # fig_title2 = f"Simulation of AC50 drift with 8/9 pulses sequence ({
    left_boundary}, {right_boundary})"
    # label2 = f"Ref: {ref_value}"
    # # plt.title(fig_title2)
    # plt.scatter(idx2[mask2], thresh_2[mask2], marker="x", color='blue',
     s=5, label=label2)

    # plt.xticks(fontsize=18)
    # plt.yticks(fontsize=18)
    plt.xlabel("AC50 drift value [$\\mu$s]", fontsize=14)
    plt.ylabel("Timing for race condition [s]", fontsize=14)

    plt.legend()
    plt.show()
```

Listing A.3: Sequence Shift Simulation

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