Development of Timing Read-Back System toward Stable Accelerator Operation

加速器の安定運転に向けたタイミング読み出しシステムの開発

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"What doesn't kill you makes you stronger."

— Friedrich Nietzsche

Abstract

Since the timing system of the Japan Proton Accelerator Research Complex (J-PARC) started in 2006, there were trigger-failure events during beam operation, some of which seriously affected the regular and stable operation of the J-PARC accelerator. Some cases showed that even the timing system showed no operational error, the delayed-trigger signal did not arrive at the device side. Thus, the operators could not find the fault remotely. Through the analysis of these events, we recognized the prominent importance of developing the timing read-back system. The system is expected to run independently from the timing system. It can read back the distributed delayed-trigger signals at the device side and confirm whether the timing signals arrive or not.

This research clarifies that a PLC-type triggered scaler module is a key for developing the timing read-back system. A study of the module started in 2020. A prototype timing read-back system with identification routines of unexpected trigger-failure events was developed based on the Experimental Physics and Industrial Control System (EPICS) framework. It was demonstrated with a dummy injection kicker signal that the read-back system was capable of detecting trigger-failure events as we expected. In addition, customizing availability with the EPICS framework was demonstrated.

Based on the study above, customized read-back systems for a vital timing signal and two delayed-trigger signals have been developed: a system of 25 Hz signal from RCS, a system of pulsed bending magnet trigger, and a system of optical-gate signal. These systems were implemented successfully and demonstrated as countermeasures against past trigger-failure events. They enable the operators to find the trigger-failure event remotely and provide the associated event information, which can help us to solve problems effectively in time.

Besides, read-back systems for other signals were also developed with the triggered scaler module, such as a Machine Protection System (MPS) beam abort signal detection system and a Low-Level Radio Frequency (LLRF) pattern monitoring system. Successful measurements of these signals show that the triggered scaler module has wide usage in various fields.

The read-back systems of this work are already in use at J-PARC MR, monitoring various accelerator signals. Plans to extend the system to cover more signals of J-PARC and to apply the system for other accelerators are also discussed.

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Abbreviations

ACC	**A**cceleration
BEPC-II	Upgrade Project of **B**eijing **E**lectron **P**ositron **C**ollider
CA	**C**hannel **A**ccess
CCB	**C**entral **C**ontrol **B**uilding
CCR	**C**entral **C**ontrol **R**oom
CLK	**C**lock
CM	**C**lock **M**aster
COD	**C**losed **O**rbit **D**istortion
CT	**C**urrent **T**ransformer
DCCT	Beam Current in J-PARC MR
DM	**D**ata **M**aster
ECA	**E**vent **C**ondition **A**ction
EDM	**E**xtensible **D**isplay **M**anager
EPICS	**E**xperimental **P**hysics and **C**ontrol **S**ystem
EVG	**E**vent **G**enerator
EVR	**E**vent **R**eceiver
E/O	**E**lectrical-to-**O**ptical
FAIR	**F**acility for **A**ntiproton and **I**on **R**esearch
FCT	**F**ast **C**urrent **T**ransformer
FX	**F**ast Extraction
GeV	**G**iga **e**lectron **V**olt
GMT	**G**eneral **M**achine **T**iming
GPS	**G**lobal **P**ositioning **S**ystem

HD	**H**adron Facility
Hz	**H**ertz
INJ	**I**njection
IOC	**I**nput/ **O**utput **C**ontroller
ITER	**I**nternational **T**hermonuclear **E**xperimental **R**eactor
I/O	**I**nput/ **O**utput
JAEA	**J**apan **A**tomic **E**nergy **A**gency
JCE	**J**AVA **C**ommissioning **E**nvironment
J-PARC	**J**apan **P**roton **A**ccelerator**R**esearch **C**omplex
KEK	High Energy Accelerator Research Organization
LAN	**L**ocal **A**rea **N**etwork
LI	J-PARC Linear Accelerator
LLRF	**L**ow **L**evel **R**adio **F**requency
L3BT	**L**inac to **3** GeV RCS **B**eam **T**ransport Line
MEDM	**M**otif **E**ditor and **D**isplay **M**anager
MeV	**M**ega **e**lectron **V**olt
MHz	**M**ega **H**ertz
MLF	**M**aterials and **L**ife Science **F**acility
MM	**M**anagement **M**aster
MPS	**M**achine **P**rotection **S**ystem
MR	**M**ain **R**ing Synchrotron
MRF	**M**icro-**R**esearch **F**inland
NIM	**N**uclear **I**nstrumentation **M**odule
NU	**N**eutrino Facility
OPI	**O**perator **I**nterface
O/E	**O**ptical-to-**E**lectrical
PLC	**P**rogrammable **L**ogic **C**ontroller
PPS	**P**ersonnel **P**rotection **S**ystem
RCS	**R**apid **C**ycling **S**ynchrotron
RDB	**R**elational **D**atabase
RF	**R**adio **F**requency

R & D	**R**esearch and **D**evelopment
SLAC	National Accelerator Laboratory
SNS	**S**pallation **N**eutron **S**ource
SSRF	**S**hanghai **S**ynchrotron **R**adiation **F**acility
SX	**S**low Extraction
TLU	**T**imestamp **L**atch **U**nit
Trig	25 Hz Trigger Clock Signal
TRN	**T**iming **R**eceiver **N**ode
TS	**T**riggered **S**caler
T2K	**T**okai to **Kamioka**
UTC	**C**oordinated **U**niversal **T**ime
WR	**W**hite **R**abbit
3NBT	**3** GeV RCS to **N**eutron Facility **B**eam **T**ransport Line
350BT	**3** GeV RCS to **50** GeV MR **B**eam **T**ransport Line

For my family

and all the people who supported me.

Part I

Background Introduction

Chapter 1

Introduction of the Dissertation

This Chapter mainly introduces the overview of this work. The motivation of the work is explained, followed by a research methodology. Then, the contribution to knowledge is given. Moreover, the structure of this dissertation is outlined, complemented by a summary of each Chapter.

1.1 Motivation

The motivation of this work is derived from the need for a read-back system for the Japan Proton Accelerator Research Complex (J-PARC) timing system. It was researched and developed in the context of case studies for the J-PARC timing system.

Over a long operation experience of J-PARC since 2006, there have been some strange beam behaviors (not often, but it does exist). In such cases, although by no means certain, the trigger failure of the timing system was suspicious as its cause. However, it is not easy to confirm that the triggers have been successfully distributed at that time or not without the proper way to record the event.

To identify the trustworthy source of these strange behaviors and ensure a highly available accelerator operation in the future, a new read-back system for the existing J-PARC timing

system is urgently needed. Fig. 1.1 shows the relationship between a timing system and a timing read-back system in general. The timing system distributes delayed-trigger to each accelerator device. The timing read-back system runs independently of the timing system. It observes and confirms delayed-trigger signals by the "sensor" at the device side, then makes an alert when a trigger failure event is detected. Therefore, the timing read-back system is crucial to identify whether the timing system causes the failure. Such a read-back system is essential for J-PARC to improve the availability of accelerators.

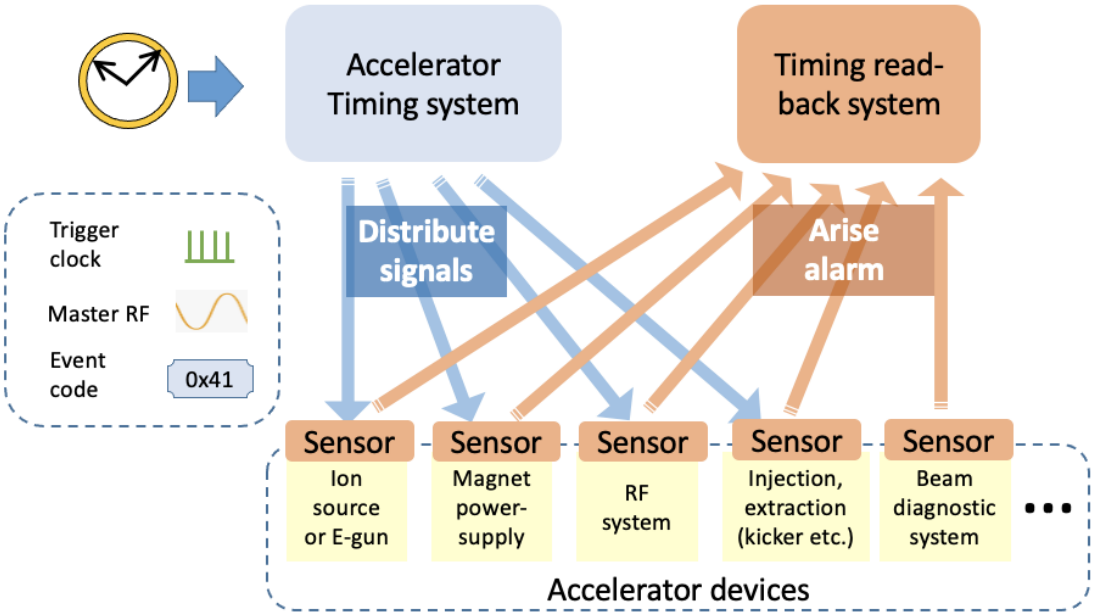

FIGURE 1.1: The relationship of general timing system and timing read-back system.

1.2 Research Process

This work is dedicated to developing a read-back system for accelerator timing. The research process of this work is mainly divided into two parts: research and development.

1.2.1 Research

Literature Review The literature review started from publications associated with the accelerator timing system. A comprehensive understanding of the timing system is the basis of developing a read-back system that meets the requirements. Most of the related

work used in this dissertation was obtained from conference proceedings and journal articles.

Some unpublished sources were J-PARC internal materials, such as triggered scaler specification documents, technical notes, presentations, and J-PARC timing parameters. These kinds of materials provided important information on the new read-back system requirements. Moreover, some accelerator-related information was acquired from communications with accelerator scientists and engineers at J-PARC.

Existing Systems at Other Sites Based on the literature review, the advantages and disadvantages of existing read-back systems for other accelerator timing were studied. This research was used as the foundation for a survey of suitable technology to develop a new read-back system. Some existing ones at accelerators, such as J-PARC and KEK, were evaluated (Chapter 5).

Technology The results showed that a read-back system based on a Programmable Logic Controller (PLC)-type triggered scaler module has more advantages than other technology (Chapter 5.4.3). There are no similar technologies as a triggered scaler module, which can (a) detect an unexpected trigger-failure event, (b) visualize the trigger signals as a waveform, and (c) customize other modules to realize multiple functions. The feature of the module is ideal for implementing the functions of the new read-back system and can be customized according to different requirements. Moreover, the Yokogawa PLC-type module is the regular hardware at J-PARC, which can be perfectly combined with other exiting PLC modules and systems. The core software is Experimental Physics and Industrial Control System (EPICS) and related modules, which are open source and are widely used in accelerator control.

1.2.2 Development

Objectives Based on the case study of J-PARC, some trigger-failure events of its timing system have been learned (Chapter 4). The main objectives of development in this work were defined:

1. Develop read-back systems to monitor timing signals based on the triggered scaler module.

2. Develop customized applications for specific accelerator devices.

The first objective requires a thorough understanding of the J-PARC timing system and the triggered scaler module. What timing signals need to be monitored, where they are located, how to measure the signals, what unexpected trigger events might be caused by, and so on, all of which need to be resolved.

The second objective is the updated version of the first objective. It requires an overall knowledge of the behaviors of accelerator beams when a faulty timing event occurs. Consequently, customized applications with monitoring accelerator signals of interest are needed to be developed.

Equipment Test To realize the two objectives, key equipment, PLC-type triggered scaler module, is studied. A test platform will be built to test the hardware function. To realize the I/O control of the module, I/O libraries will be developed. After that, the signal monitoring function will be tested. An injection kicker signal is good to demonstrate the performance of the module.

Prototype of Read-Back System After the equipment test, a prototype read-back system to detect unexpected trigger failure events is planning to be developed. It will be an EPICS IOC with a triggered scaler module. The software routines will detect faulty events in an accelerator cycle. The injection kicker signal will be used again to test the prototype trigger-failure event detection system. If it detects simulated unexpected-trigger events as expected, the actual implementations of the timing read-back system will be the next step.

Customized Read-Back Systems The final test is to apply the prototype system to the actual implementations. According to different trigger-failure events, customized read-back systems should be developed and demonstrated countermeasures against the circumstances. In addition, the customized read-back systems must be separately tested and operated for at least one month during beam operation.

Analysis and Conclusion The analysis of the test results is to identify bugs and areas for improvement in the system. If the system can detect the trigger-failure event, the system works as expected. If not, the software database or hardware needs to be modified and should test it again.

1.3 Contribution to Knowledge

The work in this dissertation aims to improve the efficiency of searching for unknown signal events and improve the stability of the accelerator operation.

A unique device, triggered scaler module, was designed and used as the key device to construct read-back systems. The differences between a triggered scaler module, a digitizer, and a simple scaler are shown in Fig. 1.2. Compare the digitizer, the triggered scaler, and the simple scaler, the uniqueness of the triggered scaler module is that it has external trigger input (digital signals) as a digitizer, and its output is a data buffer with 192 elements. It also has flexibility with other PLC-type I/O modules and with EPICS software.

The read-back system based on the triggered scaler module can measure accelerator timing signals and detect unexpected trigger-failure events by developing software libraries and identification routines. The real implementations are countermeasures against past trigger-failure events. Besides, the system can be configured as a standalone system, applied to other accelerator facilities. The application of the read-back system is vital for the accelerator timing system and helps provide stable beam operation.

1.4 Structure of Dissertation

This dissertation consists of four main parts. Each part contains one or more Chapters. The structure of the dissertation is shown in Fig. 1.3.

Part I: Background Introduction Apart from a general introduction of this dissertation, the first part is an introduction to J-PARC and several accelerator timing systems (Chapter 2 and Chapter 3). Both are required for understanding the problem discussed in Part II. The former provides the necessary background of J-PARC accelerators and experimental facilities, and the timing scheme and control system of J-PARC is also required to comprehend. The latter introduces three types of accelerator timing systems, followed by a discussion of three different timing systems. They form the fundamental material to study the problems discussed in Chapter 4.

Part II: Problem Analysis Based on the knowledge of J-PARC, four J-PARC unexpected trigger-failure events are presented (Chapter 4). This case study analysis depends

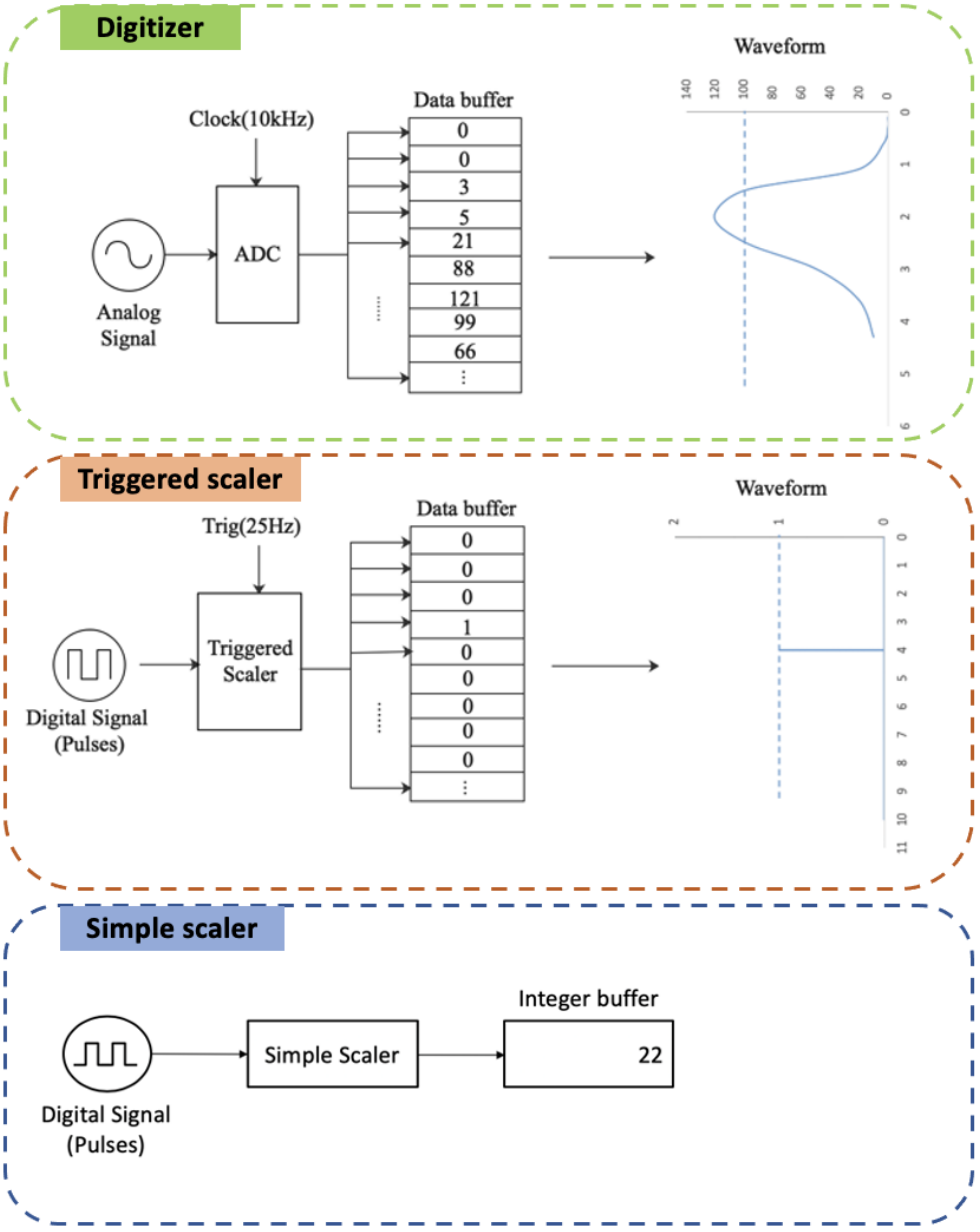

FIGURE 1.2: The comparison of digitizer, triggered scaler, and simple scaler.

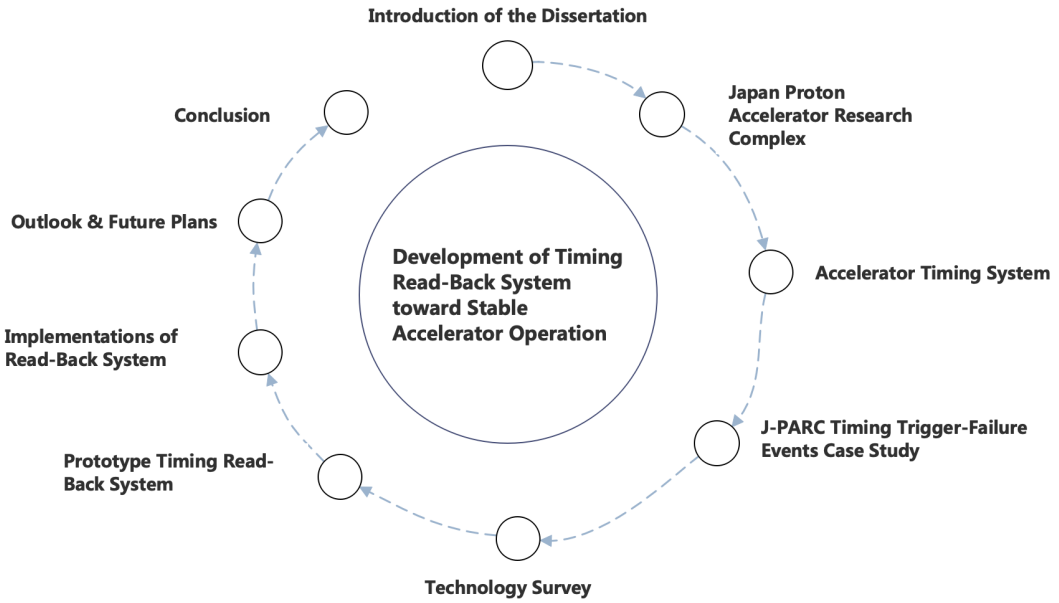

FIGURE 1.3: Structure of the dissertation.

on experienced faulty events that occurred since J-PARC operated. Building on this case study, a technology survey (Chapter 5) follows, which contains an introduction of existing systems to detect false triggers in J-PARC and other accelerator facilities. A detailed discussion of suitable hardware and software platforms is given. A unique module, the triggered scaler module, is also introduced in this Chapter, including the details of the module, such as working principle, experimental performance, and firmware update.

Part III: Approach and Implementation This part contains the introduction of different read-back systems developed based on the triggered scaler. Chapter 6 presents a prototype system. Basic functions were developed and tested using a dummy signal. In Chapter 7, customized applications were introduced. According to the case study, applications were developed for solving the past unexpected trigger-failure events effectively. The last part presents the future plan and conclusion of this work. Chapter 8 indicates some future plans at J-PARC and for other accelerators. And then, a conclusion is given to summarize the work (Chapter 9).

1.5 List of Publication

Min Yang, Norihiko Kamikubota, Yuto Tajima, Kenichi C. Sato, Nobuhiro Kikuzawa. Applications of Triggered Scaler Module for Accelerator Timing. *Proceedings of the 22nd Virtual IEEE Real Time Conference*, October 2020. URL https://arxiv.org/abs/2010.14716.

Chapter 2

Japan Proton Accelerator Research Complex

2.1 Overview

This Chapter focuses on an introduction to Japan Proton Accelerator Research Complex (J-PARC). Since the research of the work was done at J-PARC accelerators, the J-PARC accelerators are introduced in detail. Then, the timing scheme of J-PARC is explained. The J-PARC control system is also presented.

2.2 J-PARC Accelerators and Experimental Facilities

J-PARC [1] is an accelerator complex dedicated to high-power protons. It is a collaborative project between the High Energy Accelerator Research Organization (KEK) and Japan Atomic Energy Agency (JAEA). Since the first beam started in 2006, J-PARC has been playing a vital role in advanced science.

Fig. 2.1 shows the layout of J-PARC facilities. It consists of three accelerators: a 400 MeV Linear accelerator (LI), a 3 GeV Rapid-Cycle Synchrotron (RCS), and a 30 GeV Main Ring

Synchrotron (MR). In addition, the high-power beam is delivered to three experimental facilities, i.e., the Materials and Life Science Facility (MLF), the Neutrino facility (NU), and the Hadron facility (HD), for advanced studies in many areas.

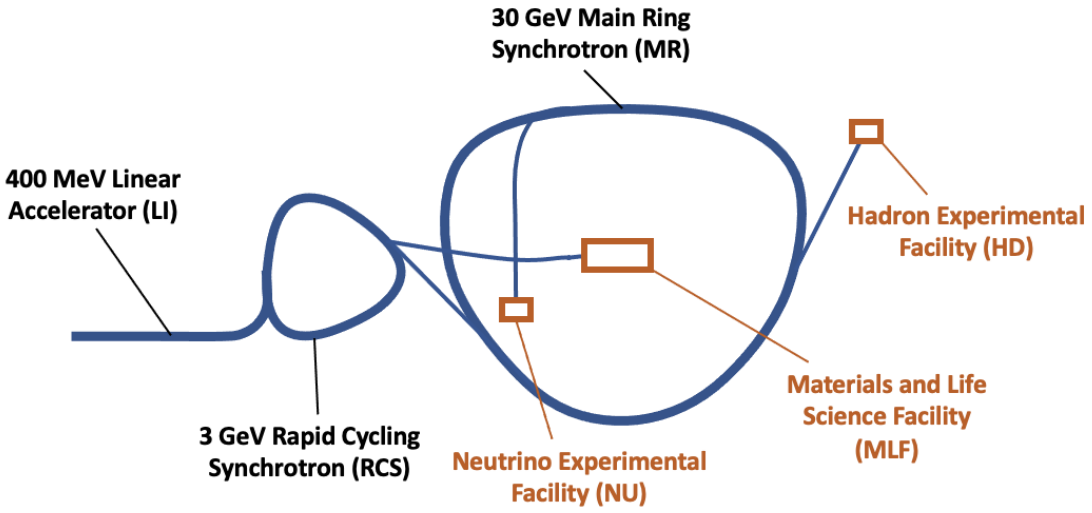

FIGURE 2.1: Layout of J-PARC facilities.

The object of J-PARC is to provide various high-power secondary particle beams, such as muon and neutrino, for forefront science conducted by users from all over the world [2, 3]. Three primary scientific goals will be achieved with these secondary particle beams: nuclear and particle physics, materials and life sciences, and R & D toward nuclear transmutation. The facility for nuclear transmutation is a future plan and has not been constructed yet.

Each of three accelerators and three experimental facilities is introduced in the following.

J-PARC LI The length of J-PARC LI is approximately 300 m. It is a proton linear accelerator, which accelerates beams up to 400 MeV. LI is designed with the 50 Hz repetition rate. However, so far, it injects beams into RCS with the repetition rate of 25 Hz [4, 5].

J-PARC RCS The circumference of RCS is 348.333 m. After the 400 MeV proton beams are injected through the transport line from LI to RCS (L3BT), the RCS accelerates them up to 3 GeV. RCS supplies beam to MR through the transport line from RCS to MR (350BT), or MLF through the transport line from RCS to MLF (3NBT) [6]. The

final objective of RCS is to distribute 1 MW high-power beams with the 25 Hz repetition rate [7].

J-PARC MR MR is a circular accelerator with the circumference of 1567.5 m. During beam operation, the 3 GeV beams are accelerated to 30 GeV in 1.4 s. Then MR delivers the 30 GeV beams to HD with the interval of 5.20 s (called slow extraction (SX)), or delivers to NU with the interval of 2.48 s (called fast extraction (FX)) [8]. Recently the power upgrade program of MR toward 1.3 MW is underway [9].

Materials and Life Science Facility MLF is one of the world's leading facilities to researchers from all over the world for scientific research and industrial applications. The aim of it is to facilitate materials and life science using the high-intensity pulsed neutron and muon beams. They are produced using 3 GeV protons [10]. Twenty-three neutron beamlines were constructed for the pulsed spallation neutron source.

Neutrino Experimental Facility NU aims to carry out advanced neutrino research using the world's highest-intensity neutrino beam [11]. Neutrino beam is produced using 30 GeV protons from MR. There is a multi-national physics experimental project called T2K (Tokai to Kamioka), which directs high-intensity neutrino beams from the neutrino facility to the super-kamiokade in Hida, Gifu prefecture (295 km away from the J-PARC site) to study neutrino oscillation.

Hadron Experimental Facility HD is designed to investigate the fundamental components of matter (mesons and hadrons in nuclei) and measure their interactions with extremely high precision. The primary high-intensity proton beam extracted from MR is used to produce kaons, pions, and other secondary particles [12].

2.3 J-PARC MR Timing Scheme

In J-PARC, two time cycles are used during beam operation: rapid cycle and slow cycle. A 25 Hz rapid cycle is used at the LI and RCS accelerators, and a slow cycle is used at the MR accelerator. Because the slow cycle decides the overall time behavior of the accelerators, it is also called "machine cycle."

Fig. 2.2 shows timing schemes of two beam operation modes of MR: FX mode for beam delivery to NU and SX mode for beam delivery to HD.

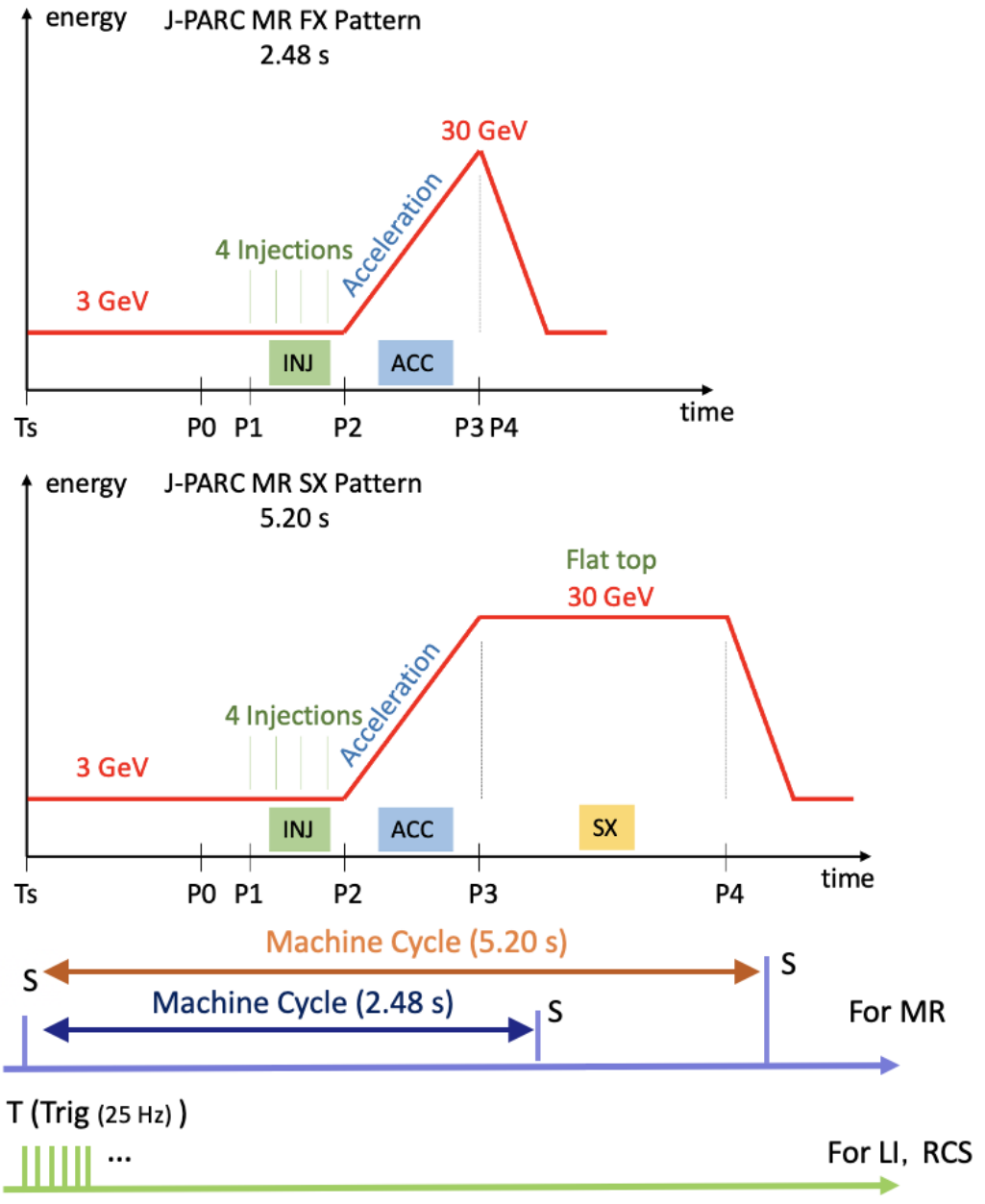

FIGURE 2.2: Timing schemes of two beam operation modes of J-PARC MR. The red lines represent the time variation of the beam energy.

The cycle interval of FX (SX) mode is 2.48 s (5.20 s), respectively. The time points from P1 to P4 indicate the beginning of MR injection, the beginning of MR acceleration, the end of MR acceleration and the beginning of 30 GeV flat top, and the end of flat top, respectively. These time points correspond to three main phases in one MR cycle: an injection (INJ) phase, an acceleration (ACC) phase, and a fast extraction (FX) phase, or a slow extraction (SX) phase. During the INJ phase, MR accepts four successive injections from RCS in one machine cycle. During the ACC phase, the 3 GeV beam is accelerated up to 30 GeV.

In the FX phase, a high-power beam is delivered to NU as soon as the beam reaches the energy of 30 GeV. When a failure event (machine protection system event, which will be explained in Chapter 7.5.1.1) occurs during the ACC phase, the beam is extracted safely into the dump [13].

In the SX phase, the accelerated 30 GeV beam is slowly (i.e., 2.1-2.2 s) extracted to HD by the third integer resonant extraction [14]. However, when a failure event occurs, the SX process is stopped immediately, and the rest of the beam is dumped at the end of the flat top.

2.4 J-PARC Control System

Early decisions of J-PARC were made by JAEA for LI and RCS, and by KEK for MR. Therefore, control systems were developed based on different policies by two institutes [15]. The components of the control systems for three accelerators are shown in Table 2.1. The table reflects the environments of the control community around 2002 to 2007.

Table 2.1: The components of three control systems in J-PARC [15].

Accelerator	Basic GUI tool	High-level application tool	Operating system	Hardware	Driver
LI	JAVA MEDM	XAL/JCE	VxWorks PowerPC	VME	VME I/O modules; TeraDev for PLC
RCS	JAVA MEDM	SAD	VxWorks PowerPC	VME	VME I/O modules; TeraDev for PLC
MR	MEDM EDM	SAD Python ROOT	Linux	VME	NetDev for PLC; WE7000 drivers

2.4.1 Software

2.4.1.1 EPICS

For ease of administration, all control systems in J-PARC use EPICS framework [16]. It is a free and open-source software framework for developing distributed control system. It has been used in many accelerators, telescopes, scientific experiments, for example, KEK and J-PARC in Japan, BEPC-II (upgrade project of Beijing Electron Positron Collider) and SSRF (Shanghai Synchrotron Radiation Facility) in China, SLAC (National Accelerator Laboratory) and SNS (Spallation Neutron Source) in United States of America, FAIR (Facility for Antiproton and Ion Research) in Germany, and ITER (International Thermonuclear Experimental Reactor) in France. The worldwide community maintains the fundamental sources of software and encourages communication between users.

The Architecture of EPICS The basic components of EPICS are: Operator Interface (OPI), Input/Output Controller (IOC), and Local Area Network (LAN).

OPI is a graphical or command line interface for operators or equipment experts.

IOC is a front-end computer which converts Channel Access (CA) to various kinds of communication protocols (such as VME bus, PCI bus, GPIB, serial ports, Yokogawa PLC bus, field busses, etc).

LAN allows the communication between OPI and IOC. An EPICS software, CA, provides network transparent access to IOC databases [17].

2.4.1.2 Software for GUI and High-Level Application

In LI and RCS, JAVA is the default platform of all of the OPI applications. For the early commissioning of LI, XAL [18], a JAVA-based programming tool for accelerator physics was introduced from SNS [19]. In addition, a JAVA Commissioning Environment (JCE) was developed to write commissioning applications in Strategic Accelerator Design (SAD) script (see below) for LI [20]. Some GUI applications were developed by an EPICS tool, Motif Editor and Display Manager (MEDM).

In MR, policies were introduced from KEKB. MR introduced standard EPICS tools as they are in KEKB: MEDM and Extensible Display Manager (EDM), for the rapid development of GUI applications. The SAD [21], a computer program for accelerator design

and simulations, was introduced from KEKB as the default high-level application tool. The Python script and ROOT [22] are also used in MR.

2.4.2 Hardware for I/O Controller

Control systems for all the three accelerators use a VME-bus computer as the default I/O controller (i.e., EPICS IOC). For LI and RCS, a PowerPC-based CPU board with a real-time operating system (VxWorks) was used. Many VME-bus I/O boards were used for both digital and analog signals. Pieces of Yokogawa PLC were also introduced as local controllers. For MR, KEK selected an intel-based CPU board together with Linux operating system. Since MR is a slow cycle machine, millisecond-order real-time features were not needed. The Linux is easy to maintain and to develop customized control software. Since 2008, a new CPU module for Yokogawa PLC, in which Linux and EPICS run with PLC I/O modules was introduced [23, 24]. Numbers of EPICS IOCs in MR were reported elsewhere [25].

2.4.3 Network

The network system for J-PARC accelerator control consists of a) the redundant core switches located in the central building, and b) about 250 edge switches in distributed buildings. The backbone of the network is the 10 Gbps rate. The typical edge switch has 48 ports of the 1 Gbps rate. To avoid traffic concentration, the network is divided into sub-networks (VLANs). Each accelerator or experimental facility has its own VLAN (for example, LI-VLAN, NU-VLAN). In addition, because all accelerators are controlled from the Central Control Room (CCR), CCR-VLAN exists.

More details of the network system are given elsewhere [26].

2.4.4 Ralational Database

Both JAEA and KEK use PostgreSQL Relational Database (RDB). It has been used for automatic generation of configuration files for EPICS IOC in JAEA [27]. An archive system for LI and RCS was also developed using the RDB. KEK has used the RDB to manage IP addresses, EPICS record names, screen copies of terminals, etc. An electric logbook, Zlog [28], also depends on the RDB.

2.4.5 Personnel Protection System (PPS)

The PPS is the essential system for protecting personnel safety against radiation and other hazards during accelerator operation. Two PLC ladder logics were developed by two companies, which is expected to increase the system reliability. Details of the PPS are given elsewhere [29].

2.4.6 Machine Protection System (MPS)

The MPS is an accelerator-wide fast interlock for protecting accelerator devices from the damage caused by high power beams. It is necessary to stop the beam as soon as possible when a failure of device (typically a power supply for magnet or Radio Frequency (RF)) happens. For LI and RCS, the MPS system has a simple logic with a tree-type topology [15, 30]. When a failure occurs, the MPS starts to stop the ion source in LI within 10 μs. While for the MR-MPS system, more complicated logic is needed, since the behavior of the MR-MPS depends on phases of the slow cycle, a beam mode (single shot or continuous), and the status of downstream experimental facilities. Thus, a different MPS system was developed [31]. More information on the MR-MPS is given in [32].

2.4.7 Timing System

The research of the J-PARC timing system was made in a very early phase. From 2002 to 2003, NIM modules and VME-bus timing modules (transmitter and receiver) were developed by JAEA. However, it was designed only for 25 Hz machines (LI and RCS). To match the slow cycle machine of MR, using the same hardware but different software framework was needed. Details will be given in Chapter 3.2.1.

Chapter 3

Accelerator Timing System

Timing systems play an essential role in the successful operation of accelerators. They are applied not only to synchronize different processes but also to ensure the overall coherency of data acquisition.

This Chapter mainly introduces the timing systems in three different accelerator complexes, followed by discussing three kinds of timing systems.

3.1 Timing System Overview

In general, the timing system is to provide a trigger to each of the accelerator components with a specified delay. The trigger signal is distributed from one master to many receiving nodes through a dedicated timing network.

There are two types of timing strategies in a timing system: event-based system and time-based system [33]. In an event-based system, the timing master is responsible for sending a clock signal (for example, 50 Hz) and a message through the timing network. The timing receivers would generate pulses to the specific accelerator components using the received clock signal and the message. In a time-based system, each receiver has time synchronization mechanism (for example, Global Positioning System (GPS)) to function

as an internal clock. The master would broadcast a message to receivers through the timing network to generate pulses at a specified time using the internal clock. These two approaches can be combined in the natural accelerator timing system.

3.2 Timing System of Many Facilities

This section gives three timing frameworks in three institutes: J-PARC timing, Micro-Research Finland (MRF) timing for the KEK Linac, and White Rabbit timing for the FAIR accelerator facility in GSI.

3.2.1 J-PARC Timing System

J-PARC timing system started in 2006. At that time, a large number of VME modules and related NIM modules were installed. It is a homemade event-based system [34]. EPICS is used for low-level software development. High-level applications are developed with JAVA in JAEA and with Python in KEK (see also in Chapter 2.4) [35].

The hardware structure of the J-PARC timing system is shown in Fig. 3.1. It consists of one transmitter module and approximately 200 receiver modules. There are three "base signals" in J-PARC timing system: 12 MHz master RF signal (CLK), 25 Hz trigger clock signal (Trig), and event code (type-code, Type).

The CLK is provided by a commercial high-stability function generator. The Trig is generated from the CLK and used for the start signal of every 25 Hz rapid cycle. The event code is a 31 bit number, which has information on beam destination and beam parameters, generated by the transmitter module and sent to all of the receiver modules at a 25 Hz rate. A fiber-optic network and several optical-to-electrical (O/E), electrical-to-optical (E/O) modules are used for signal transmission from Central Control Building (CCB) to many facility buildings. The receiver module receives event codes and then generates delayed trigger signals or gate signals at the 10.4 ns accuracy. These signals are used that each component of the accelerator runs at the specified time [35].

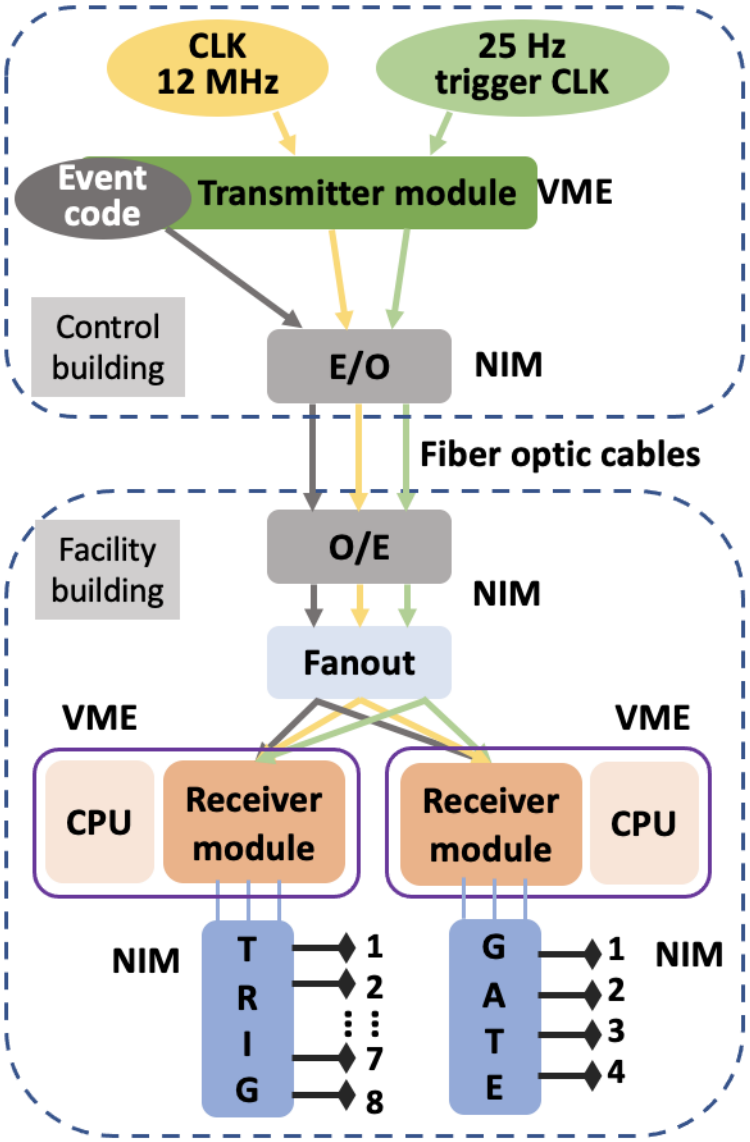

FIGURE 3.1: The hardware structure of J-PARC timing system.

3.2.1.1 New Timing System in J-PARC

Even though the original timing system has been running without significant problems since 2006, the optical transceiver parts used in the O/E and E/O modules were discontinued. This fact makes the system difficult to maintain.

To proceed scheduled replacement of old modules with new ones, a next-generation timing system has been developed [36]. The structure of the new timing system is shown in Fig. 3.2. It is designed to have compatibility with the present system. The new timing

transmitter module serializes three "base signals" into one optical serial line. For high-speed serial communication, a Small Form-factor Pluggable (SFP) optical transceiver is introduced as the standard optical device. The new transmitter module generates the optical signal and distributes it to the new receiver modules via the new optical fanout modules.

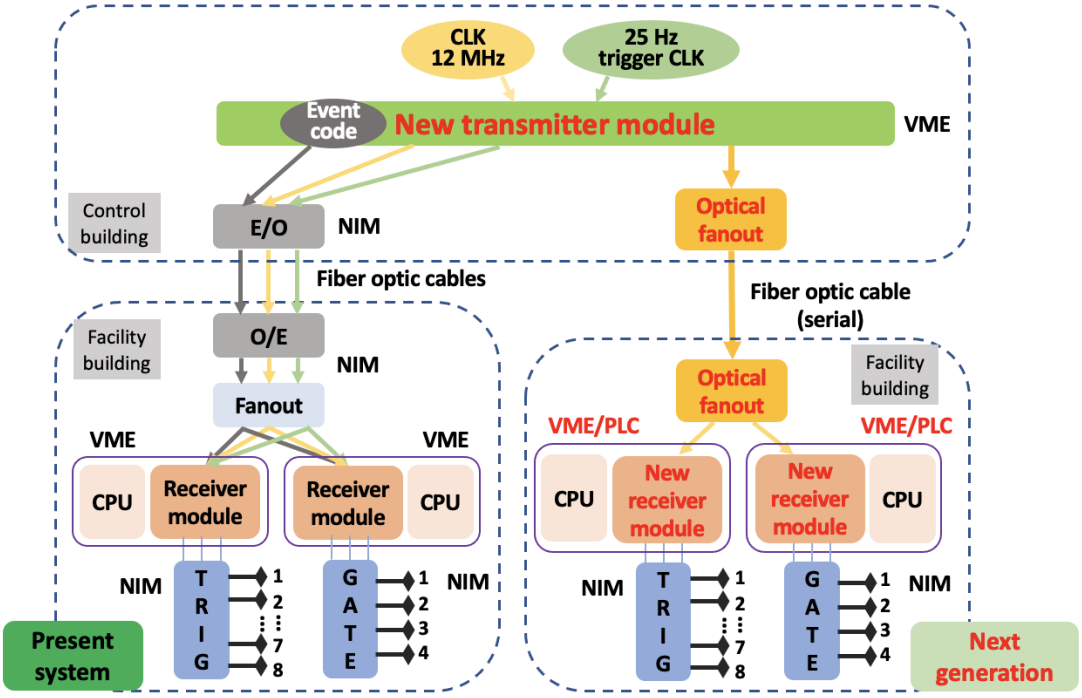

FIGURE 3.2: The structure of next-generation timing system.

Deployment of the next-generation modules is already started. The new transmitter module was introduced in 2019. As of June 2021, 61 (8) new receiver modules were replaced by new ones in LI (RCS). Roughly half of the LI modules were replaced already.

3.2.2 KEK Linac Timing System

KEK Linac is operated as an injector to five different circular accelerators: SuperKEKB High Energy Ring (HER), SuperKEKB Low Energy Ring (LER), Photon Factory (PF) ring, PF-AR, Positron Damping Ring (DR). KEK Linac timing system is dedicated to supporting multiple beam modes and is used to synchronize the circular accelerators [37]. The beam repetition rate in Linac is 50 Hz, and beam mode should switch every 20 ms [38].

An event-based timing system with the MRF products was introduced to KEK Linac. The MRF timing system consists of two kinds of modules: the "Event Generator (VME-EVG-230)" module and the "Event Receiver (VME-EVR-230-RF)" module. The system uses optical fiber to transmit a 16 bit word at a frequency between 50 MHz and 142 MHz by 8b/10b encoding. The rate of event clock is 114.24 MHz in Linac; the bit rate of the event link is about 2.3 Gbps [39]. All 256 event codes are user-defined, except for some special functions. After receiving the event codes, each EVR generates a pulse with a specified delay. The software of the MRF timing system is well integrated with EPICS by using device support module [40]. The KEK Linac timing system structure with RF signals is shown in Fig. 3.3. Details are given in [37].

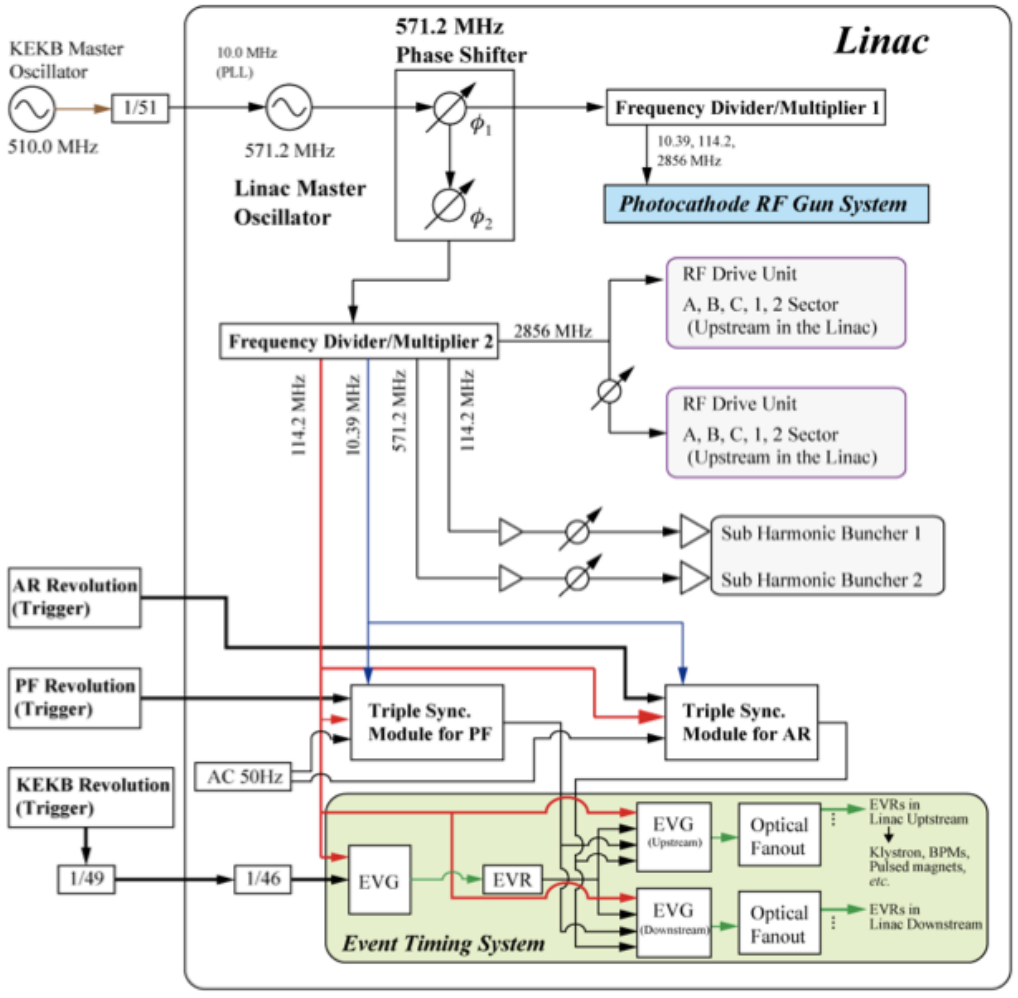

FIGURE 3.3: The structure of KEK Linac timing system with RF signals (Quoted from [37]).

3.2.3 FAIR Timing System

Facility for Anti-proton and Ion Research (FAIR) [41] is under construction at GSI, which is located in Darmstadt, Germany, as one of the most extensive and most complex accelerator facilities in the world. The structure of FAIR facilities is shown in Fig. 3.4. The heart facility of it is a ring accelerator, SIS100, which circumference is 1100 m (Fig. 3.5). Several storage rings and experimental facilities are connected to the primary ring accelerator.

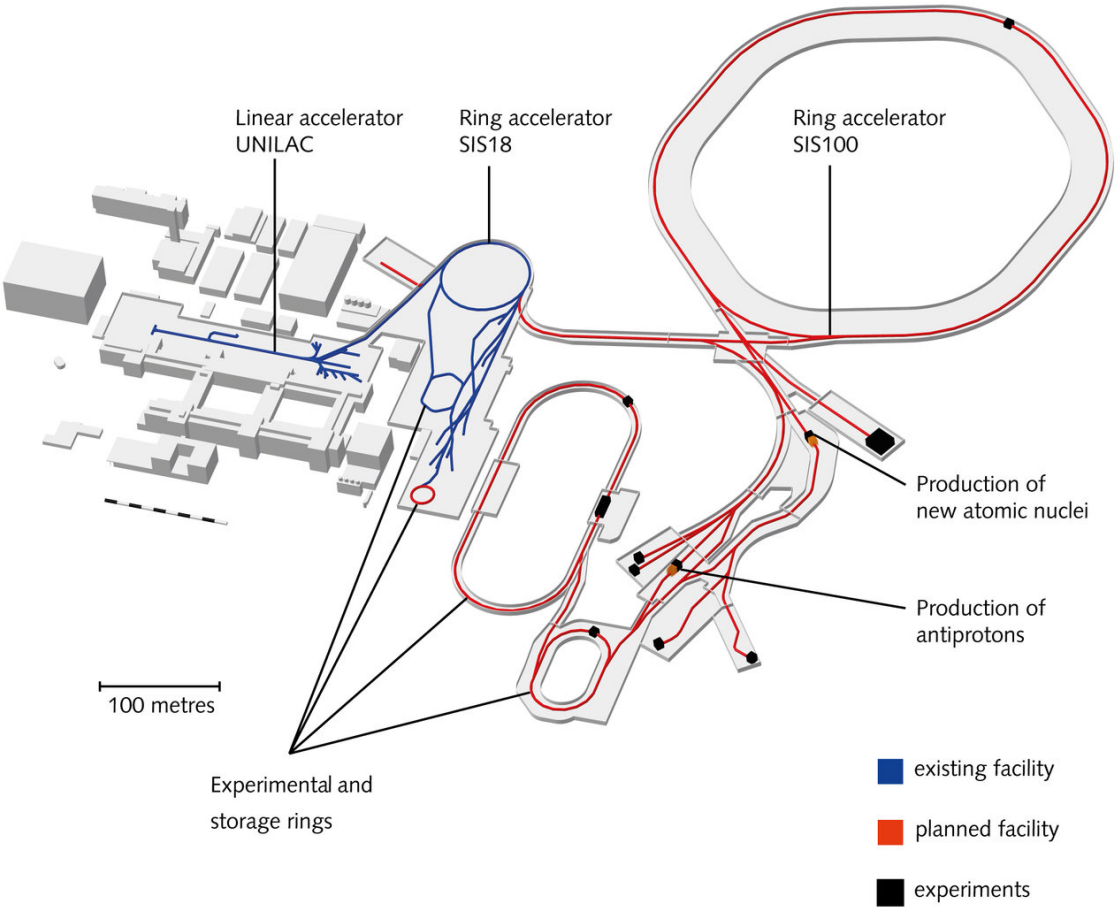

FIGURE 3.4: The structure of FAIR accelerator facilities (Quoted from [41]).

FIGURE 3.5: SIS100 under construction in June 2019.

Since the FAIR facility is made up of several accelerators, and all of them need to be closely synchronized, which is called "General Machine Timing (GMT) system," is used to trigger and synchronize the accelerator components with specific accelerator cycles [42]. The time-synchronization of 2000-3000 nodes with sub-nanosecond accuracy is the main task of the timing system [43]. Fig. 3.6 shows the structure of the GMT system.

The critical components of the GMT are Clock Master (CM), a Data Master (DM), a White Rabbit (WR) network, and Timing Receiver Nodes (TRN) [44].

The CM is the source of time and frequency for the timing network. It uses 10 MHz and pulse-per-second signal from a Global Positioning System (GPS) receiver and the Coordinated Universal Time (UTC) for the synchronization of the network.

The DM controls the accelerator facilities in hard real-time by broadcasting timing messages via the dedicated timing network.

WR relies on the PTP (Precision Time Protocol) to synchronize nodes with sub-nanosecond accuracy [42, 45]. The WR network has high-accuracy timing distribution and provides synchronization propagation and transports timing messages to the timing receivers, using network switches dedicated for WR and fiber optic cables. It has been demonstrated that sub-nanosecond synchronization with jitter in the pico-second range is achieved over distances of a few kilometers and across WR switches [46].

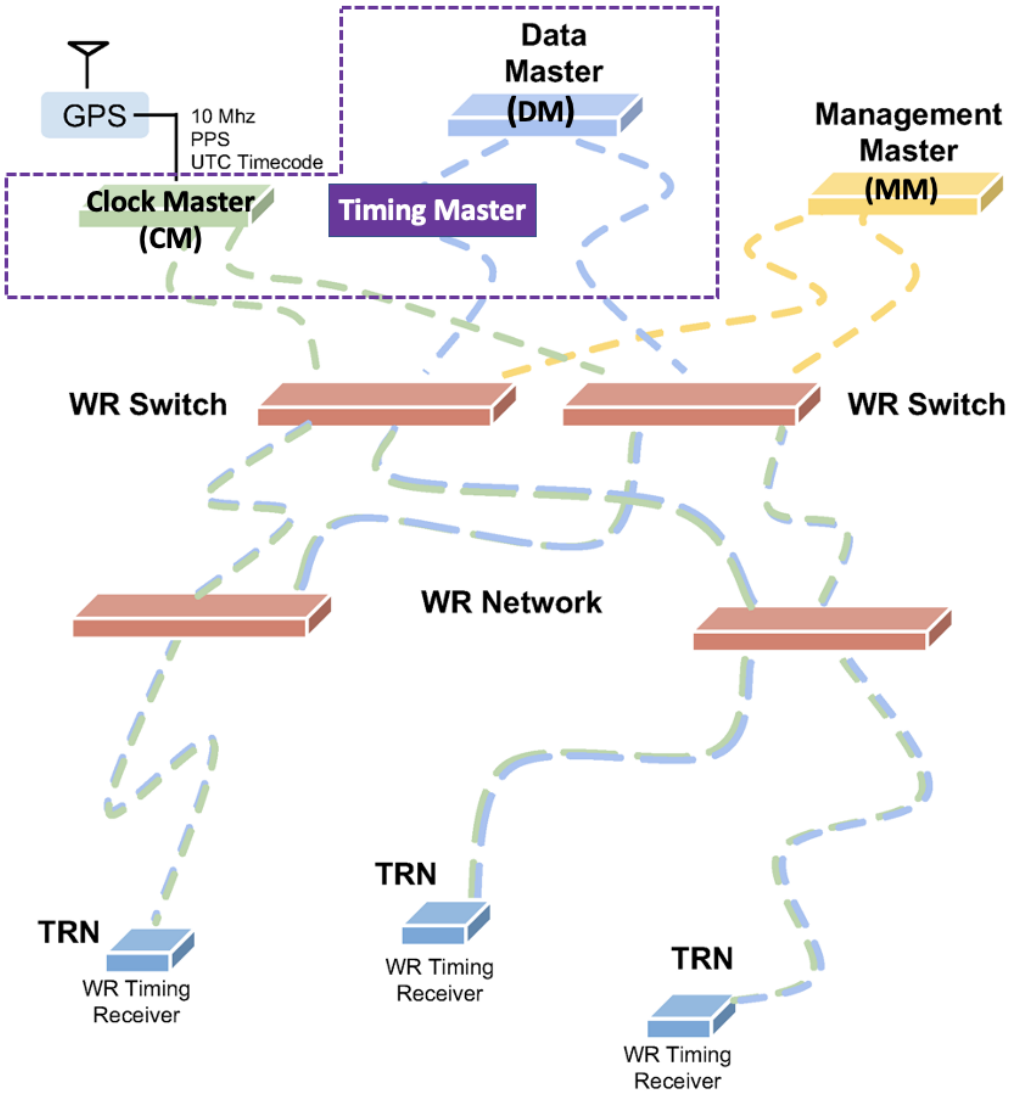

FIGURE 3.6: The structure of the general machine timing system (Quoted from [42]).

The TRN receives timing messages and executes machine-relevant actions on time.

The Management Master (MM) in the Fig. 3.6 serves IP addresses to the management port of WR switches and WR nodes using the Bootstrap Protocol (BOOTP) [47].

3.3 Summary

This Chapter introduced three types of accelerator timing systems: J-PARC timing system, KEK timing system, and FAIR timing system. Each of them has its characteristics. The first and the second systems are event-based, while the third one is a time-based system. Table 3.1 shows a summary of three timing systems.

TABLE 3.1: The comparison of J-PARC timing system, KEK timing system, and FAIR timing system.

	Hard -ware; Form -factor	Scale; Operation	Accuracy; Jitter	Master clock; Master trigger	Event generator; Event ID
J-PARC	Home -made; VME, PLC	200 receivers; Since 2006	10 ns; <1 ns	12 MHz; 25 Hz	A timing master; Type code (31 bit)
KEK Linac	MRF; VME	20 EVRs; Since 2008	- 30 ps	114.24 MHz; 50 Hz	EVG modules; Event code (8 bit)
FAIR	WR; Home -made	2-3k nodes; Test since 2015	sub-ns; ps	10 MHz; -	Data manager; ID in a timing message

J-PARC timing system is specially designed for J-PARC accelerators. Compared to the MRF timing system, it has only one master module with many event-sequence buffers depending on the needs. The master module is placed at CCB, but the receiver modules are scattered at each facility building. This may cause data transmission problems that are not easy to be found remotely.

The KEK timing system is an MRF-based system, which is general and widespread in the current accelerator timing field. The EVG and EVR are placed at different places that may cause data transmission problems.

The FAIR timing system is a WR-based system, which can achieve nanosecond accuracy requirements. The time synchronization of distributed TRNs is based on the WR's PTP protocol, with which we can avoid long-distance transmission problems effectively.

Part II

Problem Analysis

Chapter 4

J-PARC Timing Trigger-Failure Events Case Study

4.1 Overview

Since 2006, some trigger-failure events have occurred during the J-PARC beam operation. Herein, four cases are introduced: an irregular trigger event and three missing trigger events.

4.2 25 Hz Irregular Trigger Event

From November to December in 2016, the accelerator operation was suspended a few to ten times per day [48], because of the faults of a beam diagnostic system, which is located on the MR injection transport line (350BT). The position of the beam monitor is shown in Fig. 4.1. Table 4.1 shows the number of MPS events per shift (8 hours) from November 22nd to December 1st, which corresponds to the numbers of operation suspensions.

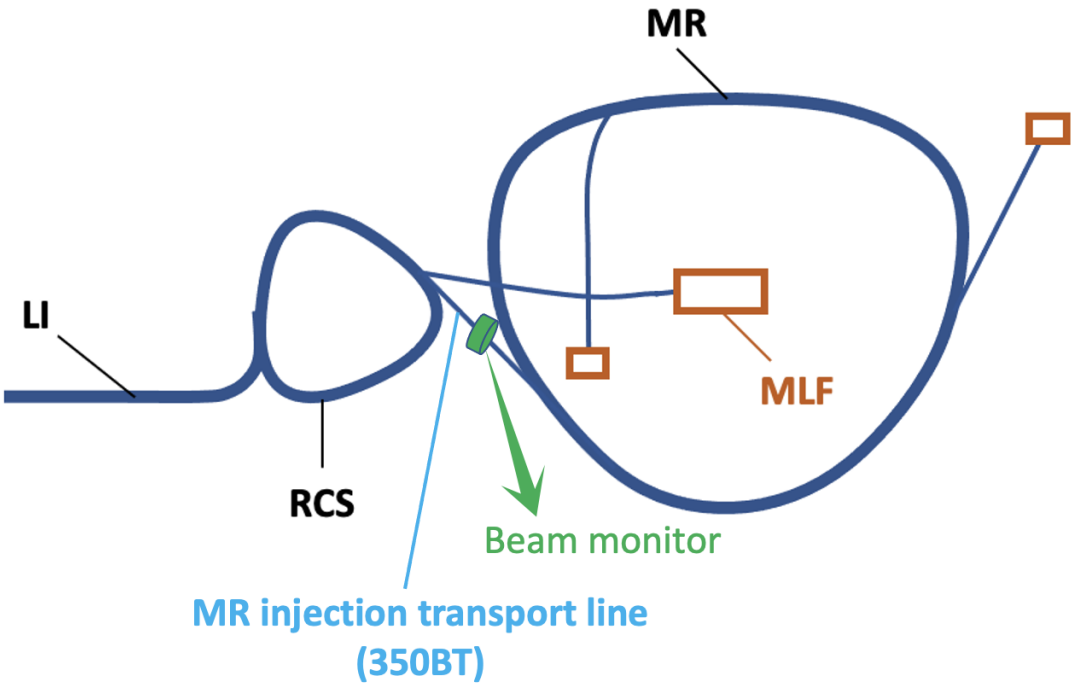

FIGURE 4.1: The position of beam monitor on the MR injection transport line (350BT).

TABLE 4.1: Number of MPS events during November 22th to December 1st, 2016

	1:00-9:00	9:00-17:00	17:00-1:00
11/12	0	1	1
11/23	3	0	0
11/24	0	0	0
11/25	0	0	0
11/26	1	2	1
11/27	1	0	0
11/28	0	0	1
11/29	10	6	0
11/30	2	1	0
12/01	6	8	problem solved

A 25 Hz trigger signal used for the data acquisition of a critical beam monitor caused the faults. The transmission path of the signal is very long (about 2 km), from RCS to the D1 (the first power supply building of MR), through the CCB and the D3 (the third power supply building of MR). It was challenging to find the defective module among many candidates at different buildings. An oscilloscope was used to check the trigger signal to determine the specific module that caused the problem. However, the rate of MPS

events was low before November 28th. Since November 29th, the MPS events became more frequent, and the oscilloscope observed irregular pulses as shown in Fig. 4.2.

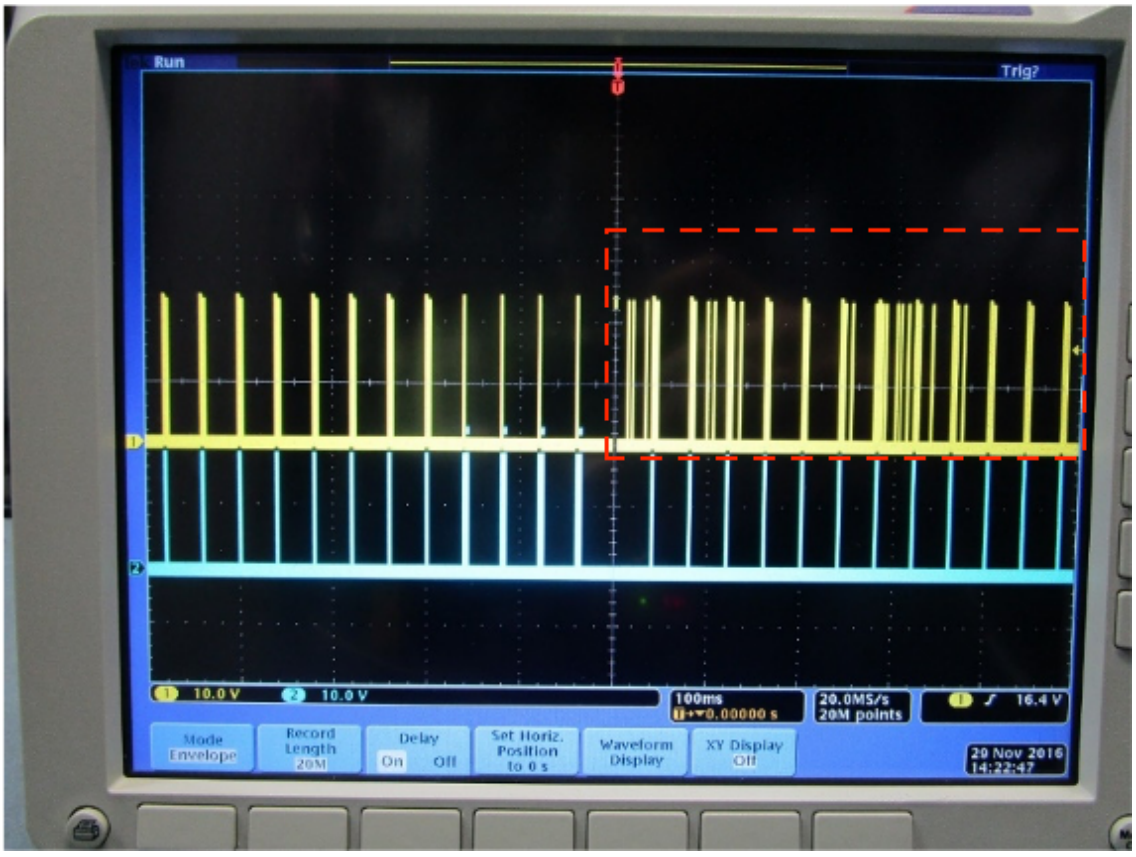

FIGURE 4.2: Irregular 25 Hz trigger signal observed with the persistence mode of an oscilloscope.

After two weeks of troubleshooting, an O/E module in RCS, which was used to send 25 Hz trigger signal from RCS to MR, was identified to produce irregular triggers. The problem was then solved by replacing the faulty O/E module.

4.3 Pulsed Bending Magnet Stopped Trigger Event

Since the J-PARC timing system started in 2006, hundreds of NIM modules have been introduced. Among them, about 120 O/E modules have been used in MR. Between 2010 and 2018, there were 14 cases in MR that a fuse in the O/E module was broken suddenly. The frequency of fuse broken per year was zero or one before 2015, but increased to three after 2016. From January to March 2018, the fuse broken happened three times in just

three months, two of which seriously affected the beam operation. In the following, one of the two cases is shown in detail: a broken fuse occurred with the trigger fanout module used for the pulsed bending magnet power supply.

In January 2018, when MR started beam study, the beam that should have reached MR did not arrive, and neither the MPS nor the PPS issued an alert. Upon arrival in the D1 local control room, it was found that the pulsed bending magnet power supply was not triggered. Investigation revealed that the fuse in the trigger fanout module (RPN-1060) was blown out (Fig. 4.3).

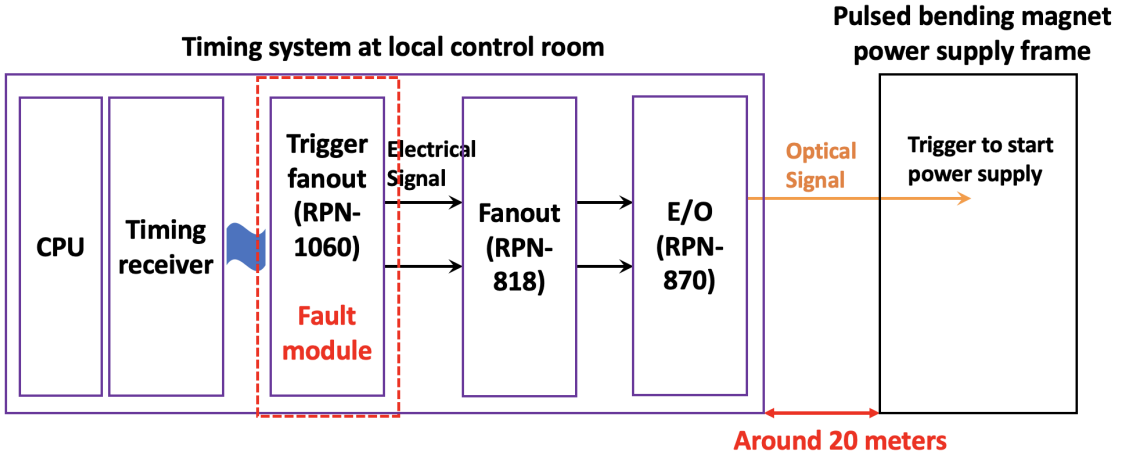

FIGURE 4.3: The transmission path of trigger signal for pulsed bending magnet power supply.

Because the pulsed bending magnet is used for beam switching between MLF and MR, the beam was misdirected to MLF directly. Although the low-intensity beam study did not damaged the MLF target, it could be dangerous if it happened at high beam intensity.

After this event, the fuses of all the 120 O/E modules in MR have been replaced one by one manually (one example is shown in Fig. 4.4). The replacement of the module fuses took about two years from 2018.

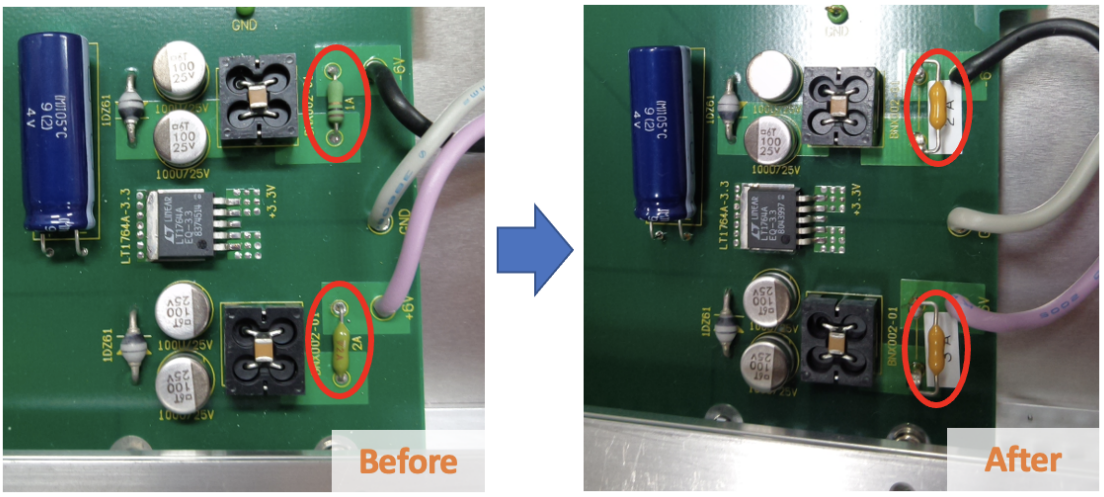

FIGURE 4.4: The pictures of fuses before and after replacement for an optical transmitter module (RPN-1130).

4.4 Steering Magnet Missing Trigger Event

The third event is a missing trigger event that occurred in November 2015. A bad quality beam appeared during stable beam delivery to HD [48]. The "bad quality" here means that the beam size was slightly larger than usual but still tolerable for experiments.

Since November 2015, there have been rare instances of beam size enlargement during beam delivery to HD. At that time, the beam loss monitor of MR did not issue an MPS event. Later analysis showed that the size of closed orbit distortion (COD) increased with acceleration. Fig. 4.5 shows an example of COD during beam operation in April 2016. During stable beam operation, the beam remains centered and stable in orbit. When a missing trigger occurs, the beam deviates from the center of the orbit.

Such beams appeared between November 2015 and May 2016, sometimes a few times per month, sometimes without a problem for a month [49] (see Table 4.2). Based on the analysis of COD, the problem was presumed that a part of steering magnets was not triggered.

Initially, it was suspected that there was a problem with the trigger signal transmission path (such as cables, O/E module, and others). Therefore, the troubleshooting of the transmission path started from top to end. The timing receiver module, E/O, and O/E modules, and connection cables showed in Fig. 4.6 were replaced step by step, but to no avail. The big steering trigger unit was also replaced finally, but the result was the same.

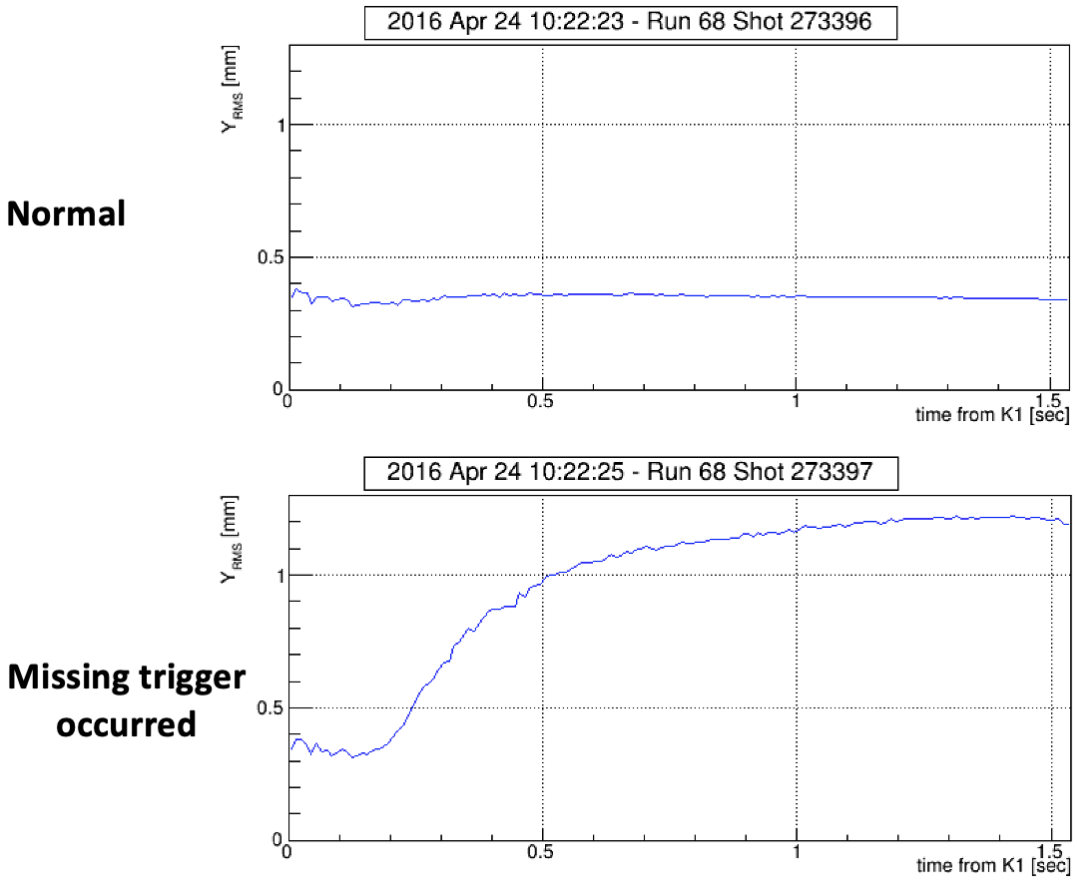

FIGURE 4.5: Comparison of normal and abnormal state of RMS COD along Y axis.

TABLE 4.2: Times of missing trigger events during November 2015 to May 2016.

Year/Month	Times
2015/11	4
2015/12	0
2016/01	0
2016/02	0
2016/03	Few
2016/04	5
2016/05/25	Problem solved

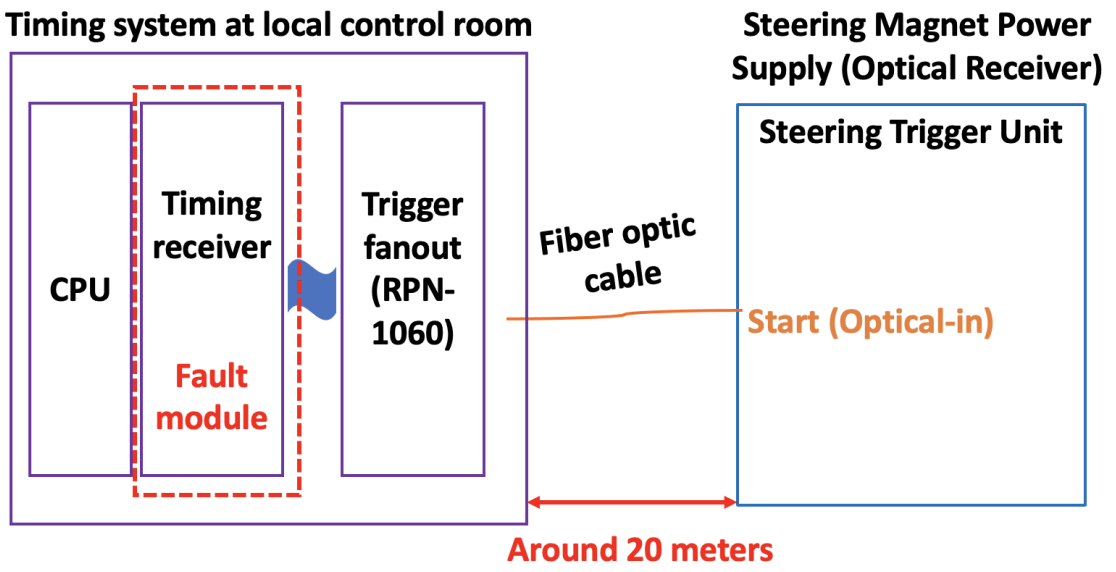

FIGURE 4.6: The transmission path of trigger signal for steering magnet.

In May 2016, a timing receiver module for MR steering magnets was found to show momentary errors and caused missing triggers. These momentary errors were not well checked before 2016. After retrieving the timestamps of errors from the archive system, it was found that the timestamps of errors agreed with the timestamps of bad beams. It was finally determined that the external common-mode noises caused the errors. After adding ferrite cores to metal cables connected to the receiver module, the problem never arose again. It took half a year to solve the problem completely.

4.5 Suspected Optical-Gate Signal Event

The fourth event is a suspected optical-gate signal event. In the summer of 2020, 41 of the 96 fuses for bending magnet trim-coil short systems were broken.

Fig. 4.7 shows the circuit of the trim-coil short system. Each of 96 bending magnets has a trim-coil short circuit to reduce the magnetic field ripple [50]. An optical gate signal is used to control the switch of the circuit.

There is one possible reason for fuses broken, a shifted gate or a missing stop signal might occur during beam operation in June 2020. Such faulty signals may blow out fuses in the circuits. However, the cause of the blown fuses has not been found yet.

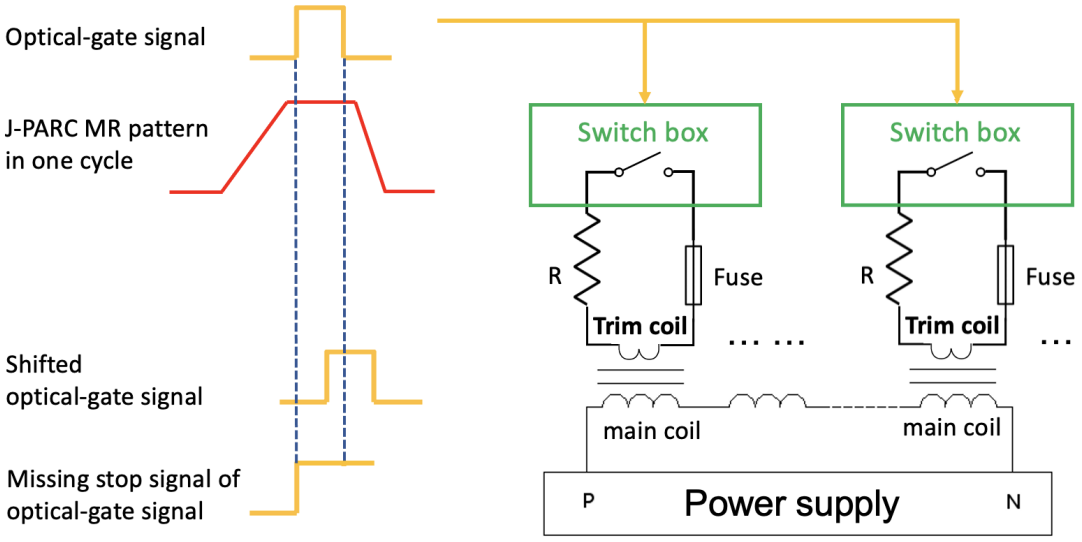

FIGURE 4.7: Circuit of trim-coil short system.

4.6 Discussion

Table 4.3 shows the summary of four trigger-failure events.

TABLE 4.3: Summary of four trigger-failure events.

Date	Type of Event	Origin	What we did
2017.11 -2017.12	Irregular trigger of 25 Hz trigger	An O/E module (generated noisy pulses)	The module was replaced
2018.01	Stopped trigger of pulsed bending magnet	An O/E module (fuse broken)	The module was replaced
2015.11 -2016.05	Missing trigger of steering magnet	A timing receiver (external noises)	Ferrite cores were added to metal cables
2020.06	Suspected optical -gate signal	Not clear	Need more investigation

The first and second events were caused by an O/E module. They are critical to accelerator operation and severe concern about the beam-switching function between MLF and MR, especially pulsed bending magnet case. Both of them showed no alert from the timing system or the control system. Thus, it was unable to find them from the control room remotely.

The third event was not much damage to accelerator operation, but it was challenging to detect such low-rate errors, and difficult to search for the trouble source from many candidates. Without experience, it may take a long time to troubleshoot the equipment and cables progressively.

The source of the fourth event is not found yet. The optical gate signal is suspected, and more investigation is needed.

The above-experienced events showed that the existing system could not help to find a trouble source, especially the missing trigger in case three. Thus, it concludes that it is inevitable to develop a read-back system to check the timing signals, detect the trigger-failure events, and help quickly determine the problematic modules. The read-back system is expected to reduce the occurrence of similar operation events mentioned and ensure regular and stable accelerator operation.

Chapter 5

Technology Survey

5.1 Overview

This Chapter focuses on two existing read-back systems: an injection kicker TDC-MPS system in J-PARC and a 50 Hz dropout monitor system in KEK. Then, an introduction to the triggered scaler module is given, followed by a discussion part.

5.2 Injection Kicker TDC-MPS System at J-PARC

This section refers to a presentation, "Update of Kicker TDC-MPS," from Takuya Sugimoto in 2021 [51].

5.2.1 Motivation

In the past, components of the injection kicker system of J-PARC MR were sometimes damaged: for example, a high-tension cable punctured, or a resistor damaged, as shown in Fig. 5.1.

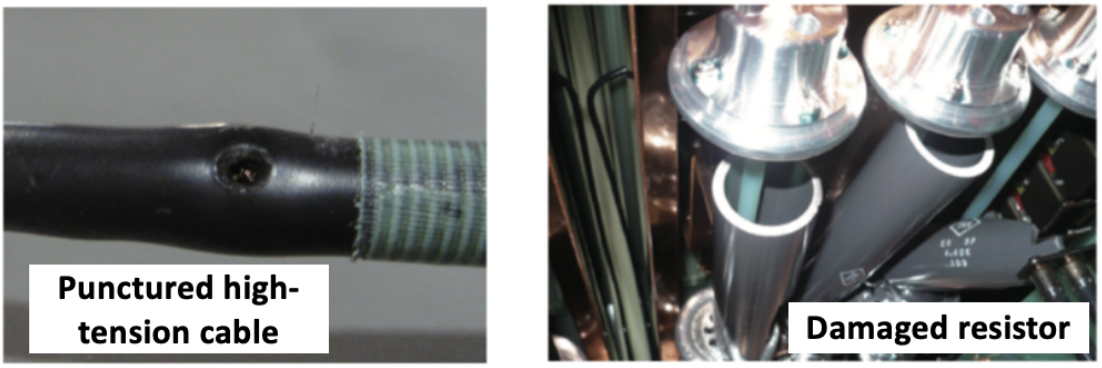

FIGURE 5.1: The high-tension cable puncture event and punctured high-tension cable and damaged resistors (Quoted from [51]).

These events were caused by various reasons: aging of a register, sudden discharge of a thyratron, miss-function by external noises, and so on. Such faults must be detected as soon as possible to generate an MPS event. Thus, a TDC-MPS system was developed around 2012.

5.2.2 System Introduction

TDC is Time-to-Digital Converter, which is important for measuring time interval between two signals. The hardware configuration of the TDC-MPS system is shown in Fig. 5.2. The output signal of an injection kicker is measured by a current transformer (CT), then converted to a TTL output signal. The system accepts eight output signals in total from the injection kickers.

The system consists of a PLC ladder-based MPS system and an IOC where the EPICS Sequencer program runs. The working principle is shown in Fig. 5.3. When the "S" signal (the start of machine cycle) arrives from the timing system, the counter inside the PLC is reset, and starts to count 1 kHz internal clock. When the PLC detects the first pulse from an injection kicker, it copies the number of clock pulses into the PLC data register (D0101, etc. in Fig. 5.3). Thus, this system behaves like a TDC with 1 ms time resolution. The EPICS Sequencer program works to get measured values from the PLC data register and compare the latched value with the standard timing value. If the difference is not 0, the total system will generate an MPS signal.

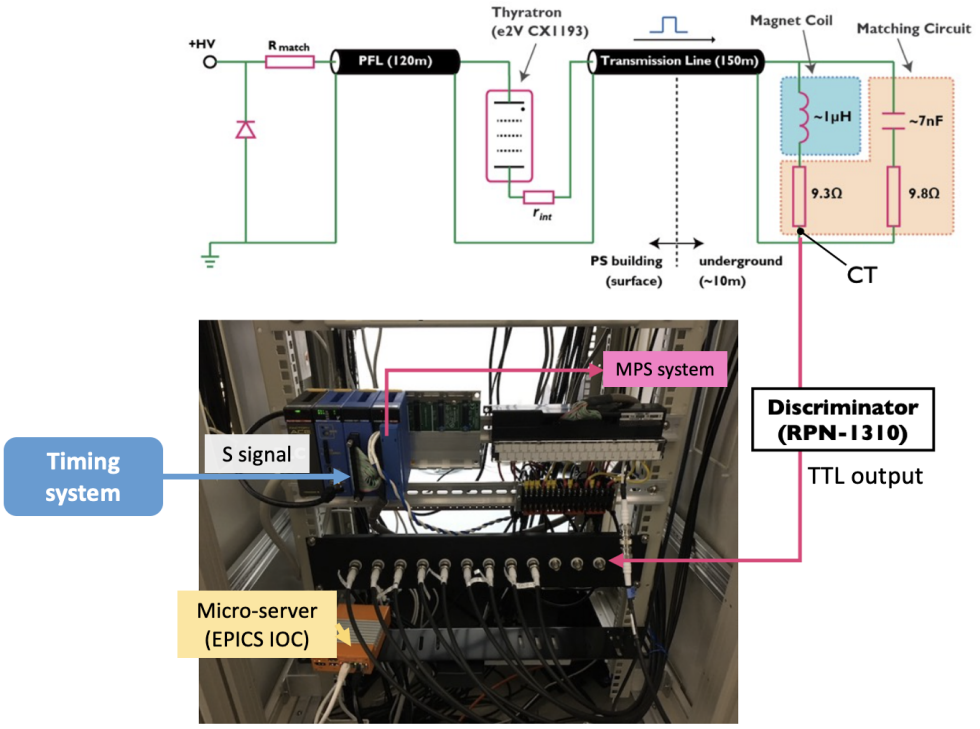

FIGURE 5.2: The hardware configuration of injection kicker (upper) and the TDC-MPS system (lower) (Quoted from [51]).

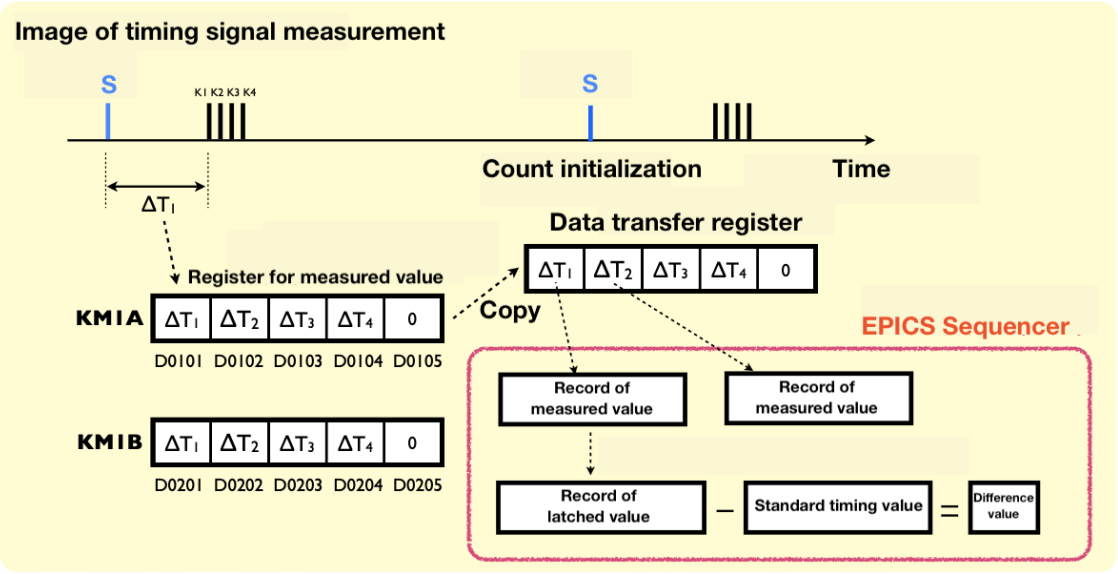

FIGURE 5.3: The working principle of kicker TDC-MPS system (Quoted from [51]).

5.3 50 Hz Dropout Monitor System at KEK

This section refers to the presentation, "50 Hz dropout monitor," presented by Kazuro Furukawa in 2004 [52].

5.3.1 Motivation

From 2000 to 2002, a missing signal for delay modules was often found. However, the event occurred only once every two weeks. Since most modules were free of problems and the frequency of the occurrence was low, it was difficult to pinpoint the problem among many modules. There were many TD4/TD4V modules [53], which generated delays with a few nanosecond time resolution. Finally, in the summer of 2002, comparators used in the TD4/TD4V modules were found to be defective, then all of the comparators were replaced. Based on this experience, the 50 Hz dropout monitor system was developed. Another motivation is to monitor the 50 Hz signal without signal stacking.

5.3.2 System Introduction

The hardware of the 50 Hz dropout monitor system, which is a NIM-type module, is shown in Fig. 5.4.

FIGURE 5.4: The hardware of 50 Hz dropout monitor system (Quoted from [52]).

The NIM module has two input channels. TTL and NIM signals can be accepted. The power supply of the system is a NIM bin or 12 V AC adapter. The frequency mode can be selected to 50 Hz or 25 Hz. Pulse intervals from 19 ms to 21 ms in 50 Hz mode (from 39 ms to 41 ms in 25 Hz mode) are allowed, otherwise the system arises an alert. The system is able to detect the substandard timing signals, missing triggers, and so on. Fig. 5.5 shows the system GUI developed by Python script.

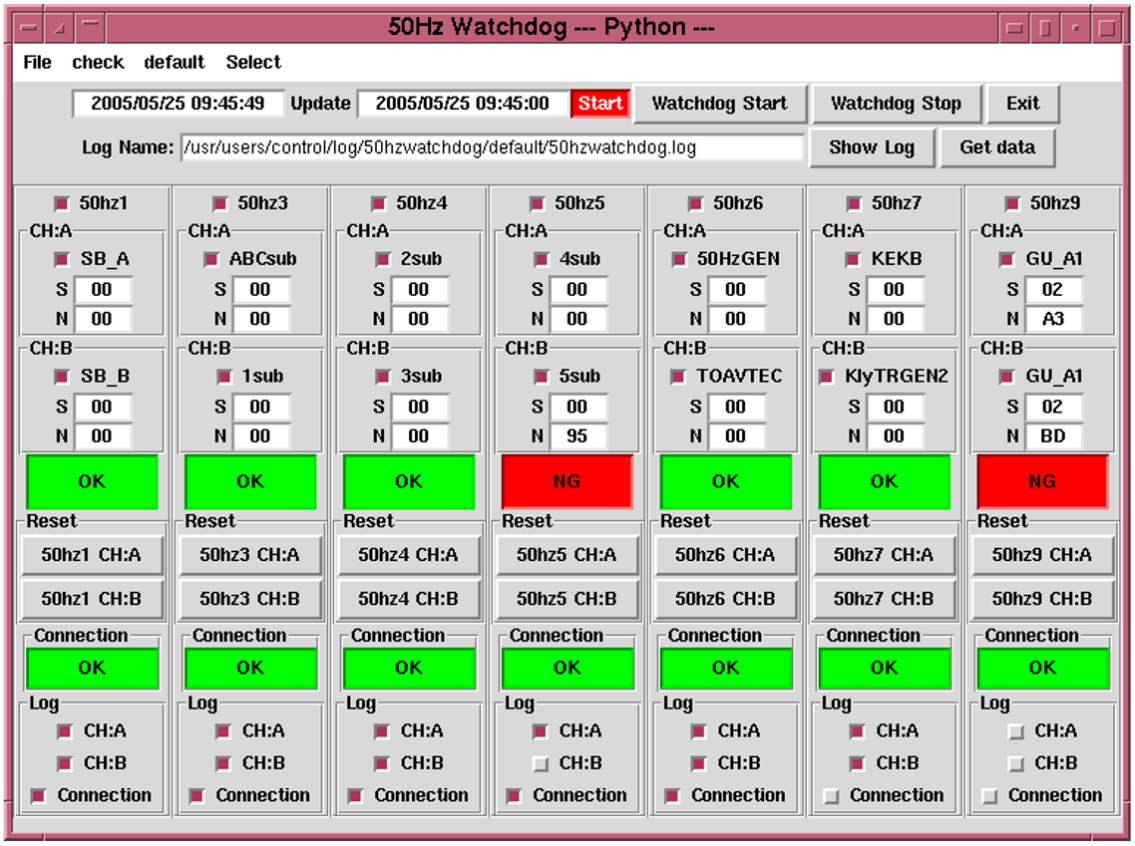

FIGURE 5.5: The GUI screenshot of 50 Hz dropout monitor system (Quoted from [52]).

5.4 Triggered Scaler Module

5.4.1 Overview

A triggered scaler (hereafter TS) was designed by J-PARC control group for reading back timing signals. It is a scaler to count number of pulses in a specified accelerator cycle, and it stores the counts in a momentary array [48, 54].

This Chapter 5.4 mainly introduces the details of the triggered scaler module. The hardware design and software design with the working principle are given. The performance tests with accelerator signals are presented. At last, a discussion is given. Most of the contents in this Chapter are the works by the J-PARC control group before 2018.

5.4.2 Module Design

5.4.2.1 Hardware Design

The triggered scaler module was designed as a Yokogawa (FA-M3/e-RT3) PLC-type, to fit the standard I/O form in J-PARC MR. There are two types of the module: the MR-type and the LI-type. The hardware appearances of two types are shown in Fig. 5.6.

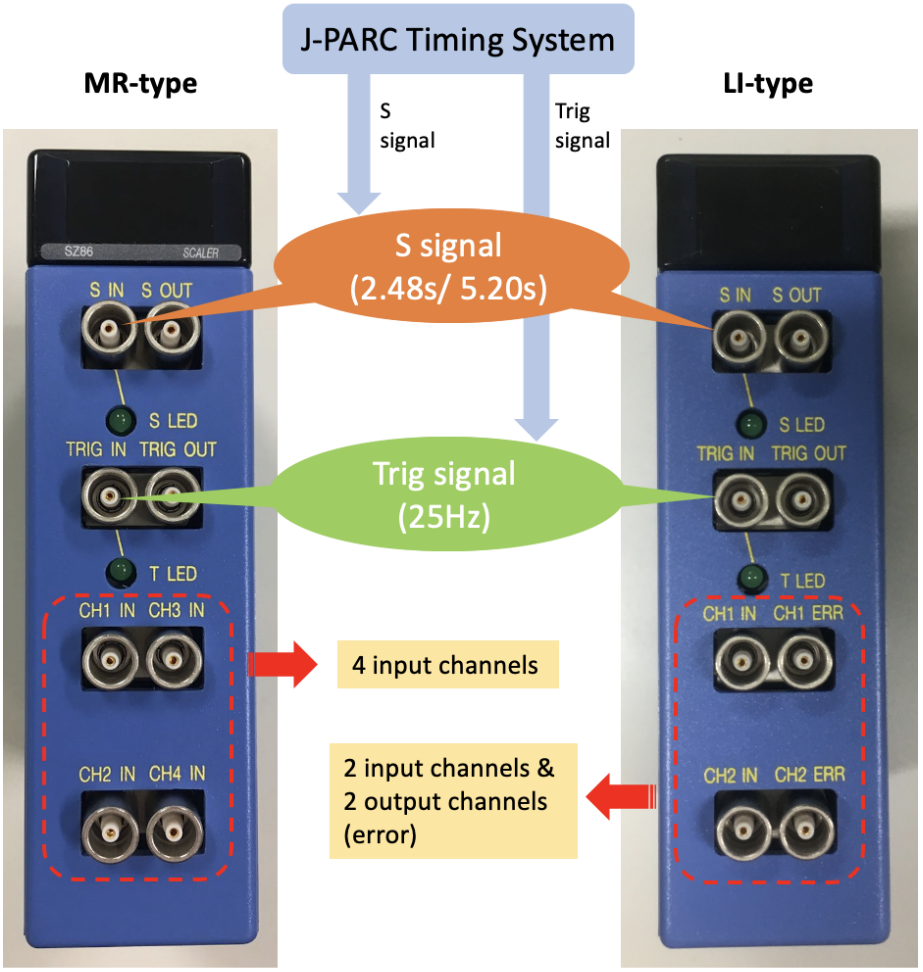

FIGURE 5.6: The hardware appearances of two types of TS module.

The LI-type TS module was designed to find a missing trigger event of the LI accelerator. The module checks the pulse count in the rapid cycle (25 Hz), and raises an error flag when an error is detected. In turn, the MR-type checks the pulse counts in the last slow cycle (2.48 s or 5.20 s). Both require the start signals of the slow cycle and the rapid cycle, provided by the J-PARC timing system. The MR-type has four input channels

and no output channel, while the LI-type has two input channels and two error-output channels. There is a dual ring buffer (192 cells × 2 for MR-type, 448 cells × 2 for LI-type, 16 bit/cell) for each channel.

In principle, each channel of the TS module works as a scaler. Two internal FPGA logics are shown in Fig. 5.7. The first logic (FPGA_1) counts the input pulses. When the "S" signal arrives, FPGA_1 starts to increase the count in the first cell of the first memory buffer. Each time the "Trig" signal arrives, FPGA_1 shifts the pointer to the next cell. When the following "S" signal arrives, the pointer is moved to the first cell of the second memory buffer. In other words, each cell keeps several trigger pulses received in a 40 ms bin (as the "Trig" signal is 25 Hz). This scheme enables retrieval of the numbers of counts per rapid cycle during the last machine cycle. The second logic (FPGA_2) reads the memory buffers, checks whether trigger faults exist or not, and sets error flags if necessary. The LI-type module can output an error signal directly through the output channels.

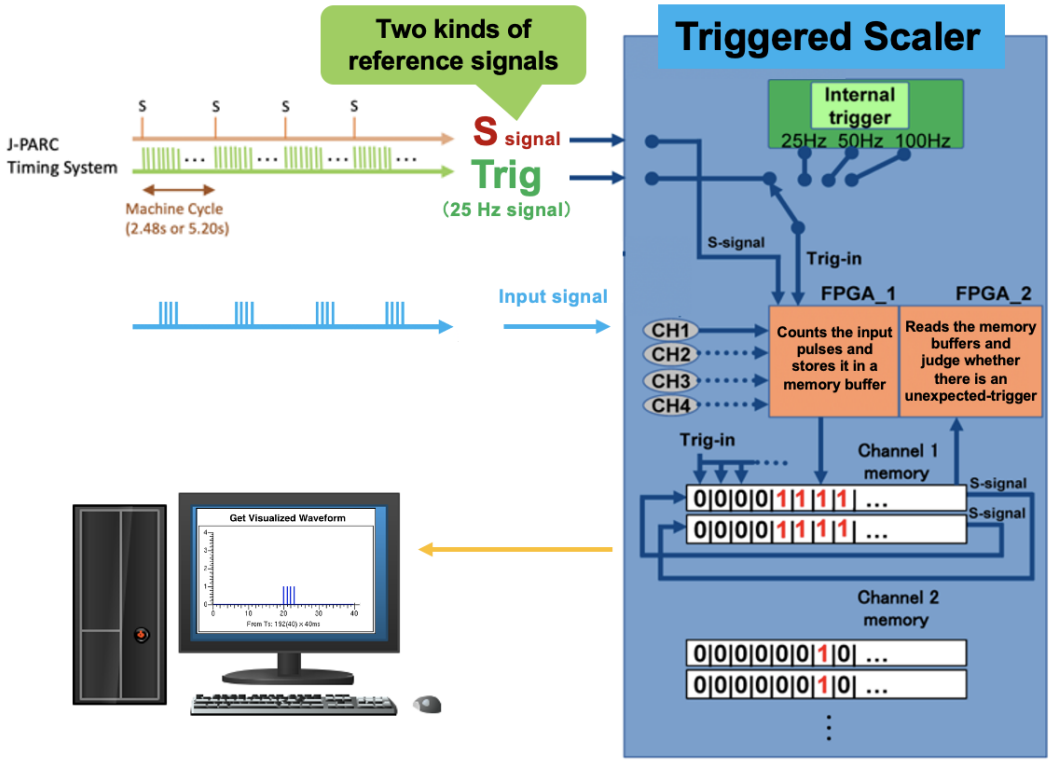

FIGURE 5.7: The image and conceptual design of the triggered scaler module.

Since the work in this dissertation mainly uses the MR-type TS module, the rest will be MR-type unless pointed out explicitly.

5.4.2.2 Software Design

To realize the functionalities of the TS module in the EPICS environment, the fundamental database definitions of the module I/O were developed [55].

To make maintenance easier, a three-layer databases scheme has been developed. The structure is shown in Fig. 5.8. At layer 1, the hardware registers of the TS module are defined. Applications for module maintenance use Layer 1 to monitor the status of hardware registers. Layer 2 has two versions, for MR and LI, respectively. The operation parameters of J-PARC MR and LI are defined. Applications developed for MR or LI operation use Layer 2. Layer 3 is for developing specific applications for unexpected trigger-failure detection or other measurements. The Layer 1 communicates with the hardware, while the other two layers do not access the hardware directly. This scheme makes it possible to develop operational applications without hardware knowledge.

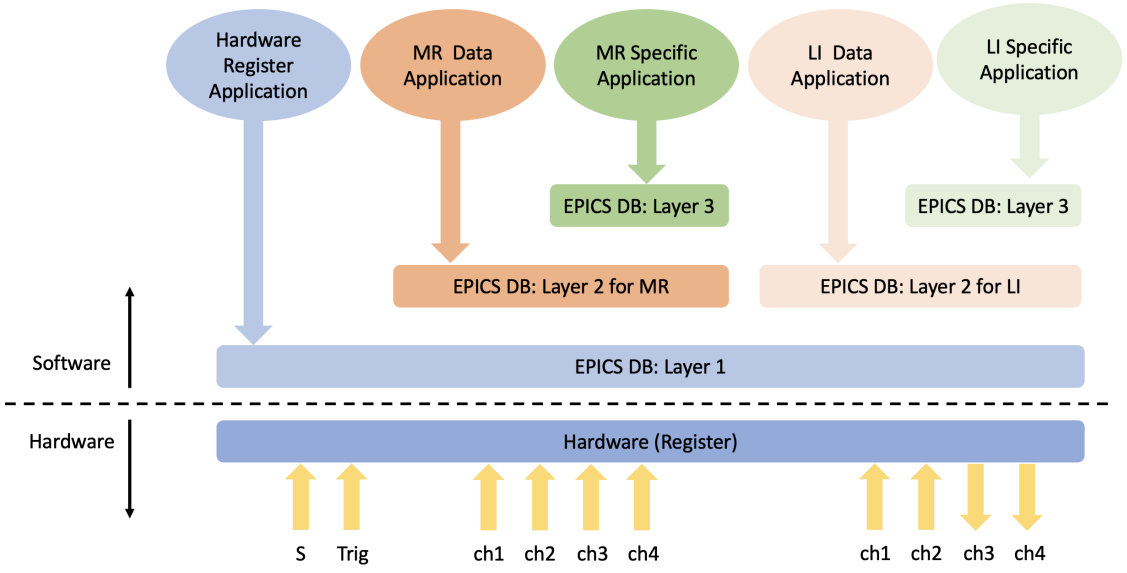

FIGURE 5.8: Three layers of software design for TS module.

5.4.3 Performance

To confirm the performance of the module, a test setup was prepared, as shown in Fig. 5.9. It consists of a CPU module, a TS module, and a power supply module. All of them are standard Yokogawa PLC modules. Linux and EPICS IOC are running on the CPU module. Two measurements were carried out in 2018.

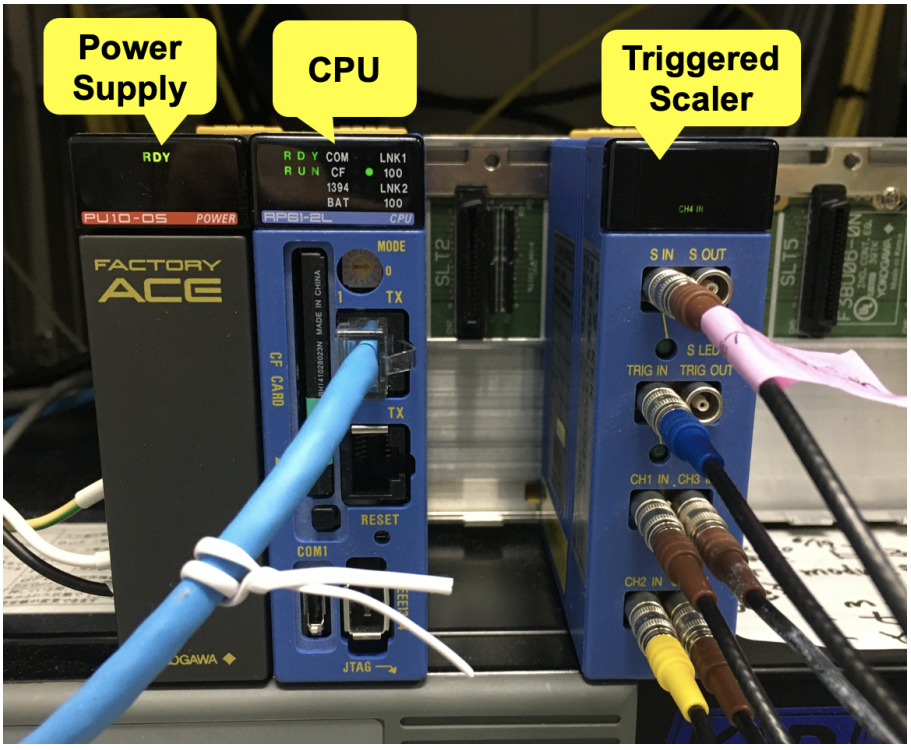

FIGURE 5.9: Measurement setup of TS module.

5.4.3.1 Measurement of An Injection Kicker Signal

A typical timing signal was measured in J-PARC MR: the trigger signal for MR injection kicker. In general, the injection kicker signal injects four times in one machine cycle (see details in 6.2.1). When the signal comes, the scaler in the TS module counts number of trigger pulses and stores them in the dual ring buffer. The EPICS "caget" command prints out the memory buffer data.

As shown in Fig. 5.10 (left), the four successive "1" values were successfully observed in the memory buffer of the module. In addition, the observed values were visualized as a waveform with an EPICS GUI tool, EDM (Fig. 5.10 (right)).

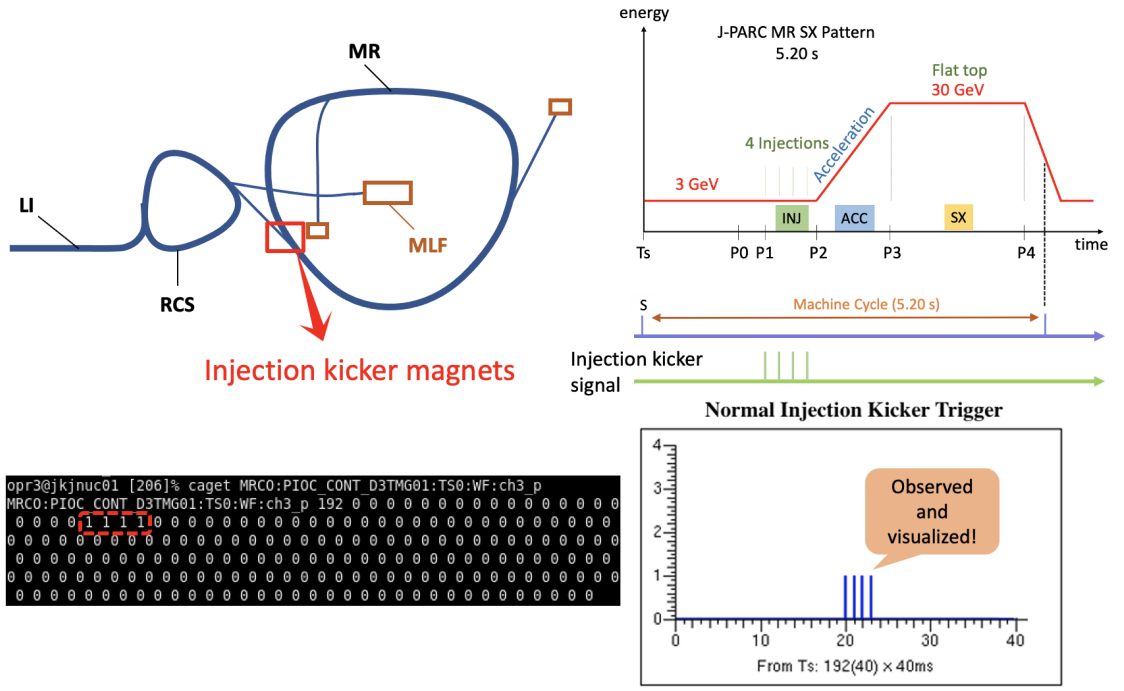

FIGURE 5.10: Measurement of a trigger for MR injection kicker.

5.4.3.2 Measurement of An RF Signal

Following the first measurement, an RF signal (MR circulation signal) generated by a Low-Level Radio Frequency (LLRF) system was measured. The 3 GeV proton beams are injected into MR and then accelerated up to 30 GeV in each machine cycle. Fig. 5.11 shows a visualization of a frequency shift of an RF signal during injection, acceleration, and extraction phases.

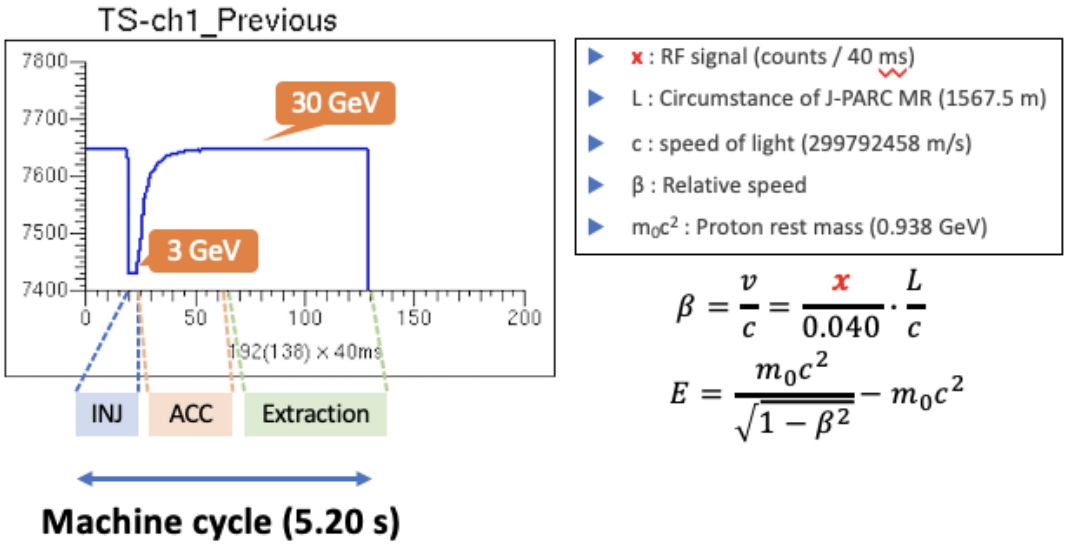

FIGURE 5.11: Measurement of an RF signal.

The number of counts in the 40 ms bin was measured using the TS. When the beam energy was 3 GeV and 30 GeV, 7429 and 7647 counts were observed, respectively. Table 5.1 revealed that the observed counts are consistent with expected counts, which correspond to the beam energies based on the theory of relativity.

TABLE 5.1: Number of counts in 40 ms, expected and observed, at two different energies.

RF parameters			Number of counts in 40 ms	
Energy (GeV)	RF (MHz)	One turn (μs)	Expected	Observed
30	1.7205	5.231	7647	7647
3	1.6717	5.384	7429	7429

5.4.3.3 Summary of Measurements

The first measurement of an injection kicker signal showed that the TS module operated as expected. The second measurement showed that the TS module could read back for the timing signals and other signals, such as the LLRF signal.

Those two measurements demonstrated that the TS module could detect various signals and visualize them based on the relationship with the accelerator cycle.

5.5 Discussion

The first example shows a PLC ladder-based read-back system, which can read back injection kicker signals and identify abnormal signals. One limitation of this system is that it is customized for the J-PARC injection kicker. Therefore, it is difficult to apply it to other purposes or implement other functions.

The second example shows a NIM module for monitoring a 50 Hz timing signal. It is a perfect standard for various high-resolution measurements, and the module can be neatly arranged with other NIM modules. However, it is not as compact and flexible as PLC modules. Moreover, customization using software is less elastic. It is also specially formulated for timing signals and not achieved for other signals.

Following these two systems, a new module, TS module, is introduced. By comparing the previous two systems, it was found that this module is more suitable for developing the timing read-back system of J-PARC. Measurements can be related to the machine cycle and can be visualized easily as a waveform. Customization by software and by adding other I/O modules are also possible. Therefore, the TS module is decided to adopt as a vital device to develop the read-back system.

Part III

Approach and Implementation

Chapter 6

Prototype Timing Read-Back System

6.1 Overview

According to the previous measurement results, it can be proved that the triggered scaler (TS) module has an excellent capability of timing-related signals visualization with a relationship to the accelerator cycle. In Chapter 6, a prototype timing read-back system is discussed. The essence of the system is the routine to detect trigger-failure events based on the injection kicker signal.

This Chapter first introduces careful consideration for the possible trigger-failure events with the injection kicker signal. Then, the development of failure detection routine and test of the prototype system are presented. At last, the possible customized read-back system with the TS module is discussed.

6.2 Background and Motivation

6.2.1 Injection Kicker Signal at J-PARC

The injection kicker system for J-PARC MR has been in operation since May 2008. The position of the injection kicker magnets is shown in Fig. 6.1.

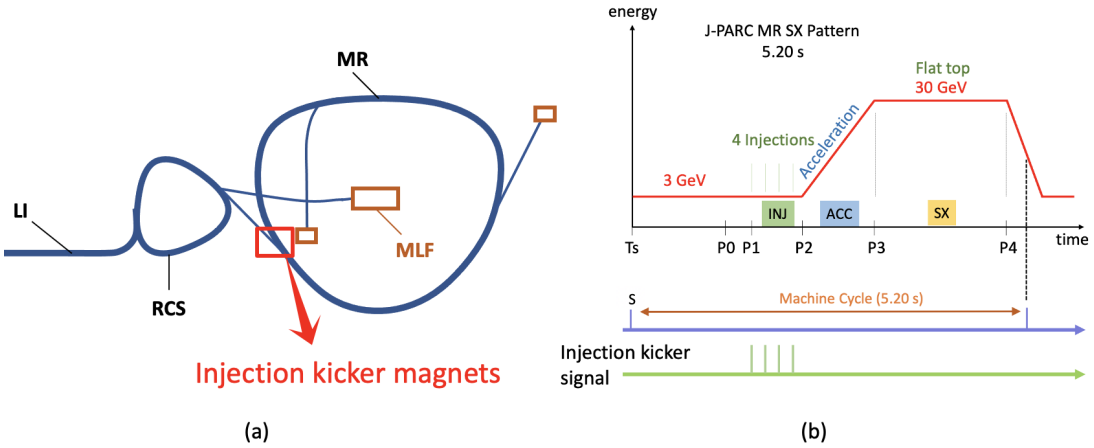

FIGURE 6.1: (a) The position of injection kicker magnets at J-PARC MR. (b) The timing pattern with four injections in J-PARC MR.

The injection kicker system, which employs four lumped kicker magnets, is used to deflect the incoming 3 GeV beam from RCS [56, 57]. As in Fig. 6.1 (b), there are four successive injections from RCS in one machine cycle. Therefore, there are four successive trigger signals. These four triggers are often referred to as the "K1-K4" signal.

6.2.2 Possible Trigger-Failure Events of Injection Kicker Signal

The injection kicker signal plays a vital role in beam injections to MR. Therefore, the failure detection of this signal is critical. There are three possible trigger-failure events, as shown in Fig. 6.2 (b), (c), and (d).

- Fig. 6.2 (a) shows a normal signal, which is four successive triggers.

- Fig. 6.2 (b) shows a missing trigger event. This means that one (or more) trigger disappears.

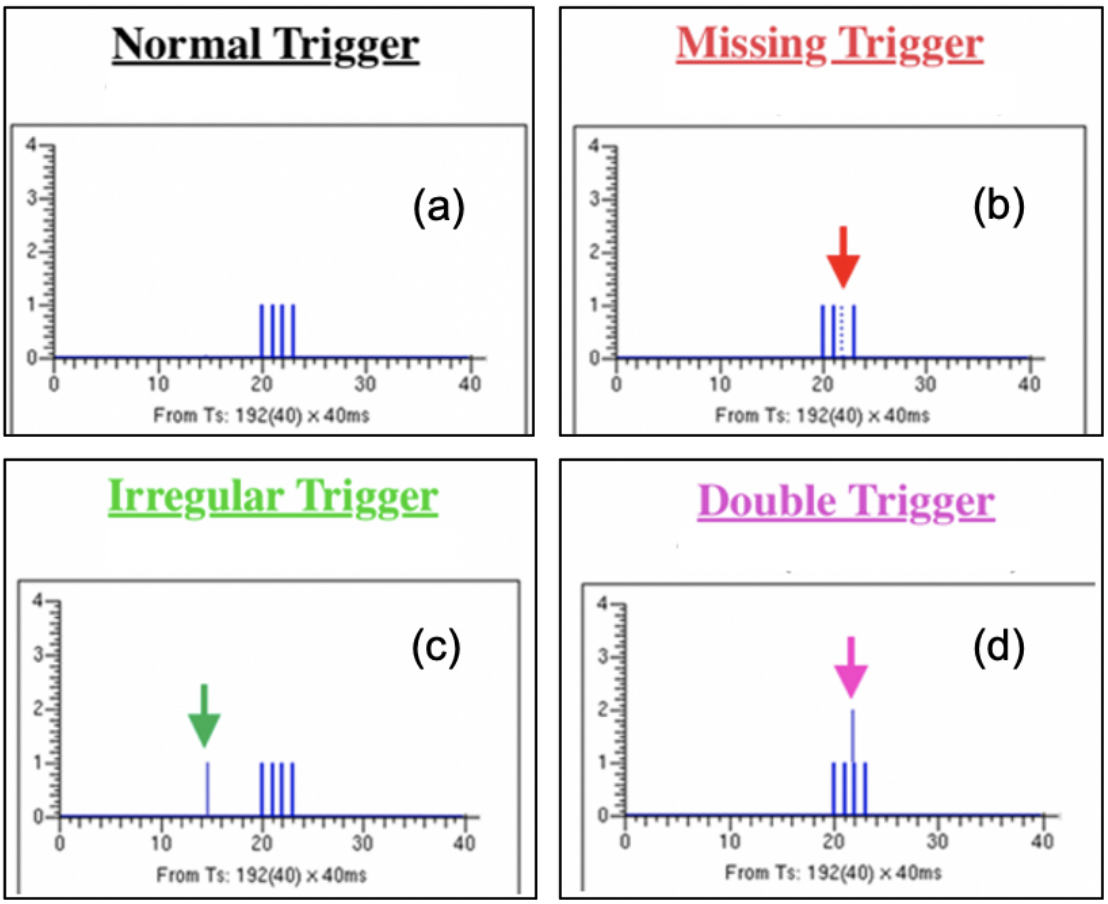

FIGURE 6.2: (a) Normal trigger of injection kicker signal, (b) a missing trigger event, (c) an irregular trigger event, and (d) a double trigger event.

- Fig. 6.2 (c) shows an irregular trigger event, which indicates that an additional trigger is overlapped into the original signal. This event may be caused by external noise.

- Fig. 6.2 (d) shows a double trigger event. This shows that one trigger is counted twice, which may be caused by poor termination.

The trigger-failure events above are undesirable for an accelerator operation and are called "unexpected trigger-failure events."

6.3 Development of Prototype Read-Back System

A prototype read-back system for the injection kicker signal and the detection routine are explained. The routine was developed to detect the above unexpected trigger-failure

events.

6.3.1 Hardware Setting

To develop the prototype system, the same setup was used, which is shown in Fig. 5.9 in Chapter 5. A dummy injection kicker signal was used during development and test. The whole test bench is shown in Fig. 6.3.

FIGURE 6.3: The test bench of prototype read-back system with a dummy signal. NIM modules are used to provide a "Trig-in" signal to the TS module.

6.3.2 Software Development

6.3.2.1 Software Logic

To detect three possible unexpected trigger-failure events, the software logic was developed as shown in Fig. 6.4.

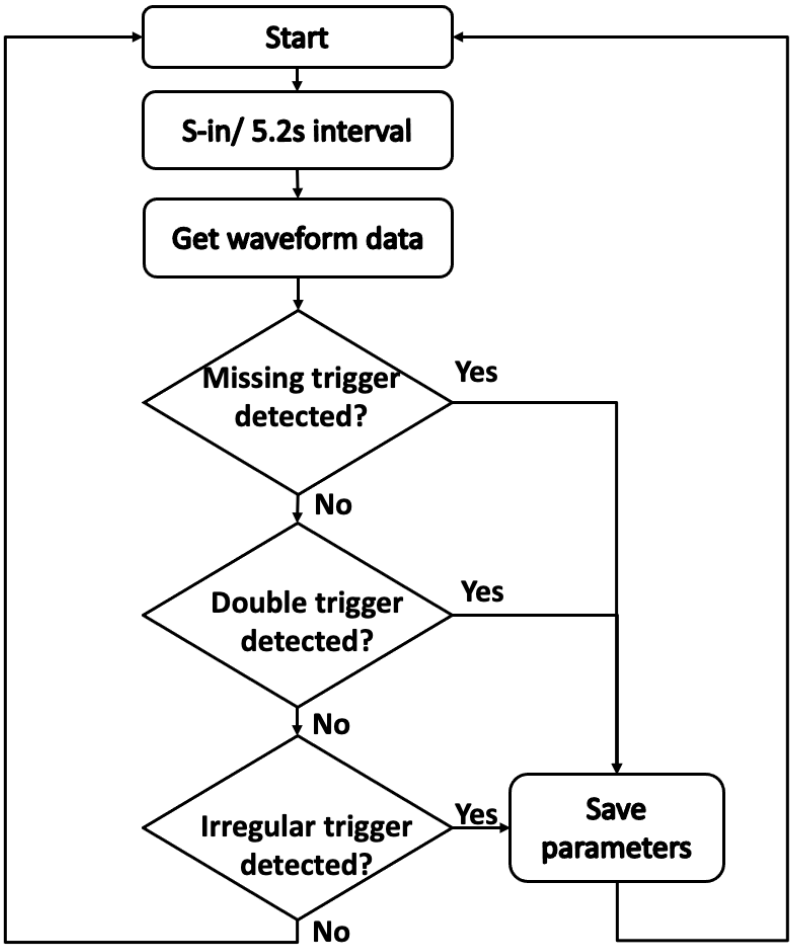

FIGURE 6.4: Software logic of unexpected trigger-failure detection.

In run-time, the TS module counts input pulses and stores them in a memory buffer. Every time the "S" signal comes in, the software extracts the stored data as a waveform-type variable (an integer array, 16 bit $\times$ 192 cells with MR-type), which corresponds to the data during the last machine cycle. Then, the software judges if there have unexpected trigger-failure events. If one or more unexpected trigger-failure events occurred, the failure event data and its timestamp would be saved simultaneously.

6.3.2.2 EPICS Database Development

According to the software logic, the EPICS database was developed to detect non-zero or not-one values in the memory buffer and identify the three types of unexpected trigger-failure events.

The "subArray," "compress," "calcout," "waveform," "timestamp," and other EPICS records are used for EPICS database development [58].

6.3.2.3 GUI Development

The appearance or disappearance of four injection triggers and the identified failure type are indicated in a GUI. The development of GUI is based on an EPICS tool, EDM. The developed GUI is shown in Fig. 6.5.

FIGURE 6.5: The developed GUI of prototype system with the injection kicker signal.

1. The first part, highlighted with green, shows the live data, such as a current J-PARC run number, a shot number, a timestamp, and an observed pattern of triggers.

2. The second part, red, will show the parameters of detected unexpected trigger-failure events, such as the timestamp, the run number, the shot number, the identified type

of unexpected trigger-failure, and appearance (or disappearance) of four injection triggers.

3. The third part, blue, will show the saved parameters when the unexpected trigger-failure occurs, such as the detected pattern of triggers, and the DCCT waveform (beam-current of MR during the machine cycle).

6.4 Test of the Prototype System

First, a dummy signal is used to simulate three types of unexpected trigger-failure events. As shown in Fig. 6.6, the system detected all of them successfully.

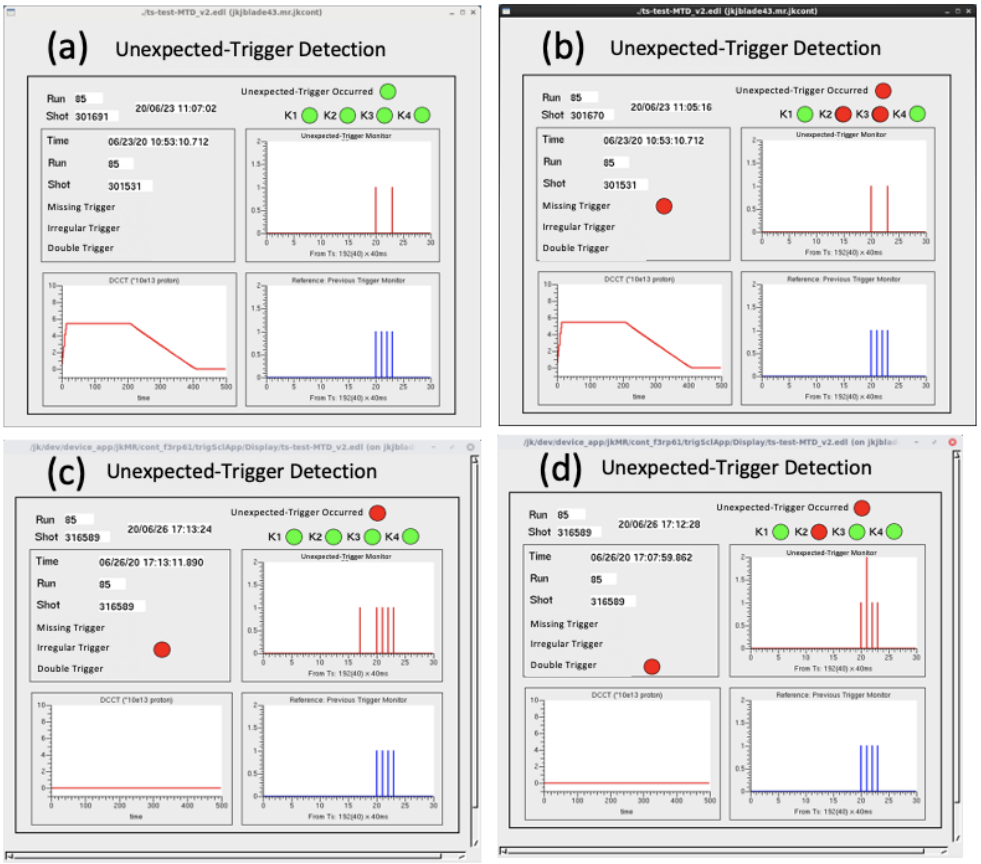

FIGURE 6.6: The screenshots of the unexpected trigger-failure detection system using a dummy signal. (a) The normal system with remained information of the last event. (b) A missing trigger event. (c) An irregular trigger event. (d) A double trigger event.

Second, the system was tested with the real injection kicker signal during J-PARC beam operation for around 40 hours in June 2020. The result showed no unexpected trigger-failure event detected in Fig. 6.7.

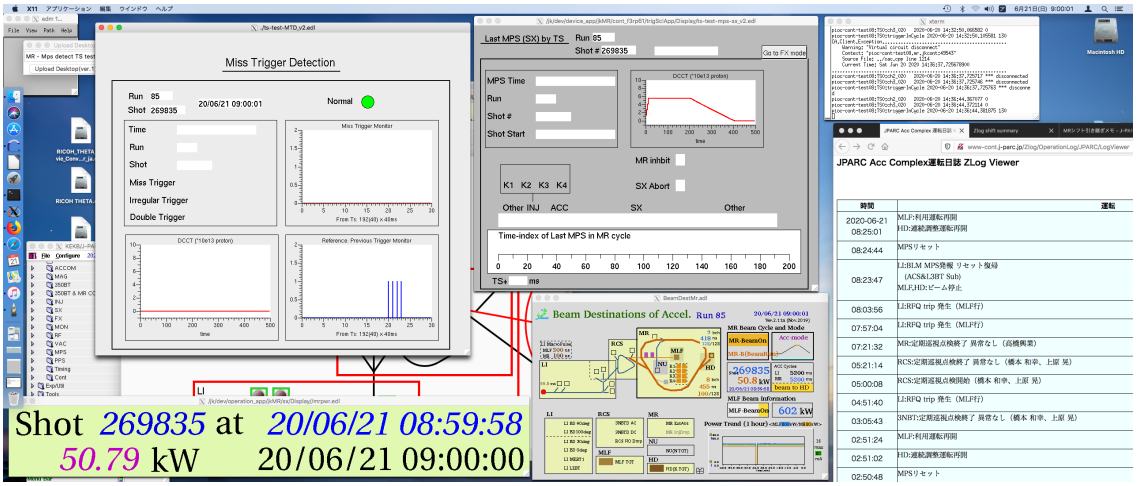

FIGURE 6.7: The measurement of unexpected trigger-failure detection system within around 40 hours.

6.5 Summary

The prototype of unexpected trigger-failure detection system has been developed and demonstrated successfully. The result proved that the TS module has capability of developing a customized read-back system for detecting unexpected trigger-failure events.

Based on the study of the prototype system, other timing signals can also be measured, such as delayed-trigger signals for accelerator devices and power supplies. In addition, customized read-back systems can be developed depending on different cases. Development of customized read-back systems is described in Chapter 7, as the countermeasures against the past trigger-failure events mentioned in Chapter 4.

Besides, since the TS module measured other signal (LLRF signal) in 2018 and succeeded in visualizing the signal, the read-back system for other signals can also be developed for extending the system functionality in various fields.

Finally, during the development of prototype system in 2020, some insufficient functions of the TS module have been reviewed. The firmware of the MR-type TS module has been

updated during 2020 and 2021, and used in the various implementations in Chapter 6 and Chapter 7. The detail of the firmware updates is given in Appendix A.

Chapter 7

Implementations of Read-Back Systems

7.1 Overview

The capability of the triggered scaler (TS) module for developing a customized read-back system has been evaluated in Chapter 6 but tested only with a dummy signal. This Chapter introduces implementations of read-back systems for actual beam operation. There are two main directions of the implementation: one is to monitor timing signals for accelerator operation and accelerator devices, another one is to monitor other signals that are not timing-related but important for accelerator operation.

In the first line of implementation, three timing read-back systems were developed, including a read-back system for the 25 Hz signal from RCS, and two customized systems for two delayed trigger signals. The read-back system of 25 Hz trigger signal was developed using the same hardware as the prototype system in actual operation. It was implemented for the real injection kicker signal. Two read-back systems of two delayed trigger signals are a read-back system of pulsed bending magnet trigger and a read-back system of optical-gate signal. These three read-back systems are countermeasures against past trigger-failure events (Chapter 4).

Besides the above three read-back systems for timing signals, two read-back systems for other signals, an MPS beam abort signal detection system and LLRF pattern monitoring system, were also developed.

7.2 Read-Back System of 25 Hz Trigger Signal from RCS

7.2.1 Background and Motivation

The 25 Hz trigger signal from RCS is used for the data acquisition of fast current transformer (FCT). The position of the FCT is located between RCS and MR, which is shown in Fig. 7.1(a). It counts number of incoming protons to MR, which is essential for MR MPS and PPS (Personnel Safety System, see Chapter 2.4.5). There was a trigger-failure event in 2016, which affected to the MPS (see Chapter 4.2). When an error of the signal occurs (Fig. 7.1(b)), not only MPS, but the FCT diagnostic system of PPS miss operation and may issue a PPS alarm.

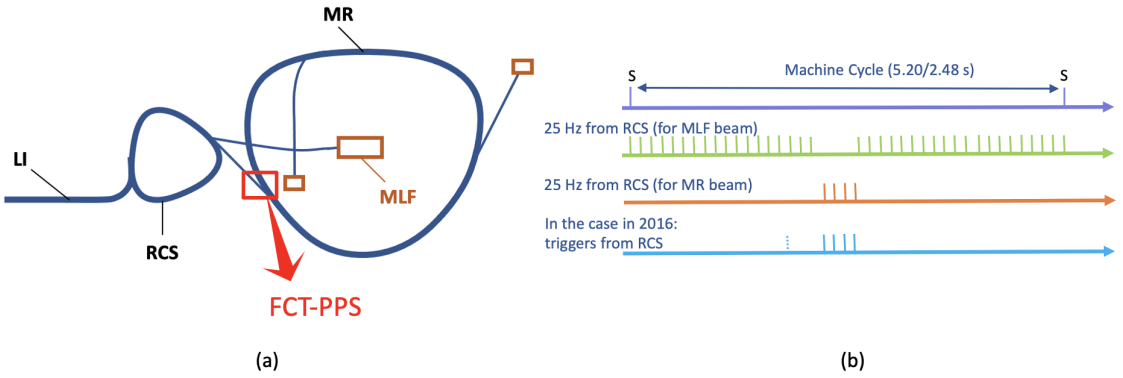

FIGURE 7.1: (a) The position of FCT-PPS for MR. (b) The pattern of 25 Hz trigger signal for MLF, MR, and for the case in 2016 (see Chapter 4.2).

An PPS alarm is very critical, since it forces accelerator devices to the cold start level for safety. Recovery takes time. Therefore, the 25 Hz trigger signal from RCS is essential for the proper operation of J-PARC, and a read-back system of the signal is urgently needed.

7.2.2 Development of the System

The hardware setup is shown in Fig. 7.2.

FIGURE 7.2: The hardware setup of 25 Hz trigger signal read-back system.

The setup includes a CPU module, a triggered scaler module, and a power supply. EPICS and Linux are running on the CPU module. The 25 Hz trigger signal is connected to the second channel of the TS module. This setup is placed at the D3 power supply building in J-PARC MR.

7.2.3 Test of the System

The GUI screenshot in Fig. 7.3 shows the 25 Hz trigger signal from RCS, which is observed by the read-back system. The system realizes the remote monitoring and the visualization of the signal. Thus, it functions as the countermeasure against the failure event in 2016 (see Chapter 4.2).

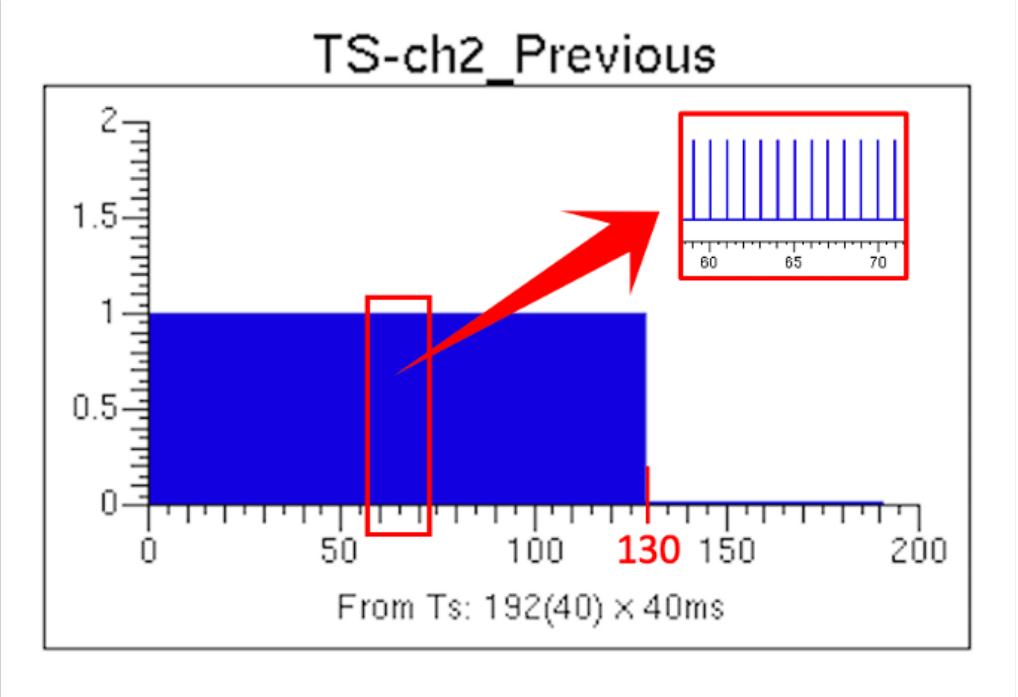

FIGURE 7.3: The observed 25 Hz trigger signal from RCS by the read-back system. The machine cycle was 5.20 s. Hence, the maximum number of cells is 130.

7.3 Read-Back System of Pulsed Bending Magnet Trigger

7.3.1 Background and Motivation

Pulsed Bending Magnet and Timing Signal The pulsed bending magnet is located in the beam transport line from the RCS to MR (350BT) (Fig. 7.4). It is designed for switching the beam to MLF or MR in each machine cycle at J-PARC [59]. Because the MR requires four successive RCS cycles, the pulsed bending magnet maintains its field flat for 120 ms, as shown in Fig. 7.4. The failure to start the pulsed bending magnet will cause the beam to be sent directly to MLF.

The timing signal, a delayed-trigger provided by the J-PARC timing system, is used to trigger the pulsed bending magnet power supply to excite the pulsed bending magnet.

Motivation of Development According to the broken fuse case mentioned in Chapter 4.3, a failure event is serious concern about the beam-switching function between MLF

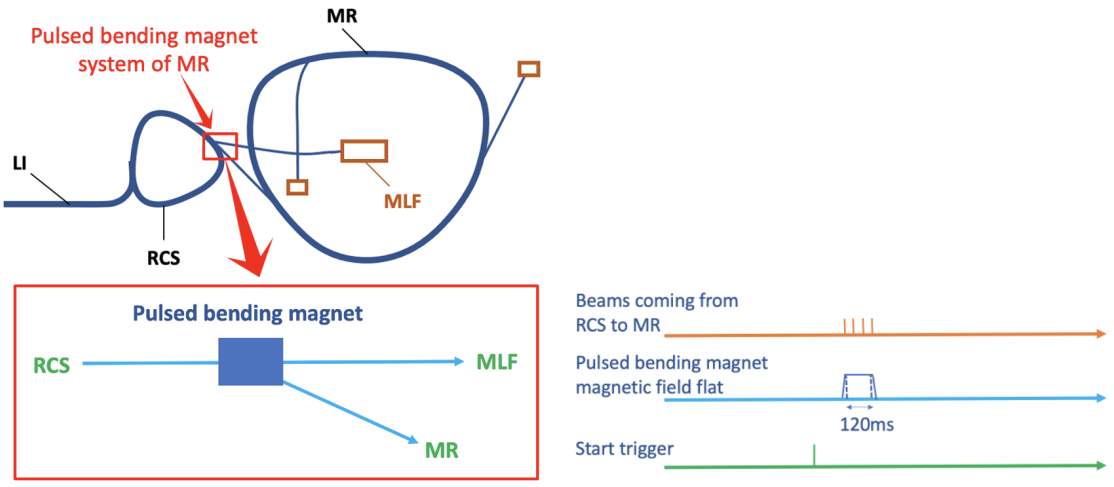

FIGURE 7.4: The location of pulsed bending magnet in J-PARC and the flat shape of the magnet field.

and MR. It is necessary to watch the timing signal for pulsed bending magnet power supply with a timing read-back system, to reduce the time to find the faulty module and identify the event type of the signal.

7.3.2 Development of the System

7.3.2.1 Hardware Setup

The hardware setup is shown in Fig. 7.5.

The trigger-failure event that occurred in 2018 was caused by a trigger fanout module (RPN-1060, see also in Chapter 4.3 and Fig. 4.3). As a countermeasure against that event, the system reads back a trigger signal from the same trigger fanout module. The "S" and the "trigger" signals are transferred with the same O/E module (RPN-870) as for the pulsed bending magnet power supply. If there is any problem with these modules, the system can identify it immediately.

The EPICS IOC with a TS module is implemented in the frame of pulsed bending magnet power supply (see also Fig. 7.9). Two media converters are used to make a network connection.

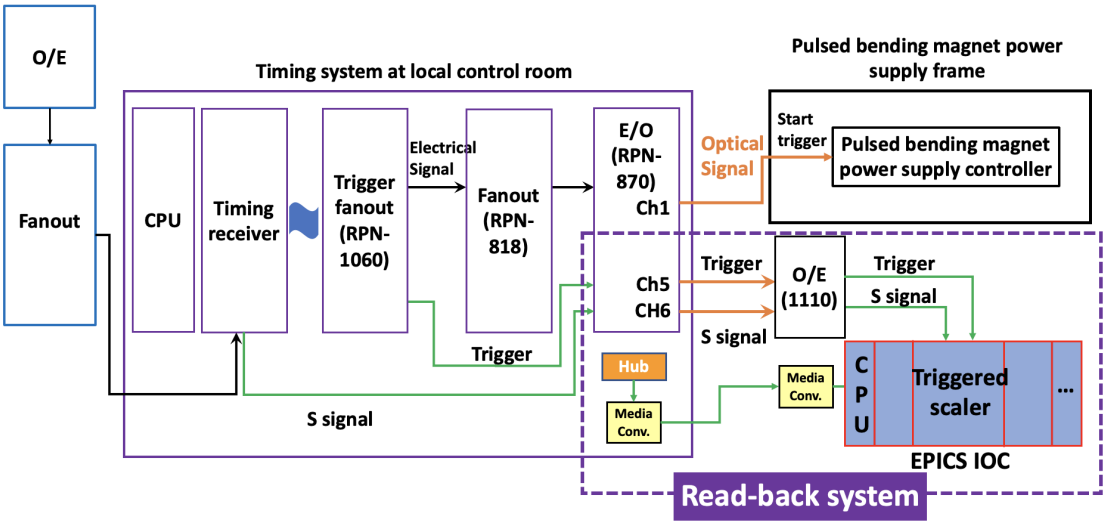

FIGURE 7.5: The hardware setup of pulsed bending magnet trigger read-back system.

7.3.2.2 Software Development

Fig. 7.6 shows the GUI screenshot of the system, which was developed using an EPICS tool, EDM. The observed trigger signal is measured by a TS module and stored in a memory buffer. The signal pattern in one machine cycle is obtained as an EPICS waveform-type data, and shown with a timestamp as in the left part of Fig. 7.6.

To realize the monitoring functionality of the system, the software logic was developed using the EPICS database. The software logic of system revolves around the status of three LEDs: "LED_TrigOK," "LED_TrigFault," and "LED_TrigStop," which is shown in Fig. 7.7 and Fig. 7.8.

The first part of software logic is shown in Fig. 7.7. At the beginning, it checks the beam destination. When MR is not the beam destination (i.e., maintenance day), it is not necessary to check the pulsed bending magnet trigger. When MR is the beam destination, the "LED_TrigOK" light turns on, and then the second software logic is processed.

As shown in Fig. 7.8, the second software logic checks the waveform data of the pulsed bending magnet trigger every machine cycle. If there is an unexpected trigger-failure event, the LED for the corresponding event type turns on, and then the "LED_TrigFault" light comes on. As the "LED_TrigFault" lights up, some useful information is latched, such as the fault waveform data with timestamp, the judged type of the fault, and some J-PARC accelerator parameters at the time. During the "LED_TrigFault" is on, the

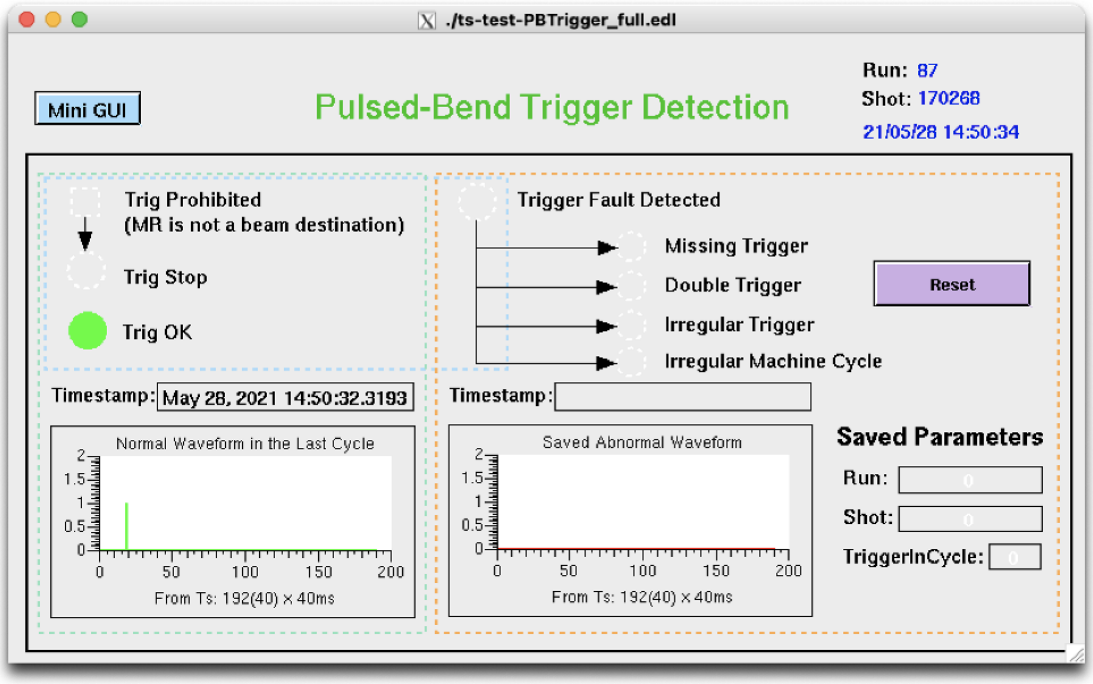

FIGURE 7.6: The GUI screenshot of pulsed bending magnet trigger read-back system. A green LED "Trig OK" means that the trigger check process is running and no trigger fault detected.

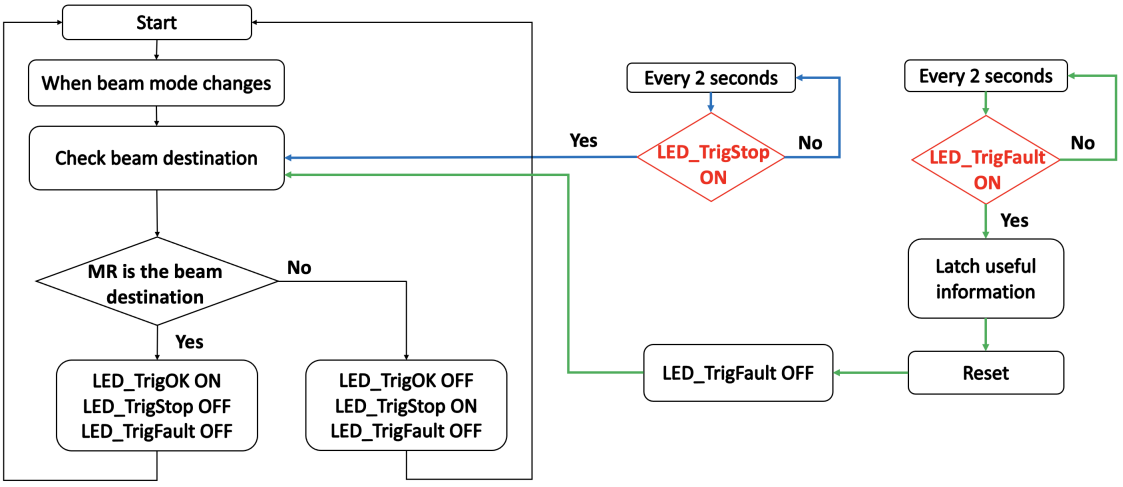

FIGURE 7.7: The first part of software logic for pulsed bending magnet trigger read-back system.

checking process is stopped until the "Reset" button is clicked, as shown in the right part of Fig. 7.7.

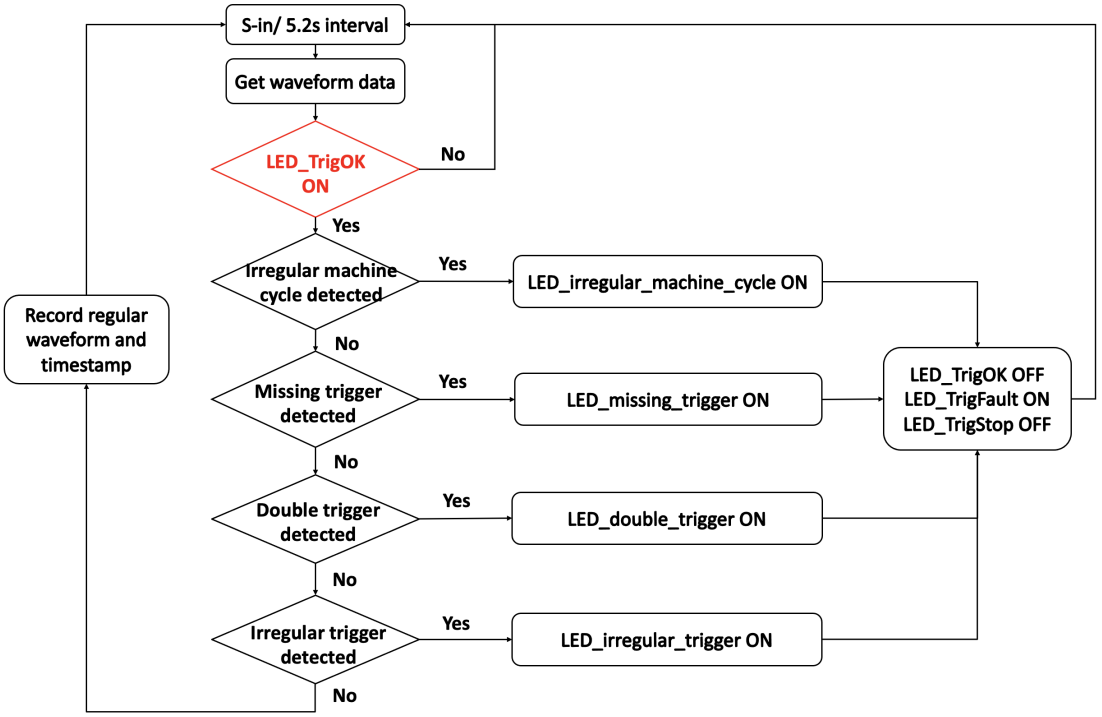

FIGURE 7.8: The second part of software logic for pulsed bending magnet trigger read-back system.

7.3.3 Test of the System

As shown in Fig. 7.9, the real implementation of the read-back system is inside the frame of the pulsed bending magnet power supply (see also Fig. 7.5).

The system started operation on May 10, 2021, and ran for around two months. No unexpected pulsed bending magnet trigger-failure event was observed. To verify that the system works as expected, it was tested using a dummy signal before and after the operation. The GUI screenshot in Fig. 7.10 indicate that the system detected an irregular trigger event successfully.

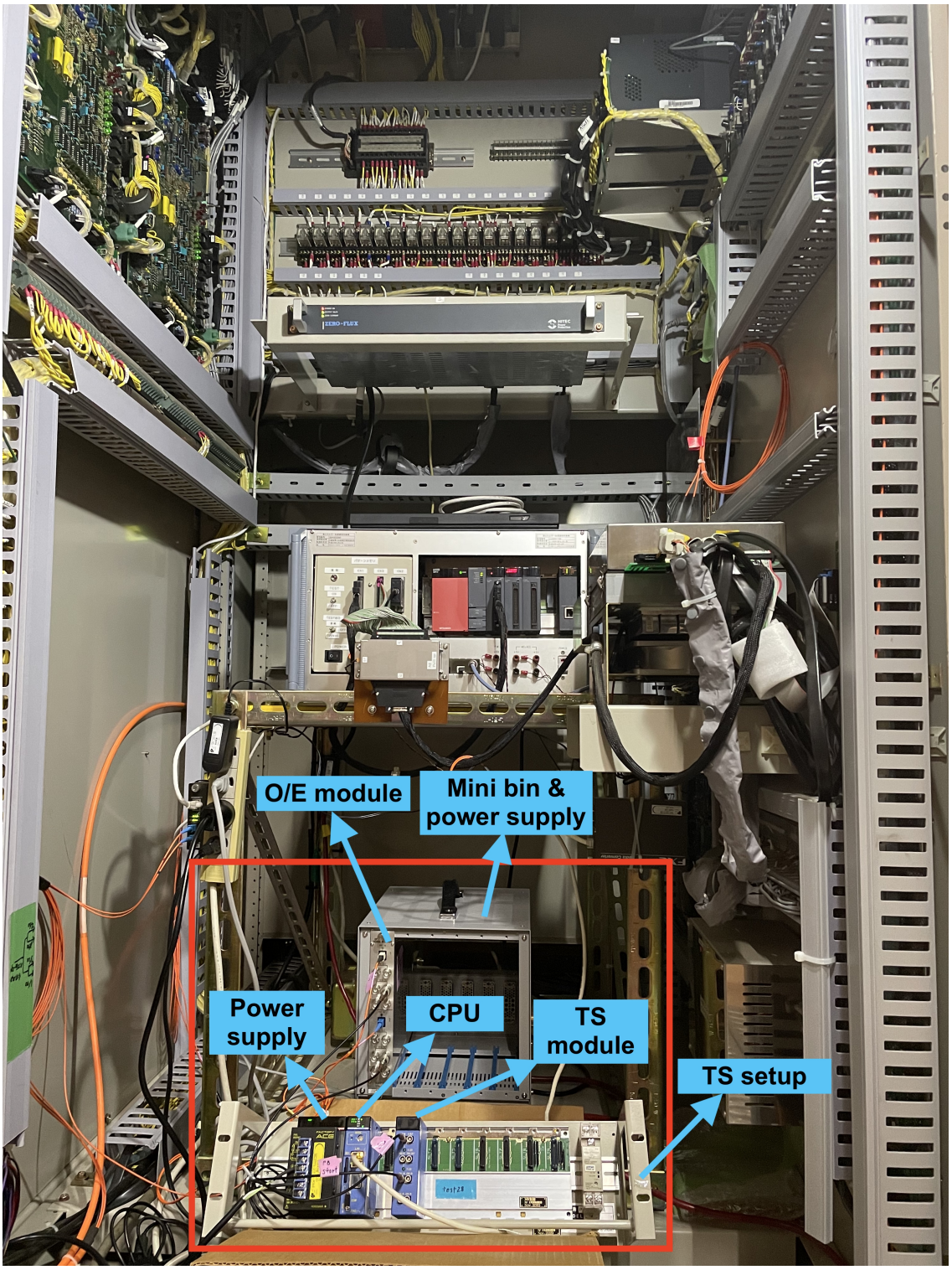

FIGURE 7.9: The real implementation of pulsed bending magnet trigger read-back system inside the frame of the pulsed bending magnet power supply.

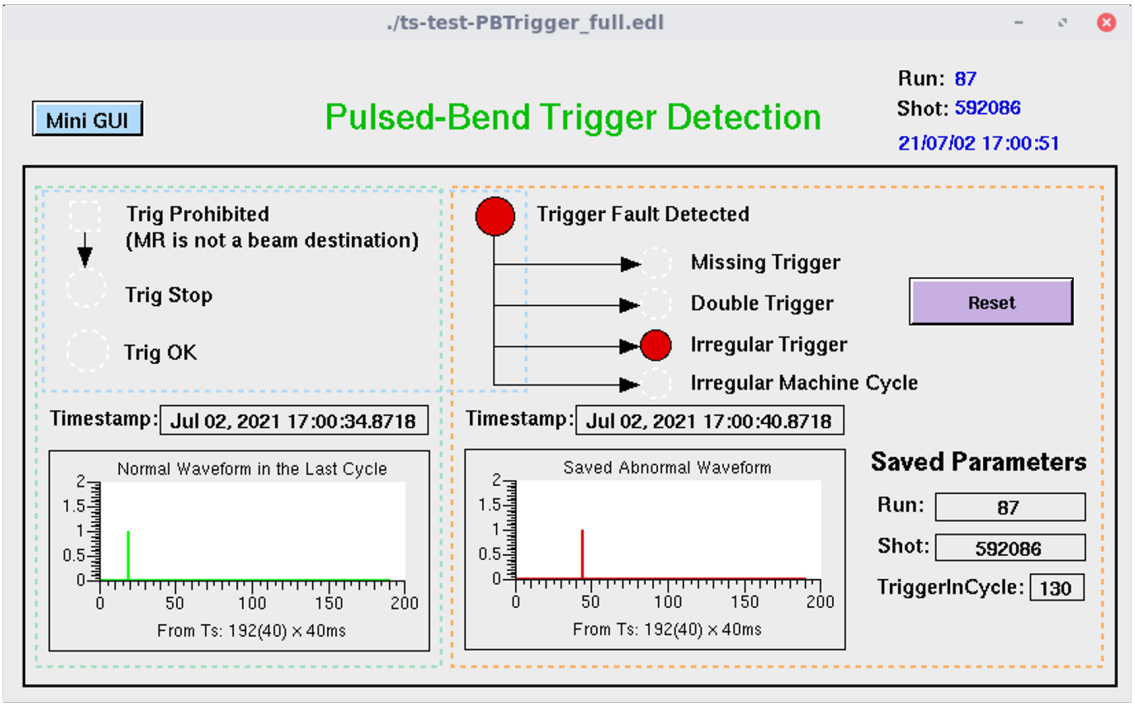

FIGURE 7.10: The GUI screenshot of pulsed bending magnet trigger read-back system with simulated irregular trigger event.

7.4 Read-Back System of Optical-Gate Signal

7.4.1 Background and Motivation

Regarding the steering magnet missing trigger event in 2015-2016, the problem has been solved by adding ferrite cores to metal cables as described in Chapter 4.4. Therefore, it is not urgent to monitor it, but it will be considered in the future.

As described in Chapter 4.5, in the summer of 2020, some fuses for the bending magnet trim-coil short system were found broken. One possible reason is that a shifted gate signal or a missing stop gate signal occurred during beam operation in June 2020. To confirm the source of broken fuses, a read-back system to supervise the optical-gate signal was developed.

7.4.2 Development of the System

7.4.2.1 Hardware Setup

The hardware setup of the system is shown in Fig. 7.11. The optical-gate signal is converted to an electrical signal by an O/E module (RPN-1110). Since the TS measures pulse signals, the electrical-gate signal is converted to a start signal and a stop signal by electronic, and observed by the TS module. The trigger fanout module (RPN-818T) is used to detect rising edges. A digitizer module added to EPICS IOC is used to detect faulty electrical-gate signal.

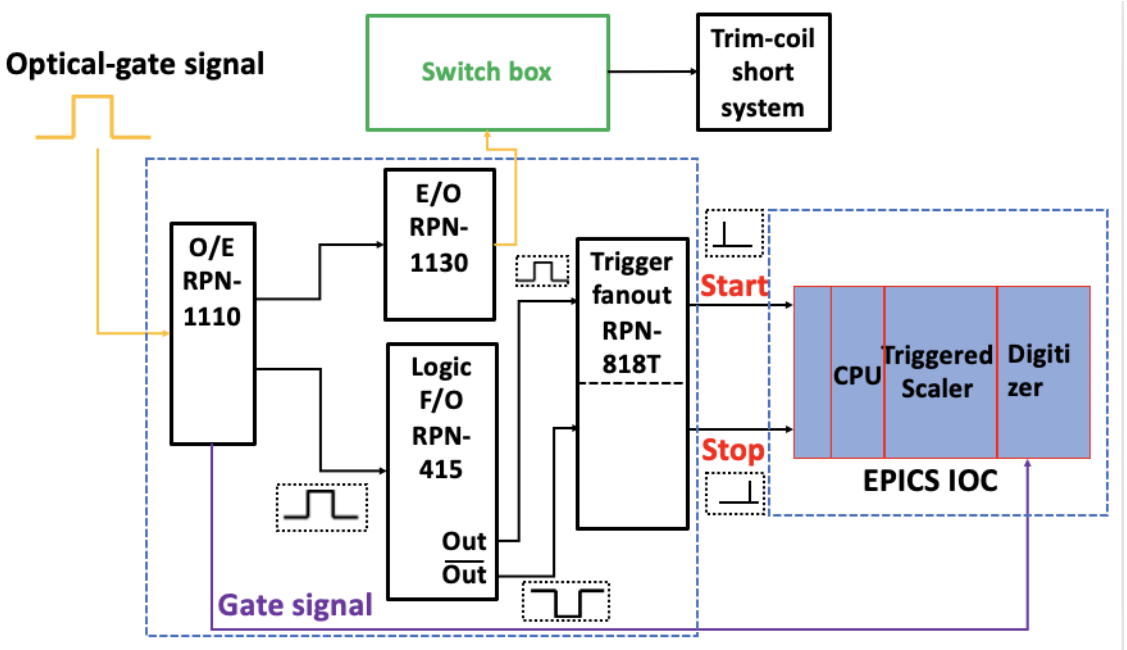

FIGURE 7.11: The hardware setup of the optical-gate signal read-back system.

7.4.2.2 Software Development

The identification routine of gate signal is shown in Fig. 7.12.

The gate start and gate stop signals are read by the TS module and stored in the memory buffer. Then, the identification routine judges if there is a shifted gate signal or a missing stop signal during the last machine cycle. If an unexpected gate signal is observed, the timestamp and the data of the gate signal are latched for reference. If no trigger-failure

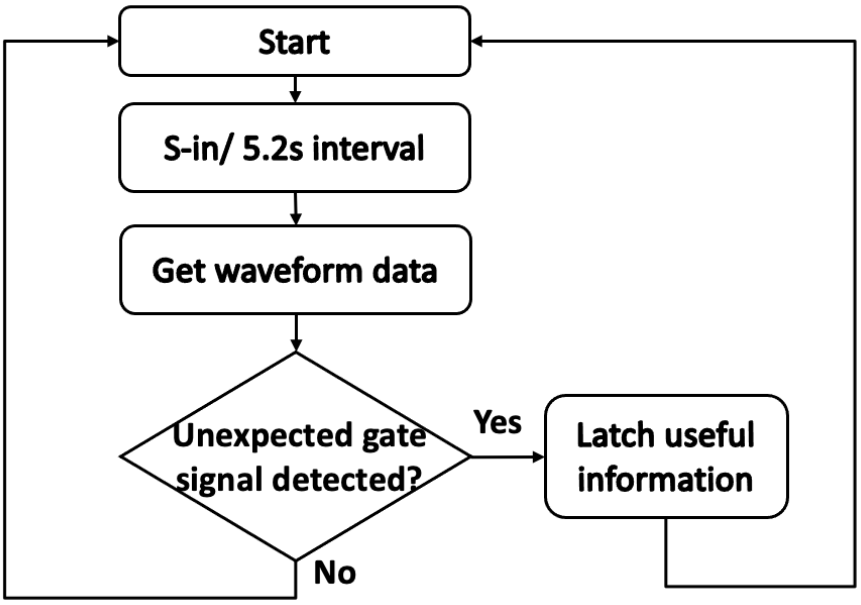

FIGURE 7.12: The identification routine of the optical-gate signal read-back system.

event occurs, the identification routine will return back the start and check the newly arrived data.

Based on the software logic, the EPICS database was developed using "subArray," "compress," "waveform," and other EPICS records [58].

7.4.3 Test of the System

As shown in Fig. 7.13, the real implementation of the read-back system is placed at the D2 building of J-PARC MR (see also Fig. 7.11). It has been operated during the J-PARC beam operation in February 2021 (from February 8 to February 28). No missing stop or shifted optical-gate signal was observed. This fact implies that the cause of broken fuses in June 2020 is not the faulty optical-gate signal. However, longer observation is preferable to come to the solid conclusion.

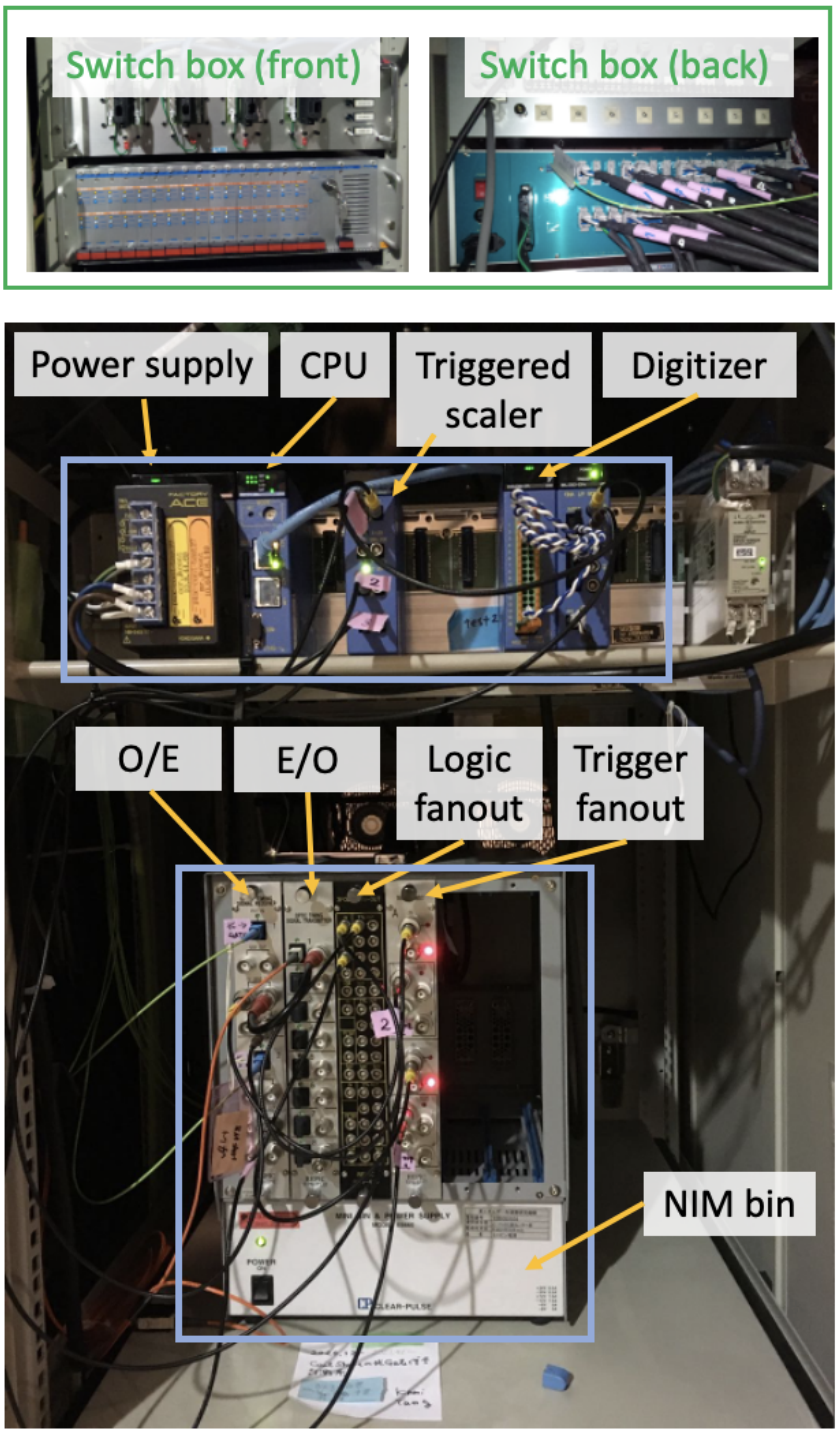

FIGURE 7.13: The real implementation of optical-gate signal read-back system.

Fig. 7.14 shows the GUI screenshot. To confirm that the read-back system has worked well, the system was tested with a simulated missing stop signal in July 2021. The upper side of the GUI shows the data in real-time: the normal start and stop signals by the TS module, and the normal electrical gate signal by the digitizer. The lower side shows the latched data when an event occurred: the missing stop signal, and the abnormal electrical gate signal. In addition, an indicator turns to red to show that an abnormal stop signal is detected.

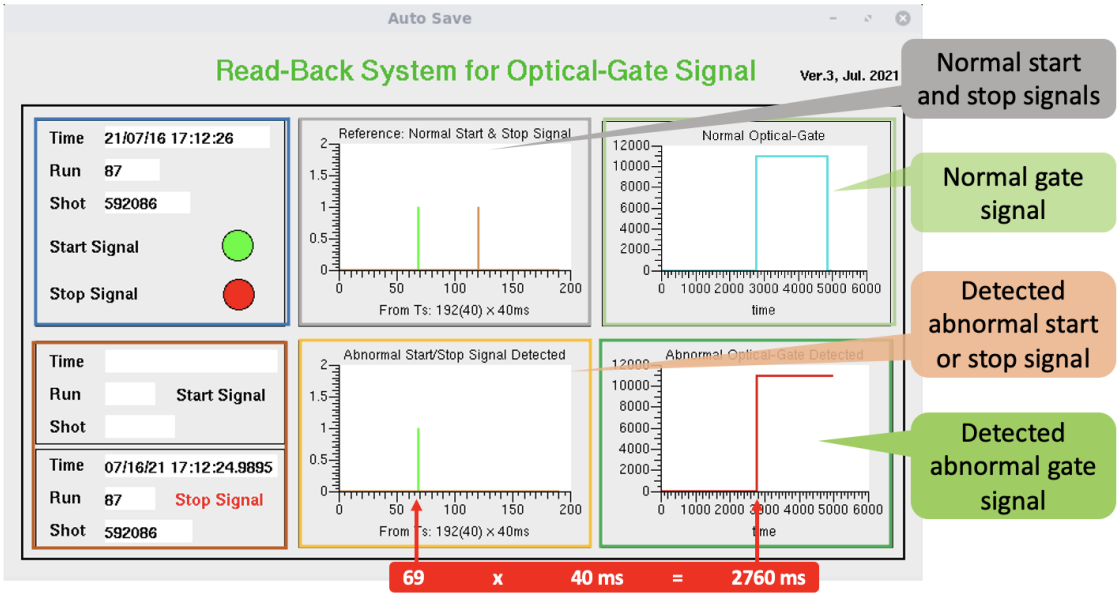

FIGURE 7.14: The GUI screenshot of optical-gate signal read-back system with a simulated missing stop event.

7.5 Read-back System of Other Signals

The above implementations of read-back systems could read back the timing-related signals to solve past trigger-failure events. In addition, two other signals were also supervised by customized read-back systems.

7.5.1 MPS Beam Abort Signal Detection System

7.5.1.1 Background and Motivation

MPS at J-PARC MR When one of MR device, such as a magnet power supply or beam loss monitor, detects a fault, the MPS of J-PARC MR generates two signals. One is an "All-Stop" signal sent to the upstream LI to stop the ion source. Another one is an "Abort" signal sent to the MR extraction kicker to abandon beams to the abort dump [32].

Motivation of Development In the J-PARC MR, timestamps of MPS events are recorded by an archive system. In order to analyze MPS events, the machine phase (INJ/ACC/SX phases are explained in Chapter 2.3) in which MPS occurs needs to be known. However, deriving this from the recorded timestamp is a complicated manual task. To easily visualize which phases of accelerator an MR MPS-abort signal generated, an MPS beam abort signal detection system was developed.

7.5.1.2 System Development

Hardware Setup The hardware setup of the system is the same as the read-back system of 25 Hz trigger signal in Fig. 7.2, only a different input channel (Channel 4) is used.

Software Development The software logic was designed as shown in Fig. 7.15.

During stable beam operation, the MPS abort signal should not appear. When an MPS event occurs, a "1" value appears in the memory buffer of TS. The EPICS database was designed to catch a "1" value in the memory buffer during the last machine cycle. When a "1" value is detected, it means an MPS event occurs, and useful information is latched. A state notation language (SNL) [60] program was developed to count the time-index, the count"1" position in a memory buffer.

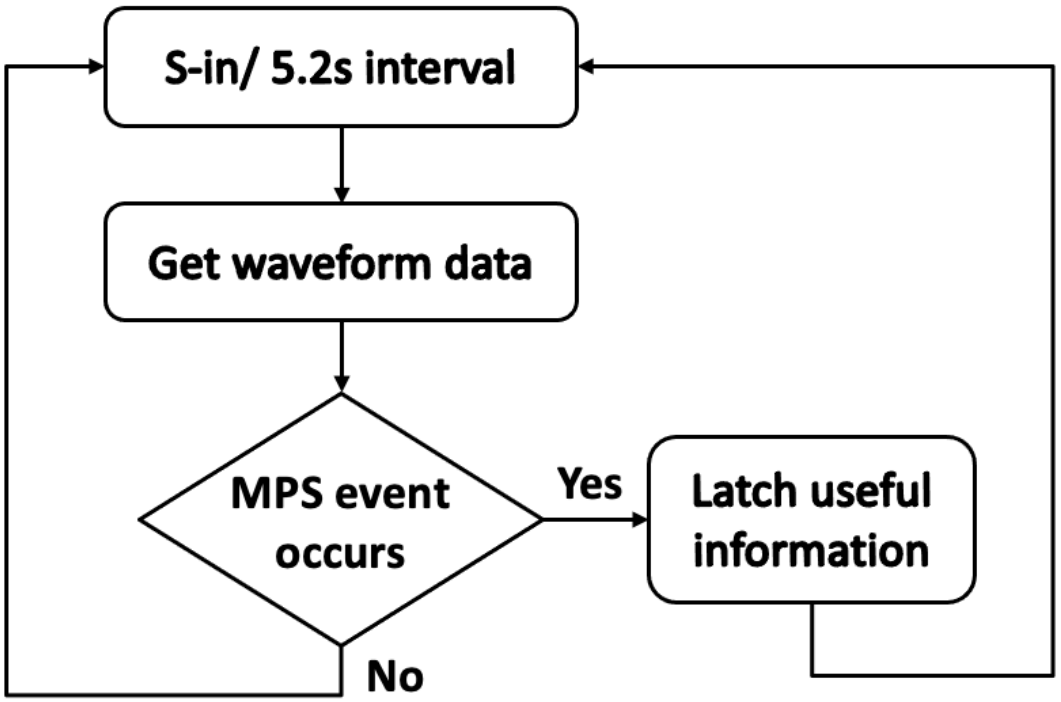

FIGURE 7.15: The software logic of the MPS beam abort signal detection system.

7.5.1.3 Test of the System

The system has been available since May 2021. It detected and visualized many MPS events during J-PARC beam operation. Fig. 7.16 shows an example of an MPS event that occurred on June 4, 2021.

1. The first part of this GUI screenshot shows the live data of J-PARC operation parameters and timestamp.
2. The second part latches the timestamps, J-PARC operation parameters, and the beam current of J-PARC MR at the event.
3. The third part visualized in which machine phase the MPS occurred.
4. The fourth part shows the time-index measured by the TS module. It shows the position of 40 ms time-bin in the MR cycle of the last MPS.

The system visualized in which machine phase the MPS occurred successfully. It helps operators to understand the MPS events easier than ever.

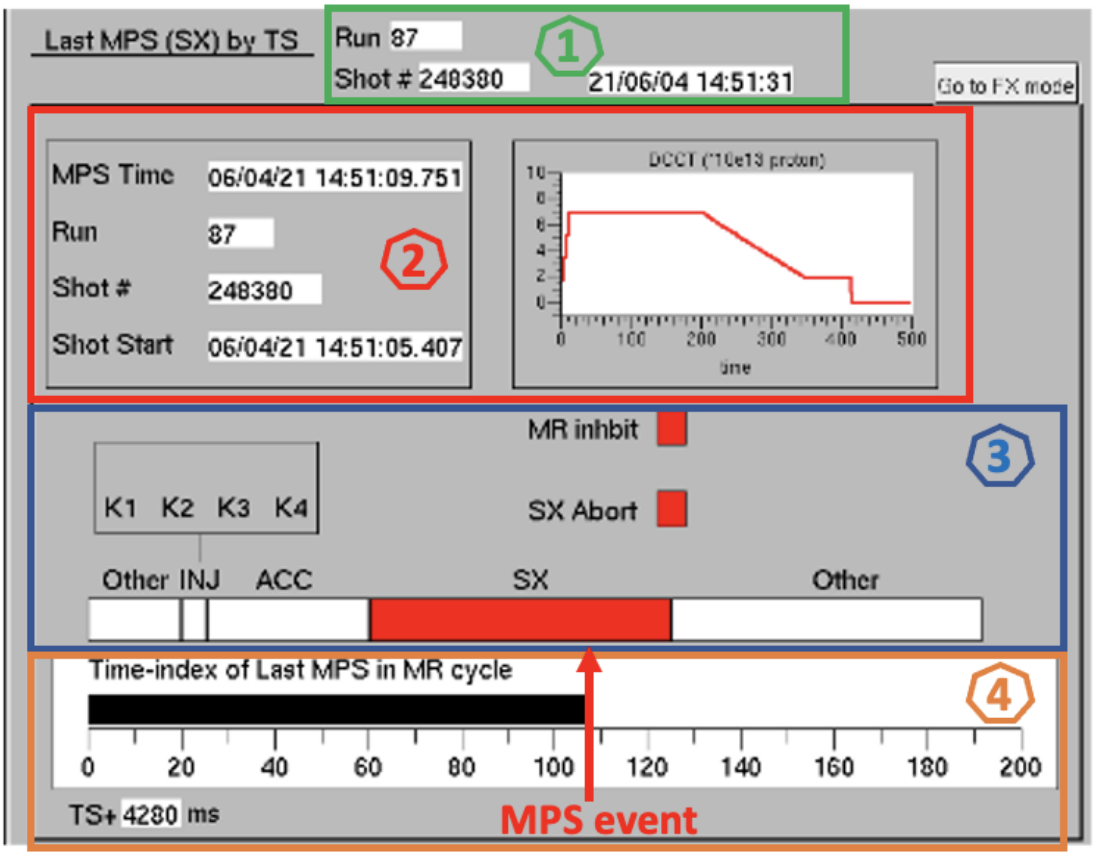

FIGURE 7.16: GUI screenshot of MPS beam abort signal detection system.

7.5.2 LLRF Pattern Monitoring System

An LLRF signal was measured as an initial test of a TS module in 2018 (see Chapter 5.4.3.2). As an upgraded system for real operation, an LLRF pattern monitoring system was developed for monitoring and visualizing the LLRF signal pattern. Fig. 7.17 shows the LLRF patterns in 30 GeV and 8 GeV.

In addition, the MR energy can be deduced from the observed LLRF pattern (see Fig. 5.11). Fig. 7.18 shows the history of the MR energy in two weeks retrieved from an achiever system. LLRF settings correspond to MR energies perfectly.

The system has been in operation since May 2021. It helps safe operation.

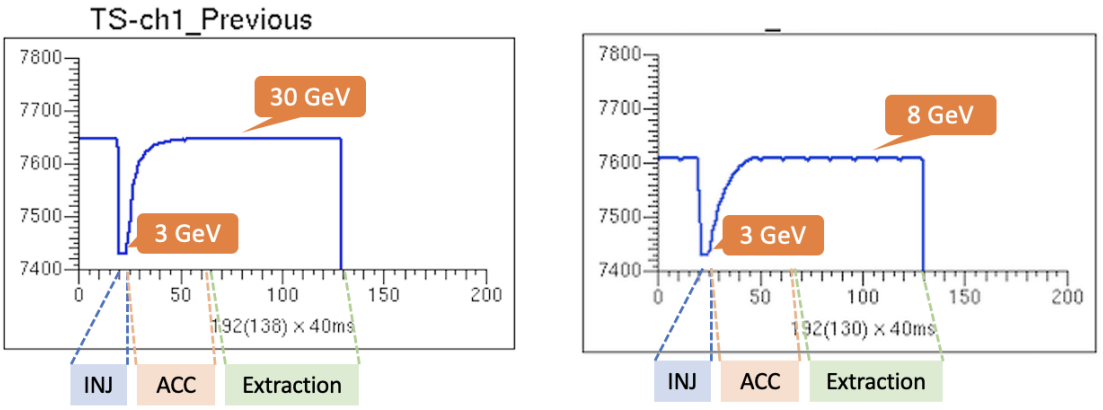

FIGURE 7.17: LLRF patterns in 30 GeV and 8 GeV energy.

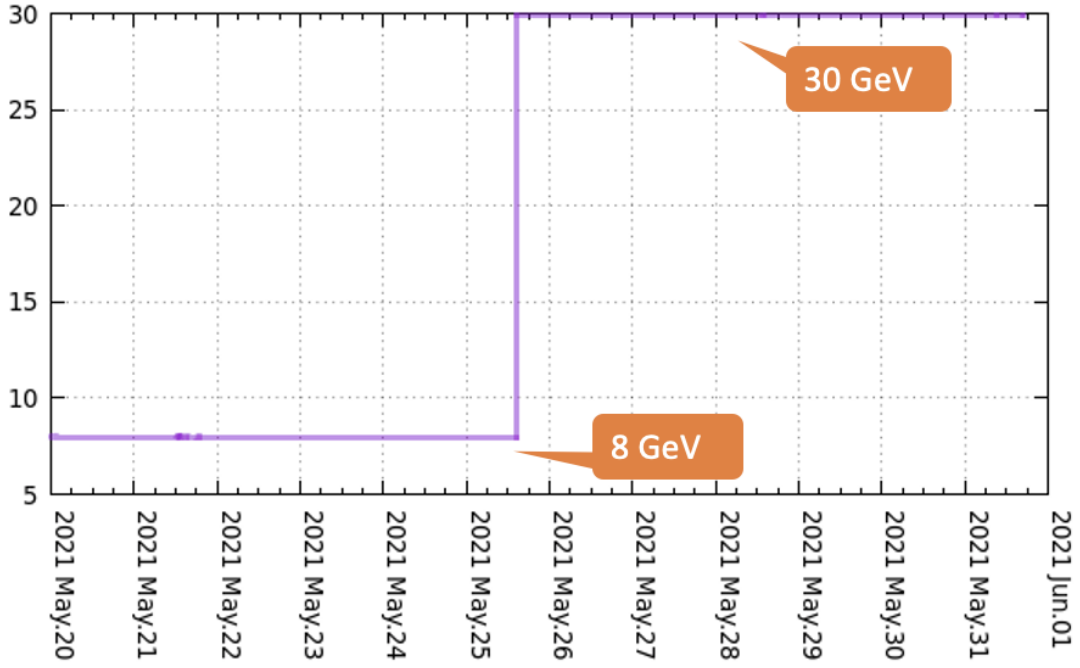

FIGURE 7.18: History of MR energy in two weeks by an achiever system.

7.6 Summary

Customized read-back systems have been developed for different signals. Table 7.1 shows the summary of the customized systems.

TABLE 7.1: Summary for five implemented read-back systems.

No.	Customized system	Achievement	Status (at J-PARC MR)
1	Read-back system of 25 Hz trigger signal from RCS	a) Remote monitoring	In use (Since 2021.05)
2	Read-back system of pulsed bending magnet trigger	a) + b) Develop identification routine for unexpected triggers	In use (2021.05-2021.06)
3	Read-back system of optical-gate signal (two delayed-triggers)	a) + b) + c) Add digitizer to monitor the gate signal	Operated for one month (2021.02)
4	MPS beam abort signal detection system	a) + d) Visualize which machine phase the MPS occurred	In use (Since 2021.05)
5	LLRF pattern monitoring system	a) + e) Verify J-PARC MR energy settings	In use (Since 2021.05)

The (a) function, remote monitoring function, has been achieved for all systems. The (b) function, identification routine of unexpected trigger-failure events, for the second and the third cases have been developed. In addition, a digitizer was added to the third system to monitor gate signal directly. These three customized systems have been demonstrated as countermeasures against past trigger-failure events. If the same events occur again, the systems can detect them immediately.

The fourth and fifth read-back systems were also developed for other signals. They have been in operation since May 2021. These additional systems provide helpful information for accelerator operation, which assists the user operation safer.

Part IV

Future Plans and Conclusion

Chapter 8

Future Plans

8.1 Overview

This Chapter aims to discuss future plans. Although the read-back systems were successfully developed and put into actual operation, many items are still to be done. Plans to survey more signals in J-PARC MR are given. In addition, an idea to implement a read-back system with the triggered scaler module (TS) module at other facilities is discussed.

8.2 Future Plans at J-PARC

8.2.1 Improved Read-Back System for Pulsed Bending Magnet Trigger

As shown in Chapter 4, the aging of timing modules has been a potential source of unexpected failures. To proceed scheduled replacement of old modules with new ones, a next-generation timing system has been developed (see details in Chapter 3.2.1.1).

The new receiver for MR is designed as a PLC module. The first receiver module is planned to be used for the improved read-back system for the pulsed bending magnet

power supply. Fig. 8.1 shows the current read-back system (upper) and the improved read-back system (lower). Both a receiver and TS modules are mounted in the same PLC-based EPICS IOC. A digitizer in the same IOC supervises the output of the power supply. As is the current system, the IOC will be located in the frame of the power supply. The improved system will have no O/E and E/O modules, which reduces the failure rate drastically. The enhanced system will be implemented in early 2022.

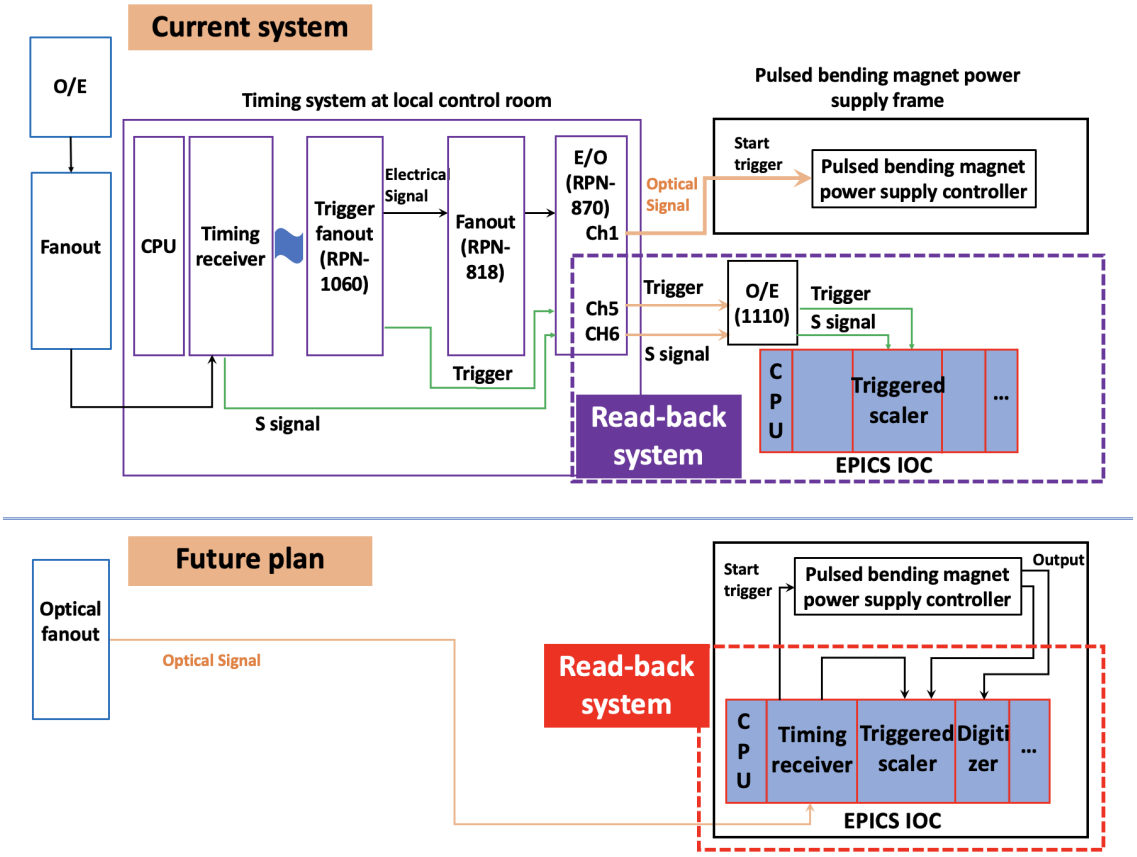

FIGURE 8.1: Comparison of current and improved read-back systems for pulsed bending magnet trigger.

8.2.2 Deployment of Read-Back Systems for J-PARC MR

Recently, the power-upgrade program of MR toward 1.3 MW is being promoted [9]. With such a high beam power, a failure of timing signals should be detected immediately, since a failure would cause more severe damage to MR devices than ever. As shown in Chapter 7, three customized read-back systems started to observe some MR timing signals. However,

there are approximately 200 signals at three power supply buildings of J-PARC MR (D1, D2, and D3). To read back all the signals is ideal but not realistic due to cost.

To verify the timing signals are successfully distributed, a read-back "setup" is planned to be installed. The setup corresponds to the "sensor" in Fig. 1.1. Each setup consists of a PLC-based EPICS IOC with 1 or 2 TS modules. Table 8.1 shows the minimum number of setups to cover each of devices per each of three power supply buildings, which supervises 60 of 200 signals. The implementation of the setups will be in the next 2 or 3 years.

TABLE 8.1: Plan of read-back setups for J-PARC MR.

Signal classification	Signal/Device	Location	Number of setup
Basic signal	S in	D1, D2, D3	3
	Trig clock (25 Hz)		
Delayed triggers for safety devices	Pulsed bending magnet	D1	1
Delayed triggers for power supplies	Injection	D1	1
	Fast extraction	D3	1
	Slow extraction	D2	1
	RF	D1, D3	2
	Main magnet	D1, D2, D3	3
Delayed trigger for others	Beam diagnostic	D1, D2, D3	3

8.3 Future Plans at Other Facilities

8.3.1 A Standalone Read-Back System for Other Accelerators

The current read-back setup assumes the use of the computer resources of the J-PARC control system. Thus, it is unavailable elsewhere but on the J-PARC site. However, it is possible to configure the PLC-based IOC to be a standalone system. Considering the benefit of small form-factor, it is easy to bring the system to other accelerator facilities. Fig. 8.2 shows a possible design of a standalone read-back system.

The system requires two signal links from the target accelerator facility: (a) pulse signals to be measured, and (b) a "S" signal (start of the machine cycle). The former is measured by a TS module to check whether unexpected trigger-failure events occurred or not. The latter is needed to start the module. When the facility does not have the "S" (or similar) signal, a clock divider circuit would be used to simulate the signal from 50 Hz/60 Hz. The internal trigger mode of the TS module is to be used. Thus, no external trigger clock

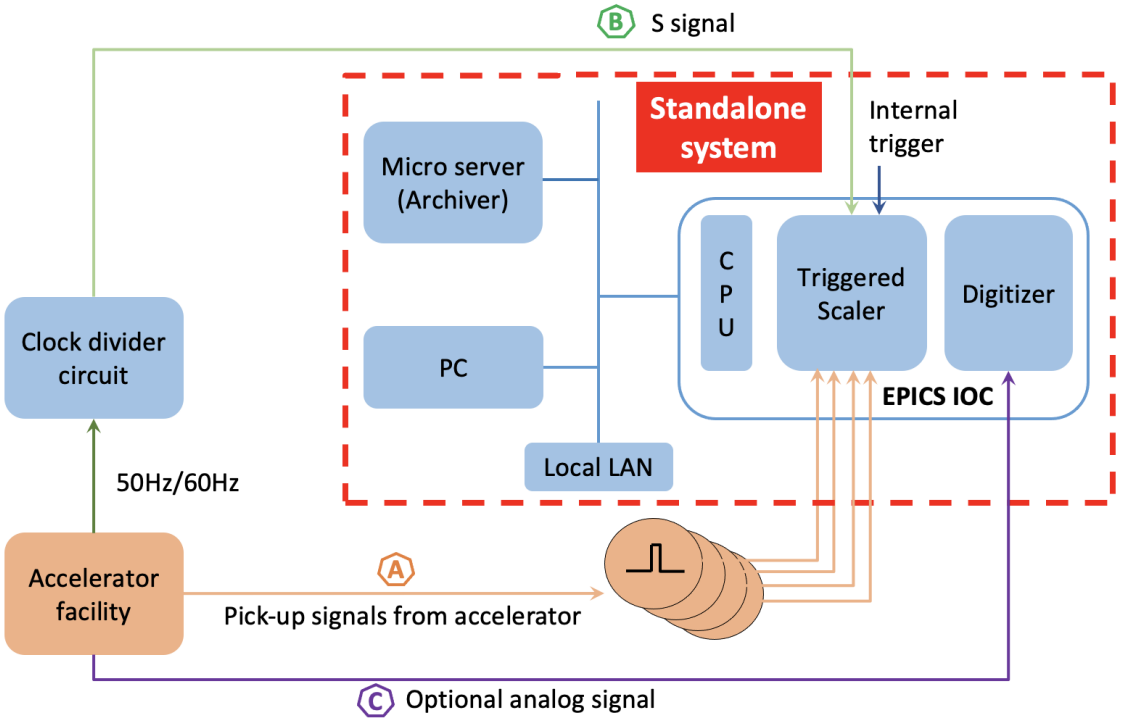

FIGURE 8.2: A standalone read-back system for other accelerators.

is needed. The (c) analog signals are optional to show the source signals when a failure event occurs.

The unexpected trigger-failure detection is customized by updating the EPICS IOC software upon request. In addition, a micro-server [61] is introduced as an archiver. It would be decisive for later analysis of faulty events.

Chapter 9

Conclusion

This dissertation focuses on the timing read-back system.

At first, according to the case study of trigger-failure events in J-PARC MR, a concept of timing read-back system was given. The system reads back delayed-trigger signals at the device side and confirms whether the timing signal arrives or not. A new module, triggered scaler (TS) module, was evaluated as the key device to develop a read-back system.

Then, a prototype read-back system was developed. It was found to detect and identify various types of trigger-failure events successfully. The TS module showed a capability of visualizing the input signal with relationship to the accelerator's machine cycle.

Following the prototype development, five customized read-back systems were developed for different accelerator signals. The EPICS framework and the PLC form-factor of TS enabled high customizing ability. Remote monitoring and trigger-failure detection scheme are realized for three timing signals: a 25 Hz signal, a delayed-trigger signal, and an optical-gate signal. These three read-back systems are demonstrated as countermeasures against the past trigger-failure events. In addition, read-back systems were developed for other signals: an MPS beam abort signal and an LLRF signal. Four of five read-backs have already been used in the J-PARC operation since May 2021.

Finally, two future plans are presented for J-PARC MR. First, a read-back system for the new power supply of the pulsed bending magnet, which is under construction in a company, is given. Second, a realistic scenario is proposed to read back the important timing signals. The realization of these plans should contribute stable operation of J-PARC MR in the future. Moreover, an idea to implement a read-back system with a TS module at other accelerator facilities is discussed. The fruitful results of this dissertation could contribute to the accelerator controls community.

Appendix A

Firmware Update List of TS Module

Based on the performance measurements of the module, some areas for improvement have been identified:

1. **Synchronize the internal trigger with the "S" signal.** When the internal 25 Hz trigger was used in the old firmware, the counting position of the buffer might be misplaced by one due to the phase deviation with the "S" signal. It means the received trigger signal sometimes shifted to the next position. After the update of the firmware, the problem was solved.

2. **Add preset-delay function for "Trig" signal.** This function is to adjust the arrival time of the "S" signal relative to the external "Trig" signal. In J-PARC, the "Trig" signal needs to be delayed by 1 μs with respect to the "S" signal. To accommodate various signal-delay conditions that may be required in other accelerators, the delays from 0.5 μs to 7.5 μs are implemented with the new firmware.

3. **Add 30 Hz, 60 Hz, and 120 Hz internal triggers.** In the old TS module, only 25 Hz, 50 Hz, or 100 Hz internal trigger can be used. To be used in western Japan and other countries, 30 Hz, 60 Hz, and 120 Hz internal trigger functions are added.

4. **Clear data buffer each time when "S" signal comes.** With the old firmware, the current data overlapped the previous data in the same data buffer, since the previous data never removed. That means that when the "S" signal comes, only the first 62 or 130 cells (corresponding 2.48 s or 5.20 s) are flushed, the remaining cells are never flushed. After the firmware update, each time the "S" signal comes, the whole data buffer will be cleared.

5. **The counts in the last element of the data buffer should be valuable.** When we measured the RF signal, the last element in the data buffer (62nd or 130th) was always 0, which was understood as a bug. After updating the hardware, the last element became normal.

6. **Enlarge the LED indicating the duration of the module.** When any of the input signals (the "S", the "Trig", and inputs) is a pulse signal of 1 μs, the LED lighting time is too short for human eyes to see clearly. Therefore, the LED lighting time is extended by about 10 ms.

The issues 1 and 5 were caused by unsynchronized internal trigger. With the new firmware, the internal trigger is synchronized with the "S" signal. The issues 2 and 3 are essential upgrades if the module is used in other facilities. The issues 4 and 6 were updated for user's conveniences.

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Declaration of Authorship

I, Min YANG, declare that this thesis titled, 'Development of Timing Read-Back System toward Stable Accelerator Operation' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
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Signed: Min YANG

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